Burst Mode Timing: Practical considerations

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Comparison of 10G to 1G

- 8b10b has a consecutive identical digit length of 5 bits, which equals 4ns
- 64b66b has a CID length of 66 bits, which equals 6.4ns
- These values are quite close!
  - Certainly 8b10b is deterministically balanced, while 64b66b relies on statistics to make pathological cases rare

Extending current designs

- As the Ad-hoc slides illustrated, current 8b10b designs are quite simple
  - AGC controlled pre-amp
  - Simple tracking limiting-amp
  - BCDR based on PLL
- We believe that these designs can be extended to 10G, and without additional overhead time

AGC time

- AGC can be accomplished by
  - Controlling the APD reverse bias
  - Controlling the TIA impedance
- Each has its own peculiarities, but can be done
  - Overload is an issue we consider in part 2…
- Our prototyping effort tells us that 100ns is a good allowance for this function

Tracking Limiting amplifier

- This is in fact linked with the AC coupling issue
  - At 10G, AC coupling makes design so much easier and less device dependent
- A 10% baseline droop suggests a time constant of 10*64 bits = 64 ns
- It seems that 100ns is a good allowance for this function, as well.

Burst CDR

- PLL-based types are preferred for 10G
  - "Sampling" methods exceed device capability at 10G, since 50G of effective rate is needed
  - Continuous tracking capability of PLL
- Our prototyping efforts show that 200ns is ample time to allow phase recovery

Conclusions on timing

- PMD overhead time – the “AGC time” in the existing standard – can remain at 400ns
  - 200ns looks possible, so 400ns is easy
- PMA overhead time – the “CDR time” in the existing standard – can remain at 400ns
  - 200ns looks possible, so 400ns is easy
- Bottom line: Keep the burst timing as before.

Overload issue

- For sensitivity, “strong-to-weak” is the problem
  - Main solution is allowing more settling time
- For Rx longevity, “weak-to-strong” is the bigger problem, because a strong burst can wreak havoc
  - Drive amplifiers non-linear – then recovery time is big
  - Damage the little transistors that make for sensitive receivers
  - 10G brings its own problems
    - Low supply voltages = reduced signal range
    - High speed = low impedances = large currents = damage

Avoiding the stress

- What we need to avoid is the sharp rising edge of the incoming optical signal
  - We need a soft start
- Remember that this is AC coupled, so we also should take care of the falling edge
  - We need a soft stop

Protocol solution

- Begin the burst with a “pre” preamble
- In 64b66b coded systems with a 9dB ER Tx, this could be
  - 66b of ‘pre-bias’ – 00 0x00000000 00000000
    - That is about 6.5dB down from nominal power
  - 66b of ‘1/8 pattern – 01 0x01010101 01010101
    - That is about 3.8dB down from nominal power
  - 66b of ‘1/4 pattern – 01 0x11111111 11111111
    - That is about 2.1dB down from nominal power
  - Begin the preamble – 01 0x55555555 55555555
- Such a pattern ramps up the power over 3 block times (~20ns), which will greatly ease the overload problem
- A similar reversed pattern should be added at the end of the burst

Thank you