Proposal on Dual-Rate Burst-mode Receiver Timing

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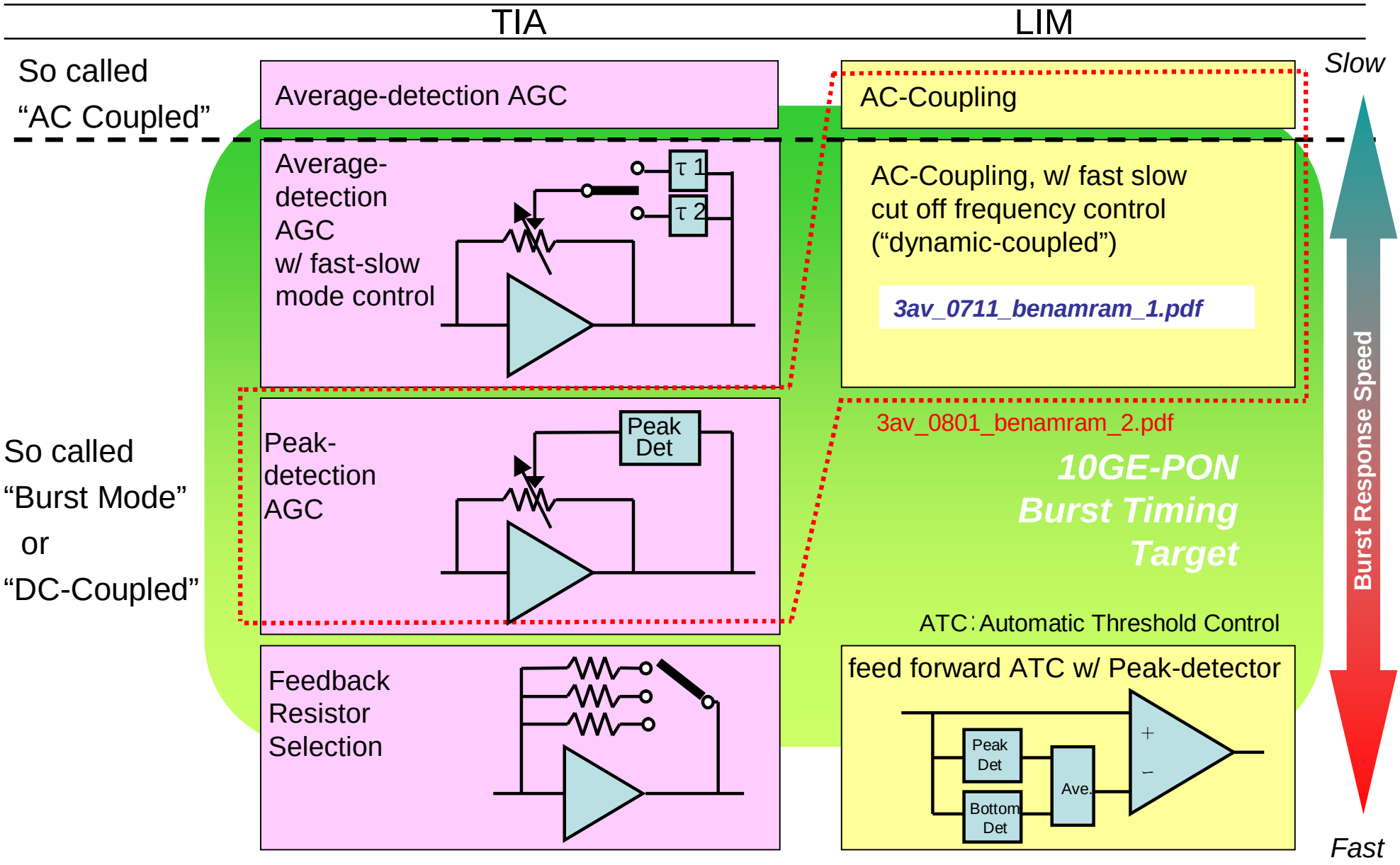
Requirement for 1G/10G Dual Rate Burst Mode Receiver Timing

- Loose maximum timing value to allow simple AC coupled design is preferred.
- Coexistence with current 802.3ah system is mandatory.
  - Maximum value of ($t_{receiver\_settling}$ + t_{cdr}) should be 800ns at 1G Mode.
    - Slower TIA AGC settling may not be allowable at 10G because TIA AGC settling for 1G Upstream is as same as that for 10G, with parallel dual-rate architecture. Therefore, maximum timing value of >800ns is not practical from the reason of dual-rate TIA AGC settling.
  - OLT can request overheads value of <800ns with 16 ns step using GATE MPCPDU.
    - The function is already installed in 802.3ah GE-PON

Burst Mode Receiver Technology Map



Simple AC Coupled Design (1)

- Target Technologies
  - TIA: Average-detection AGC
  - LIM: AC Coupled to TIA with 15 dB dynamic range
  - CDR:AC coupled to LIM with 0dB dynamic range
- Target Spec

A) Nominal time assignment

$t_{receiver\_settling} = t_{TIA\_agc} + t_{LIM} < 400ns$, $t_{cdr} < 400ns$

B) Practical time re-assignment

$t_{receiver\_settling} = t_{TIA\_agc} + t_{LIM} < 500ns$, $t_{cdr} < 300ns$

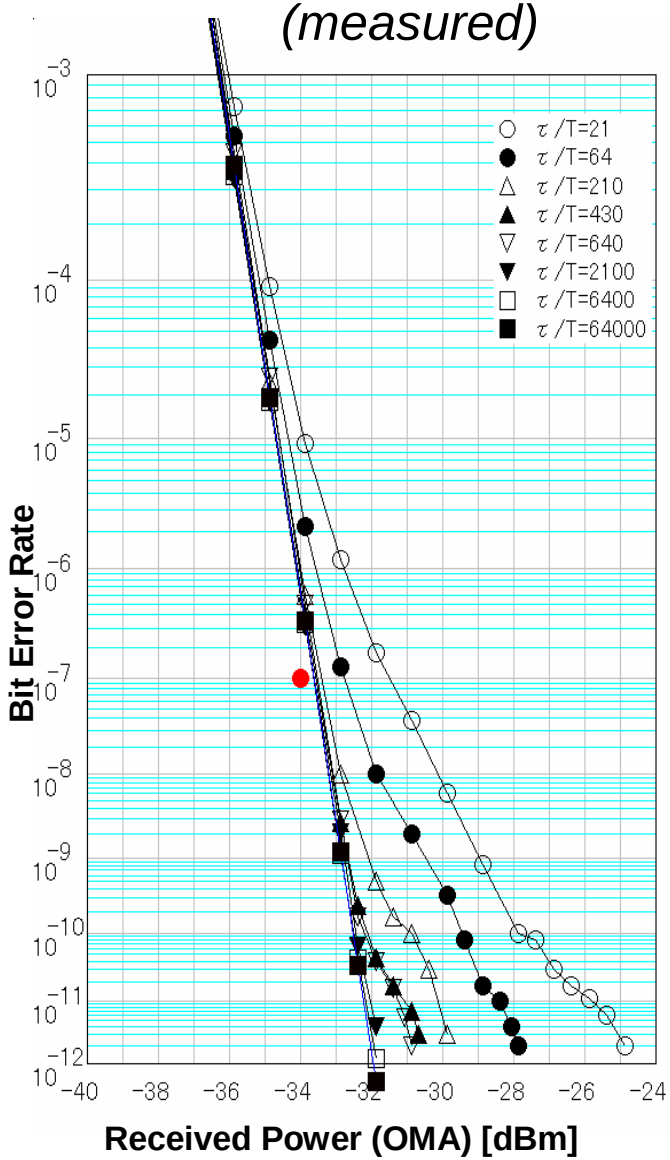
- Technical Background
  - CDR with <200ns settling is available.
  - Settling of TIA with average-detection is approximately as same as that of AC Coupling.

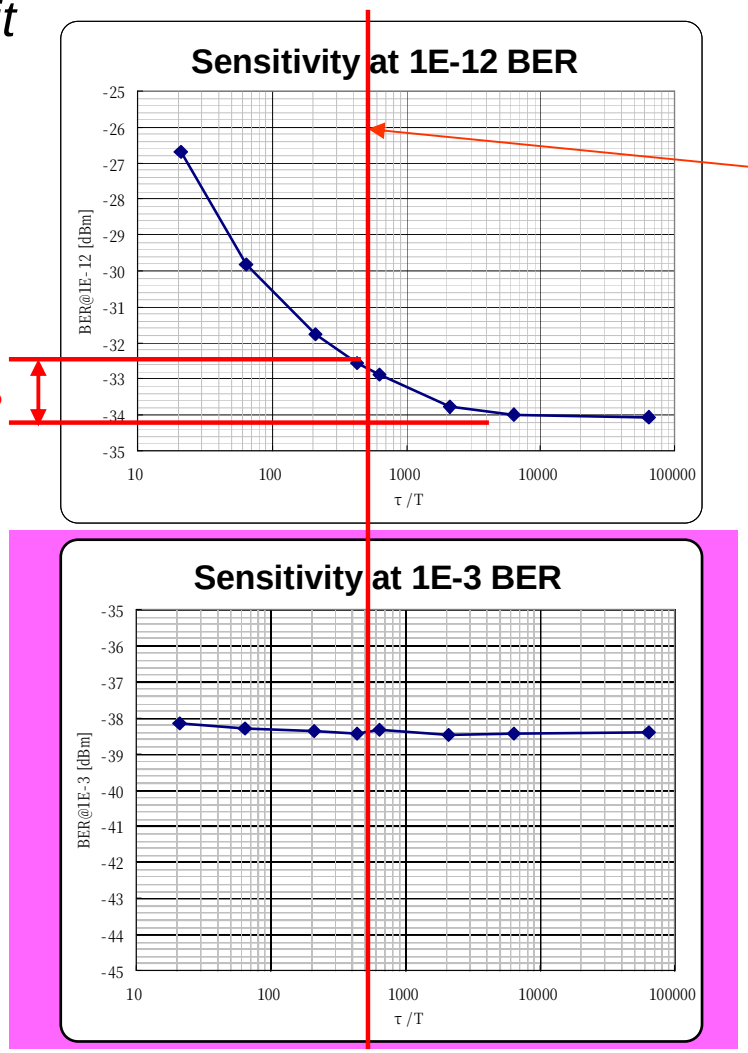
Simple AC Coupled Design (2)

- Settling time vs sensitivity penalty by CID limit
  - Briefly discussed in *3av_0801_benamram_2.pdf*
  - 250ns settling time at 20dB dynamic with 3MHz cut-off
  - Low sensitivity penalty correspond to 6% droop after 64bit CID
    - Considering dynamic range of 15dB and 0dB, <200ns and <<100ns settling can be feasible for TIA-LIM and LIM-CDR, respectively, with 3MHz cut-off.
- Sensitivity penalty by DC balance limit
  - Unlike with 8B/10B coding, DC balance is not guaranteed with 64B/66B coding.
  - Insufficient low cut-off causes significant penalty at lower BER.
    - Verification by experimental measurement is practical rather than by simulation.

Simple AC Coupled Design (3)

Penalty including DC balance limit (measured)





3MHz lower cut-off

Experimental Condition

- **1.25Gbps**
- **Continuous mode**
- **PRBS31**
- **ER: 10dB**
- **APD, M=9**

Sensitivity at 1E-3 BER with 3MHz suggests no sensitivity degradation at 1E-12 BER after FEC.

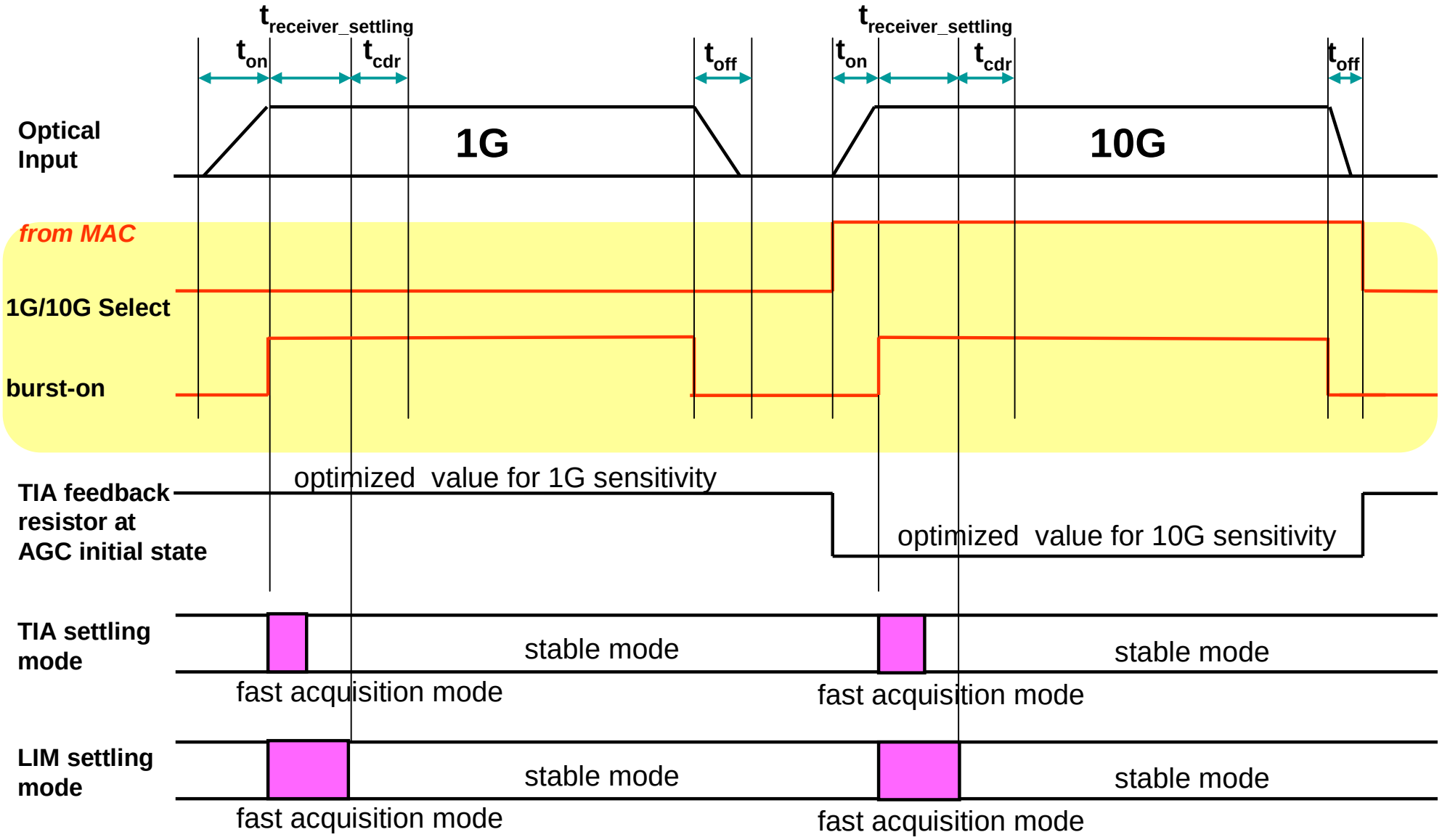
Simple AC Coupled Design (4)

- $t_{receiver\_settling} + t_{cdr} < 800ns$ can be feasible with simple AC-coupled technologies.
- To allow $t_{receiver\_settling} > t_{cdr}$ budgeting is more likely.

Timing Signal for "Tight Spec" Burst-mode Receiver

- In order to operate fast acquisition/stable mode control in “Burst-Mode” receiver, the receiver have to know start timing of the burst to be received.
- For 8B/10B encoded data with 1E-12 BER environment, it can internally be generated with the combination of fast response power detection and self reset.
- For 64B/66B encoded data with 1E-3 BER environment, neither fast response power detection nor self reset can easily be implemented.
- To deliver “burst-on” timing signal from MAC is required in order to assist burst mode receiver.
- This kind of timing signal is often installed in PON chip for 802.3ah or ITU-T PON.
  - It would be no problem to keep timing signal spec as vendors matter.

Example of Dual-Rate Burst-Mode Receiver Timing



Summary

- It is reasonable for 10G Upstream Burst Mode Receiver Timing Spec to keep that of current 802.3ah.
  - $t_{receiver\_settling} + t_{cdr}$ should be less than 800ns.
  - $t_{receiver\_settling}$ value is not specified ("400ns" means only "informative" value) .
  - OLT broadcast $t_{receiver\_settling} + t_{cdr}$ value of <800ns with 16 ns step using GATE MPCPDU.

- Timing signal from MAC to assist “burst mode” receiver is required for receiving 64B/66B encoded data at <1E-3 BER.
  - Spec for timing signal can be vendors matter