10GEPON Jitter Budget

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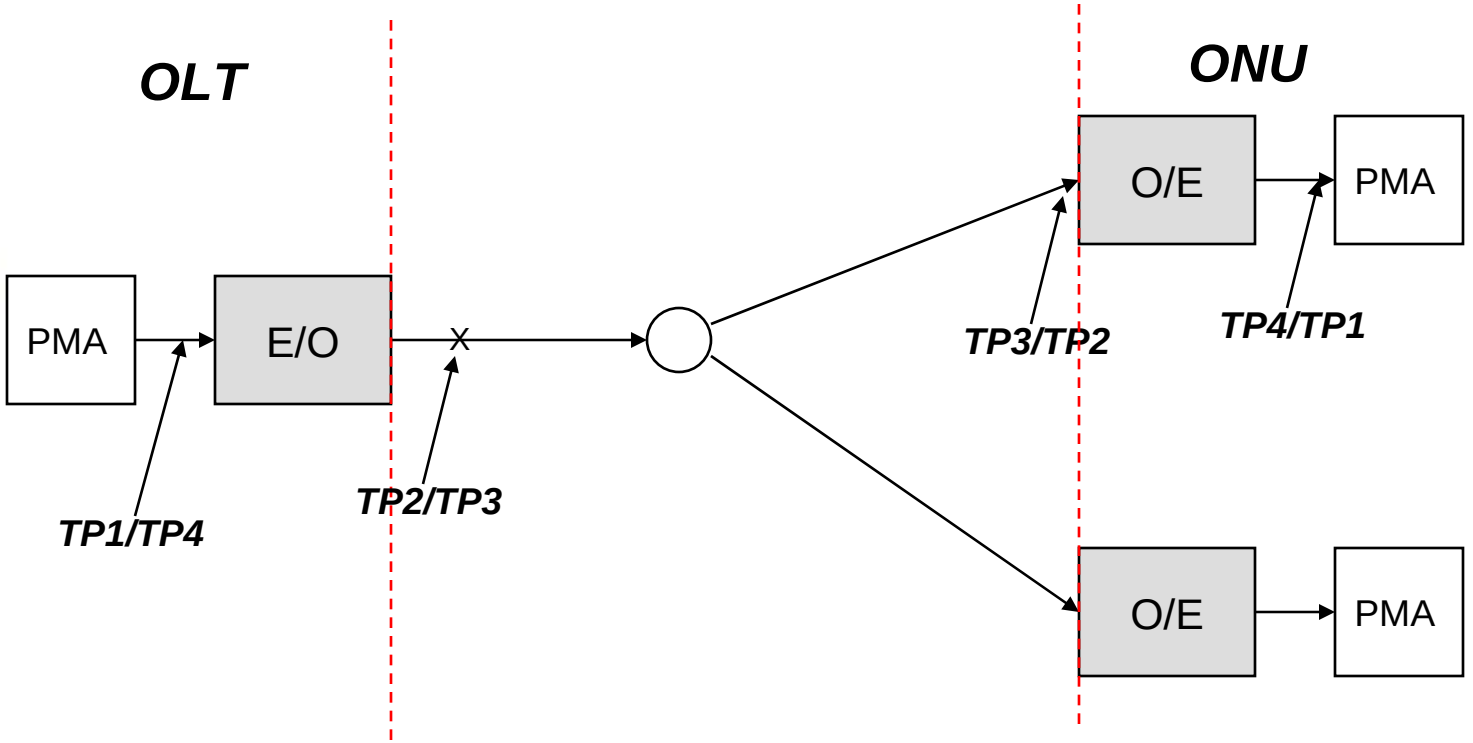
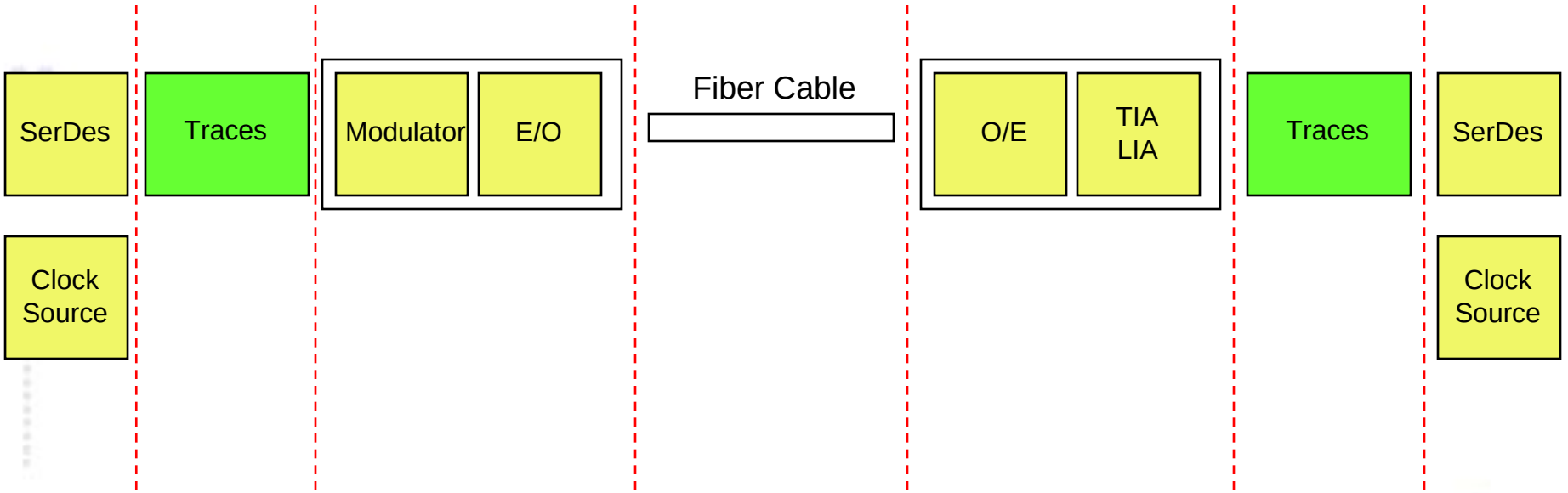
What is Jitter Budget?

- Jitter Budget is the collection of the Total Jitter generated from each component in the data path
- How much internal jitter do we generate from each component in the channel?

The Data Path



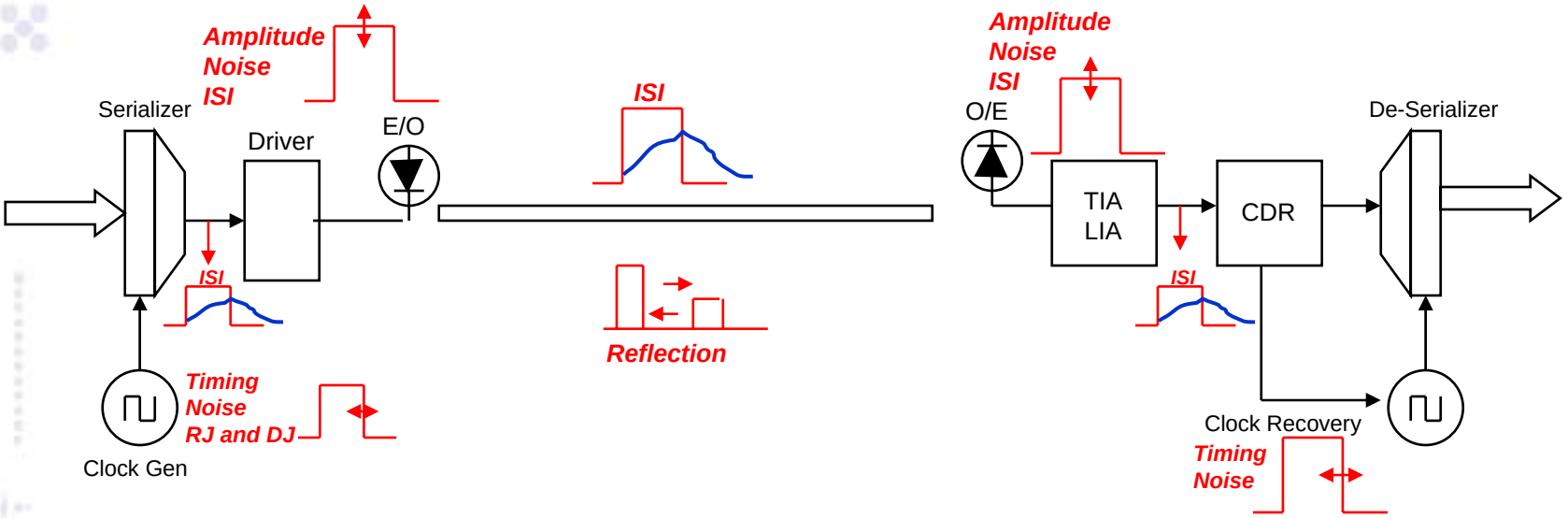
High Speed Optical Interface



Test Points

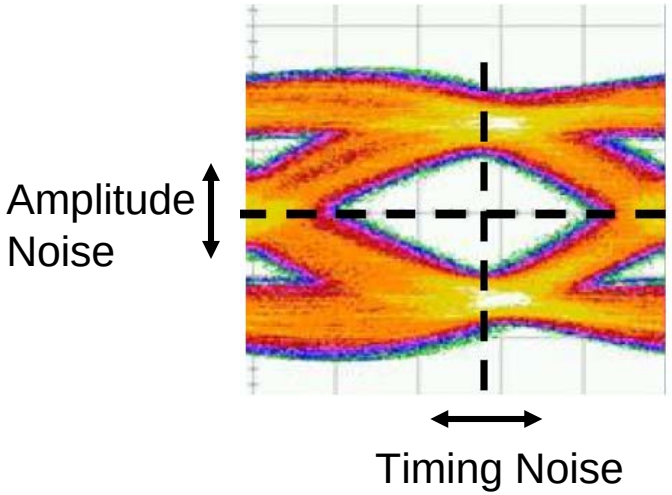
- TP1
  - Laser Driver/Modulator
- TP2
  - E/O (DFB Laser, EML Laser)
- TP3
  - Optical Fiber
- TP4
  - O/E (APD, PIN)
  - TIA
  - LIA

Jitter Components



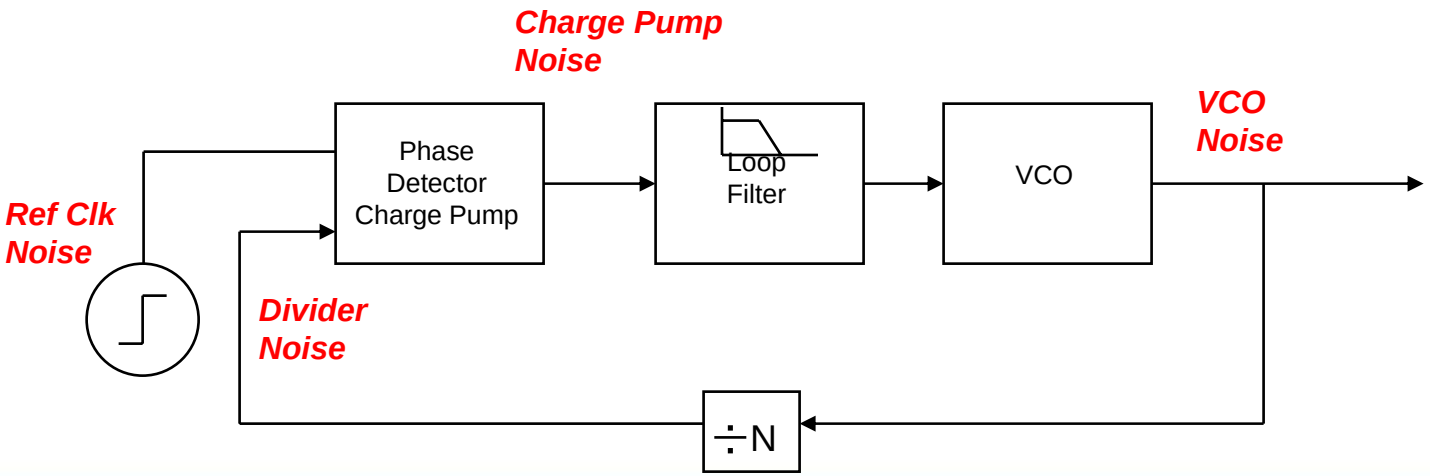
Circuit Related Noise

- Amplitude Noise
  - Thermal and Flicker Noise
  - Supply and Substrate
  - Offsets
- Timing Noise
  - Random Jitter
  - Deterministic Jitter (ISI)
  - PLL Jitter
  - VCO Clock Buffer
  - Skew



PLL – Critical Parameters

- The critical parameters of the PLL are:
  - Phase noise and jitter
  - Acquisition time
  - Acquisition range
- VCO Noise and Charge Pump Noise are the dominate noise
  - Thermal Noise
  - Flicker Noise



The Challenge

- There are few main parameters which cause to Jitter in High Speed Communication
  - PLL Architecture
  - Reference Clock/PLL
  - Power Supply
    - Bounded and Uncorrelated Jitter
    - Impact:
      - Reference Clock
      - PLL
      - SerDes
  - Transmitter/Receiver
  - Signal Integrity
    - DJ, ISI and Data Dependent Jitter
    - Impedance Matching
      - Reflection
      - Cross Talk
- Chip Package and Print Board create Jitter
- Receiver can tolerate a Maximum amount of Jitter
- In 10Gbps, The CDR at the Receiver side should be able to handle the accumulated Jitter from the whole channel including interfaces, connectors, traces etc.

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