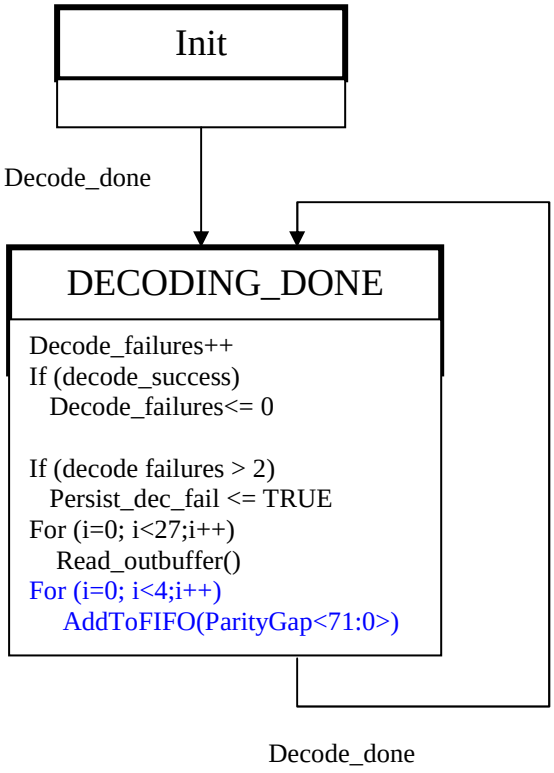

Figure 92-22 – FEC Decoder state diagram

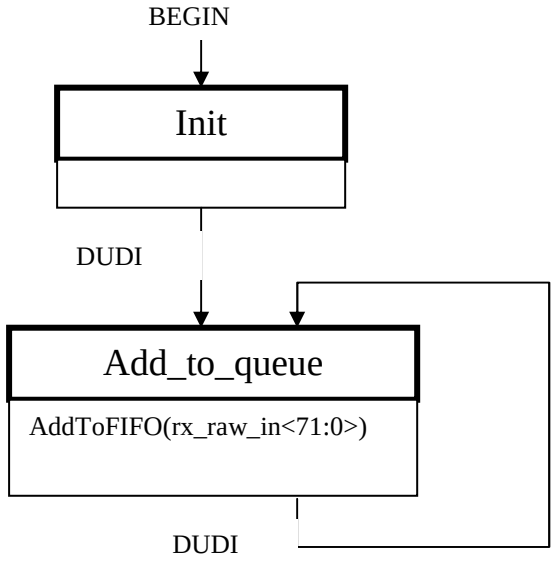

Figure 92-26 – PCS Idle Insertion, input process state diagram

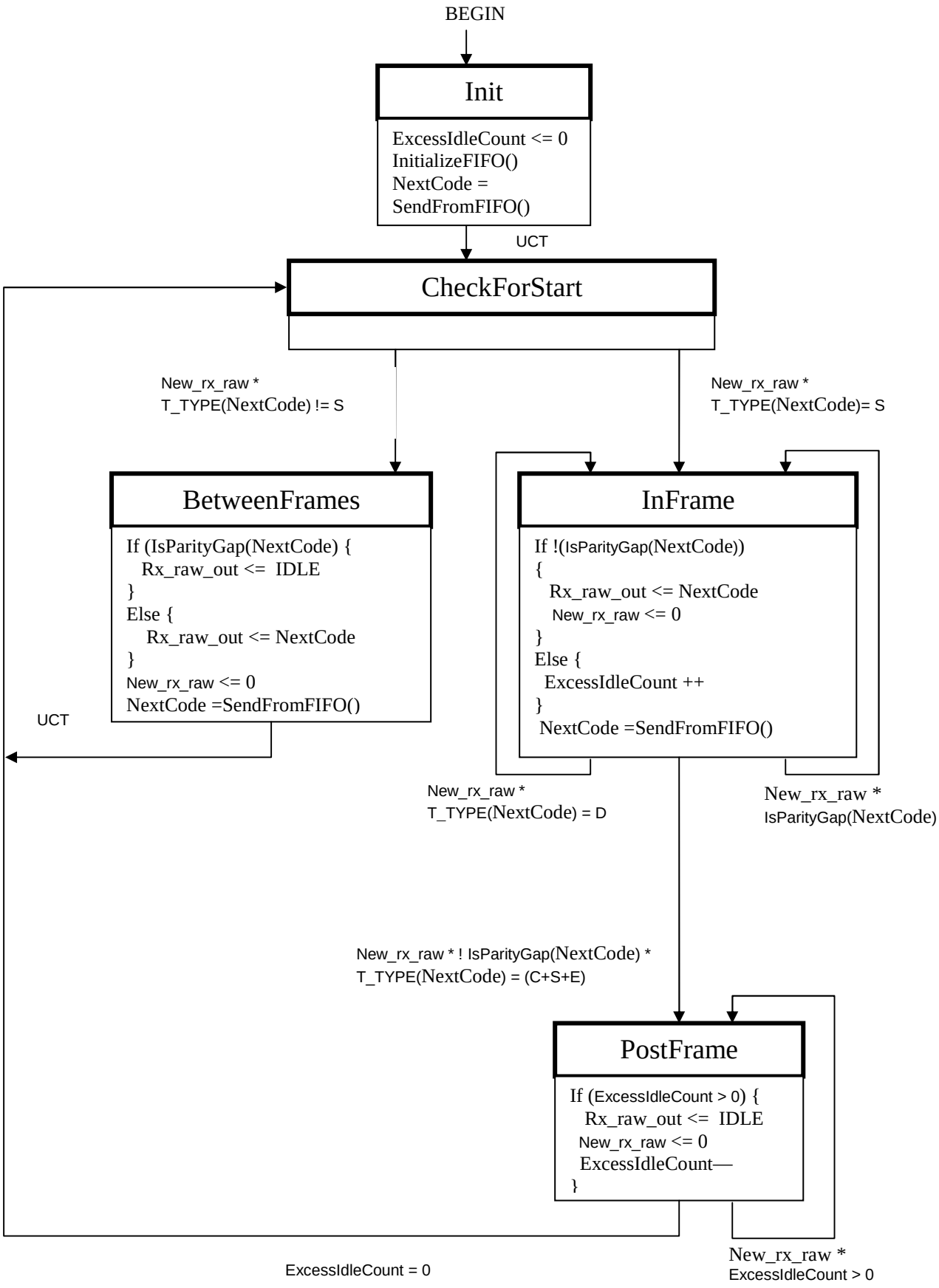

Figure 92-27 – PCS Idle Insertion, output process state diagram

[Add new constant to 92.2.3.7.1:]

ParityGap<71:0>: A vector consisting of 72 successive '1's. This constant occupies the slots in the datastream where parity was removed by the FEC decoder. The constant's value is reserved and never otherwise appears in the datastream (cf. **46.3.2.2**.).

[Add new variable to 92.2.3.7.2:]

new_rx_raw: becomes TRUE whenever a new value of rx_raw_out is required (ie. to write over the XGMII) and is FALSE otherwise. The Idle insertion process sets **new_rx_raw** to FALSE after it has written a new value to rx_raw_out.

[Add new function to 92.2.3.7.3:]

IsParityGap(rx_vector<71:0>): returns TRUE if rx_vector is the ParityGap constant and FALSE otherwise.

[modify the sentence on 125 line 37 to say the following:]

This FIFO is internal to the Idle Insertion function and is shared by input and output processes of Idle Insertion. Upon initialization, all elements of this array are set to contain 72-bit vectors representing /I/ characters. FIFO_II is a zero-based array of size sufficient to hold all the parity data associated with a maximum size frame.