Re-consider 10G CDR Locking Time Specs for PR30 Upstream

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Introduction

- Here is what D2.0 states the 10G CDR locking time

76.3.2 Extensions for 10GBASE-PR-D and 10/1GBASE-PRX-D

76.3.2.1 CDR lock timing measurement for the upstream direction

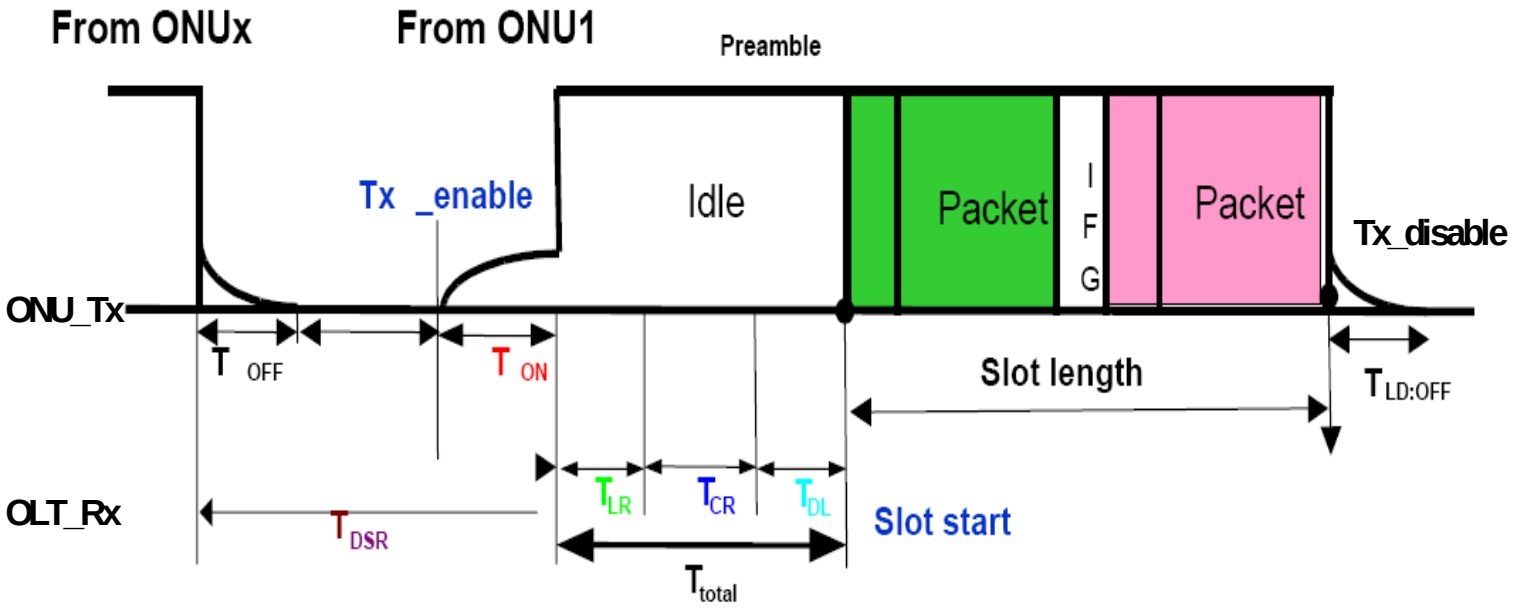
CDR lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase and frequency lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when electrical signal after the PMD at TP4, as illustrated in @@Figure 75-3@@ and @@Figure 75-4@@, reaches the conditions specified in @@Subclause 75.9.16@@ for receiver settling time to the moment when the phase and frequency are recovered and jitter is maintained for a network with BER of no more than 10^{-3}.

A PMA instantiated in an OLT becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (0x55…) at TP4.

- The intention of this talk is to examine measurement results which show 10G CDR locking time can be safely specified as <200ns, while still taking advantage of the continuous RX blocks.

Burst timing definitions

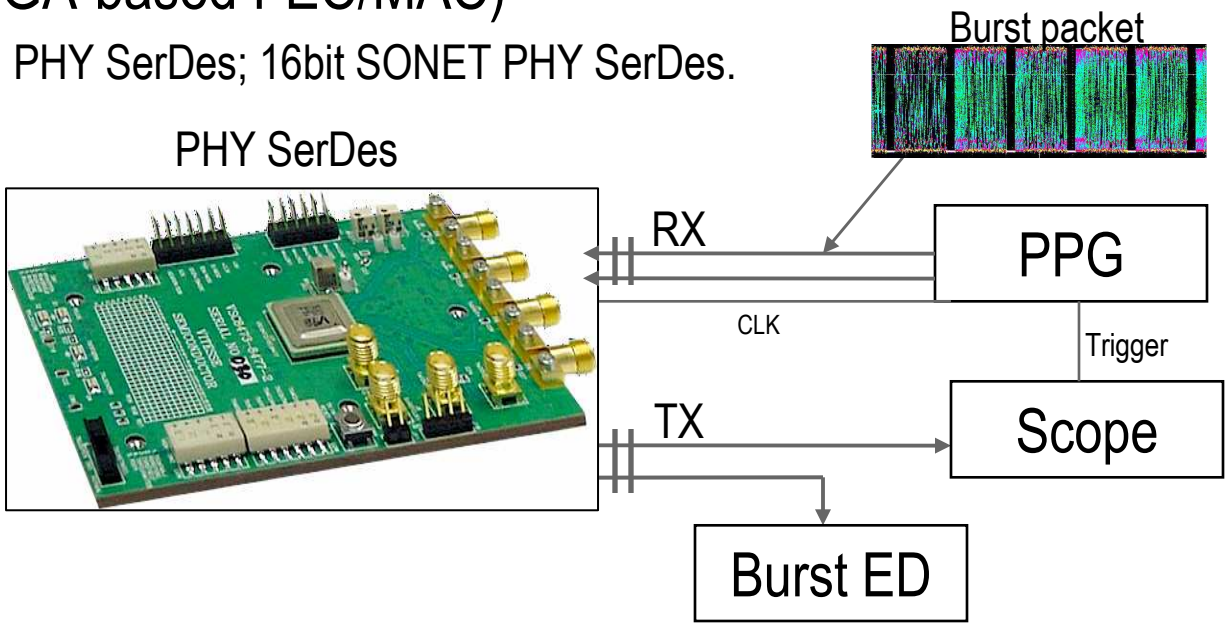
- Burst timing definition per. 802.3ah.
  - PR30-D defines $T_{receiver\_setting}$ ~ 800ns, T_{cdr} ~ 400ns.
    - Ref. to 802.2ahD3.3 Fig. 60-7 – P2MP timing parameter definition



***Source**: "Passive Optical Networks: Principles and Practice". Academic Press, 2007, Chapter 4.*

Setup Confg.

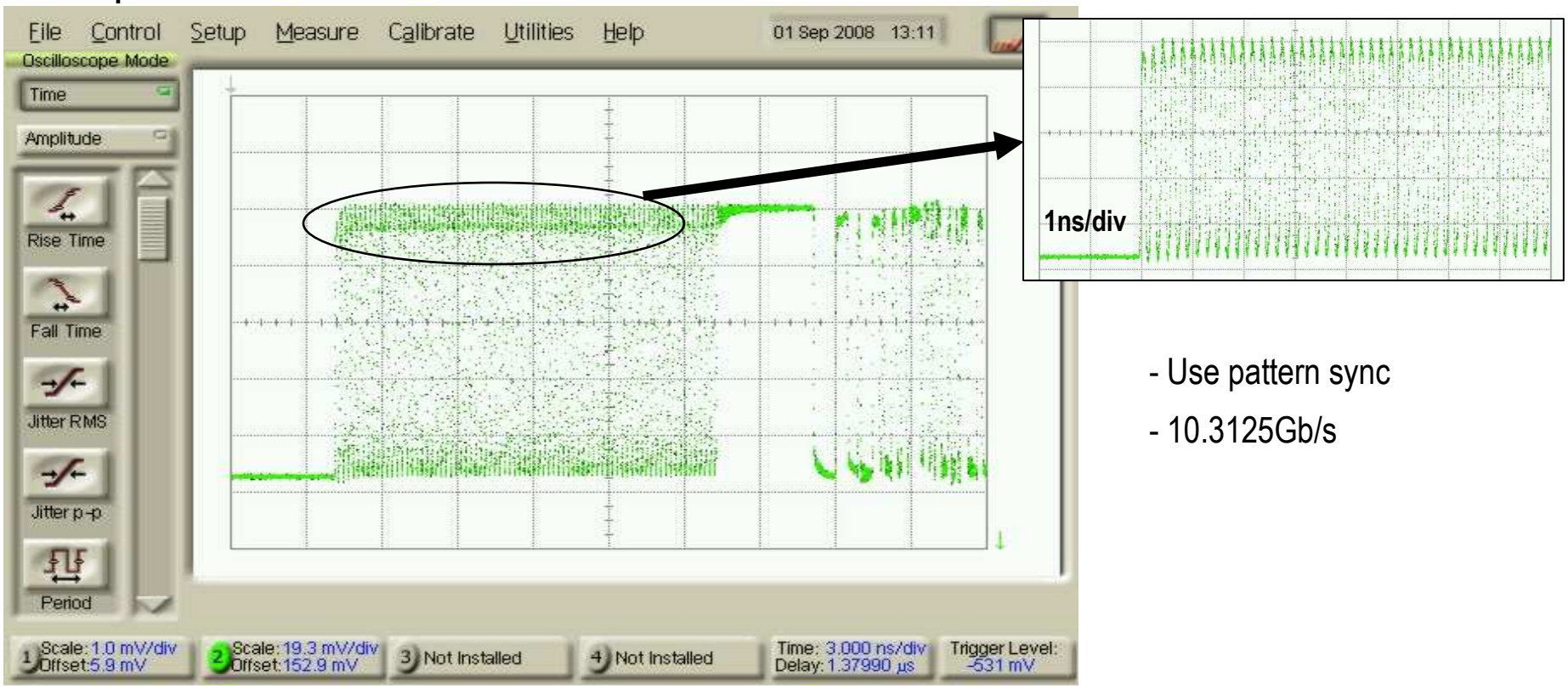
- Take advantage of complete PON testing employs two ONUs.
- But this test focus on electrical test only for one ONU case, so PPG – DUT – ED and/or Scope for 10G rate.
  - Both DUT output eye diagram and burst BER reading are monitored.
    - Delimiter is considered as part of payload when recording burst BER.
- Consider two kinds of PHY SerDes (with convenient interfaces to connect FPGA-based FEC/MAC)
  - 4-bit XAUI PHY SerDes; 16bit SONET PHY SerDes.



Input Burst Packet at 10G

- Follow 10G EPON testing burst packet
  - Testing burst pattern: burst packet length 7680bits with guard time 5362bits.
  - Total preamble 1010 pattern **(>1000bits),** Delimiter (~40bit), Payload with PRBS 2^{15}-1.
    - Delimiter is considered as part of payload in checking burst BER.

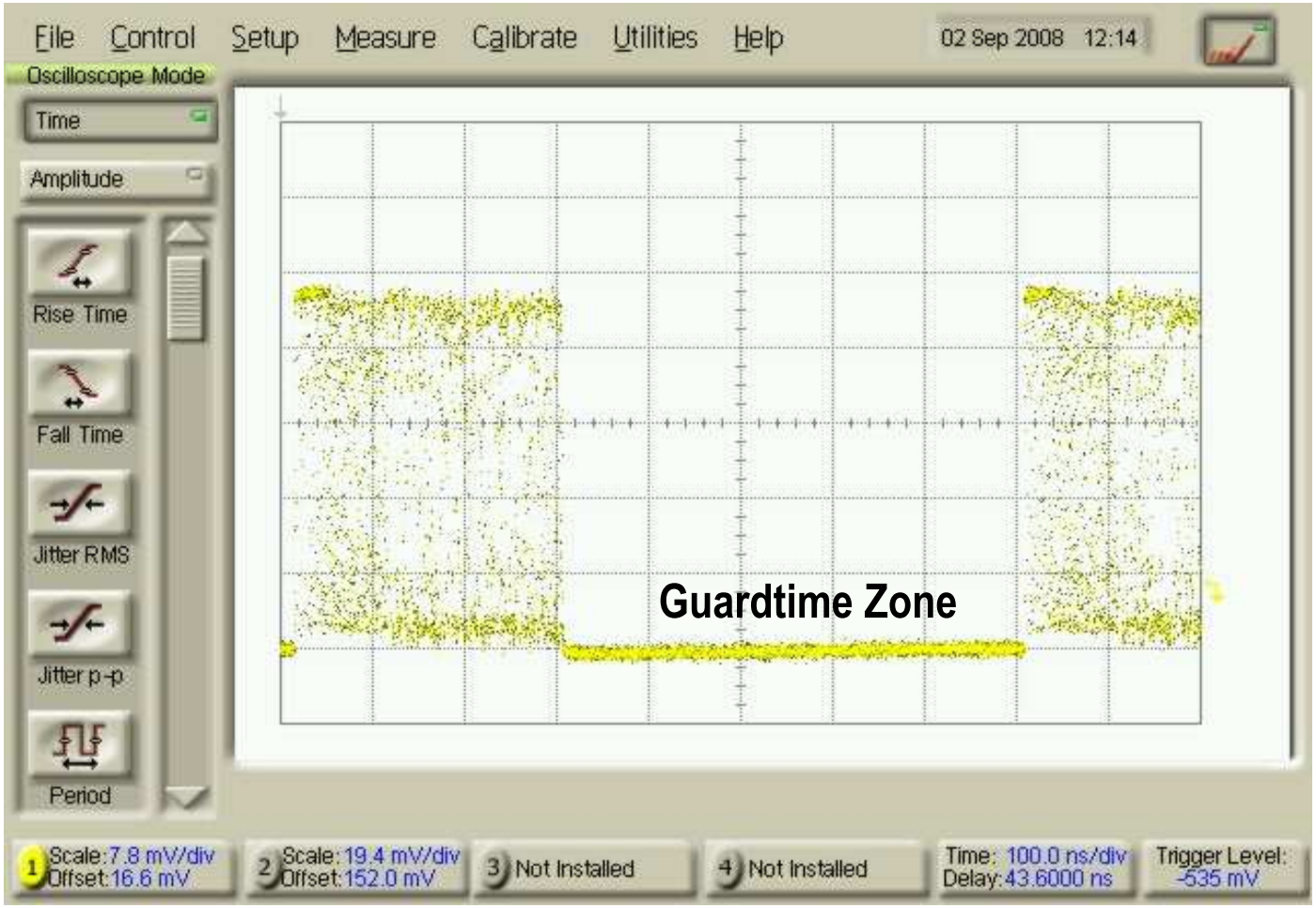
Example:



- Use pattern sync
- 10.3125Gb/s

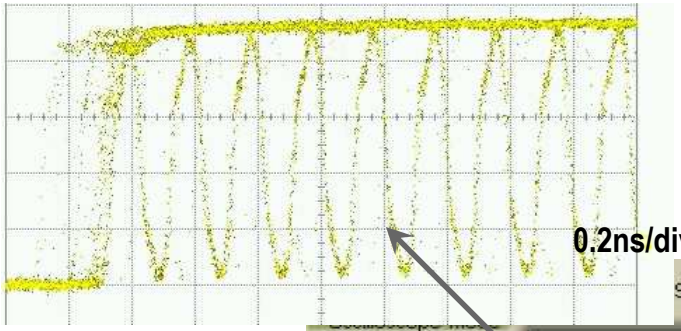
XAUI SerDes Burst Output at 10G

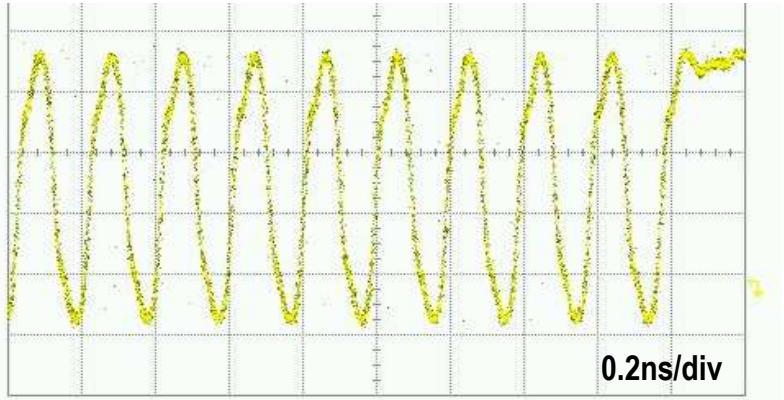
- Quiet guardtime zone
  - **With preamble 1052bits for PMA loopback.**

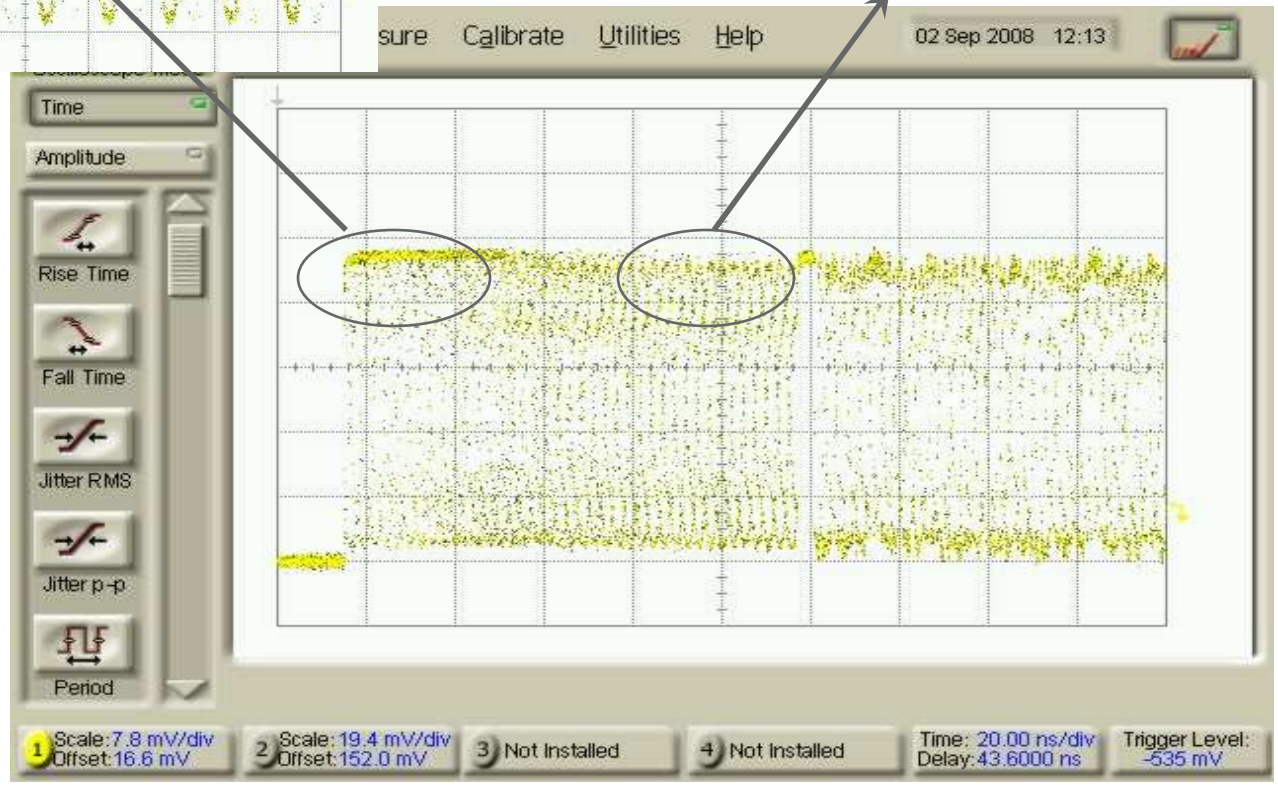


XAUI SerDes Burst Output at 10G

- XAUI SerDes board use the line gen. mo
  - **For preamble <u>1052bits</u> with PMA loopback**.

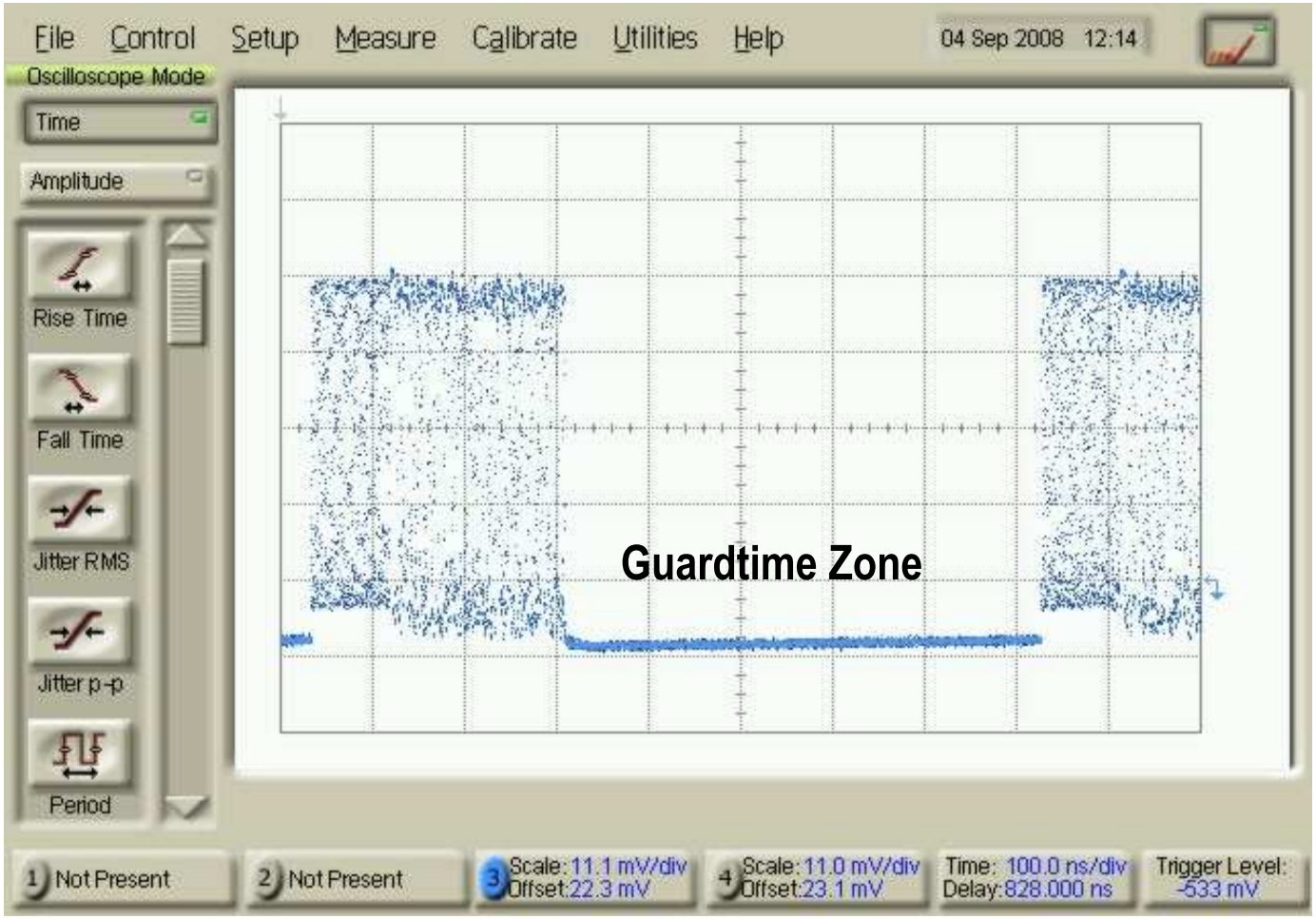






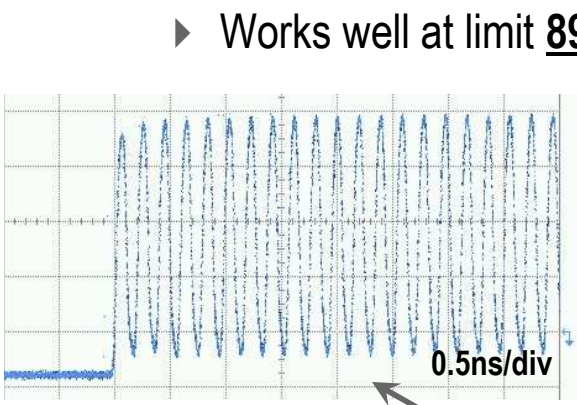
16-bit SerDes Burst Output at 10G

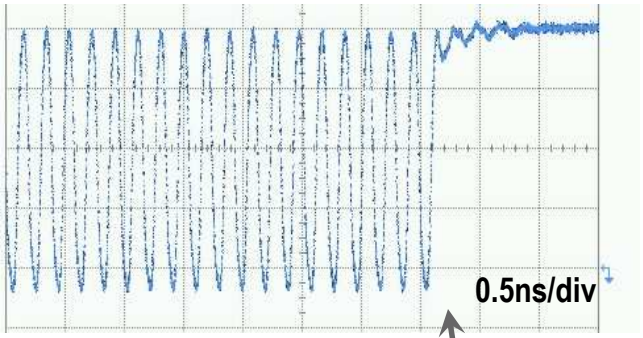
- 16-bit SerDes board use the line gen. mode with 300-pin loopback.
  - For **892** bits preamble with quiet guard time zone

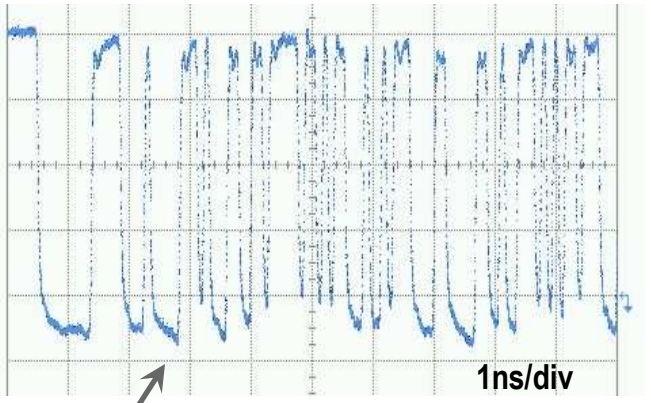


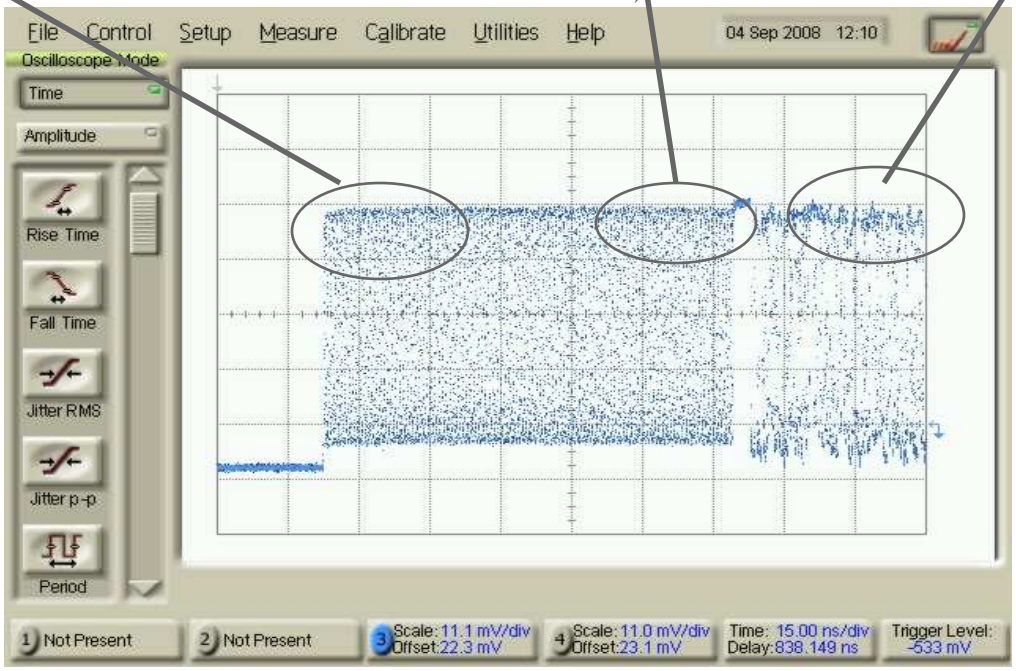
16-bit SerDes Burst Output at 10G

- 16-bit SerDes board use the line gen. mode.
  - Works well at limit **892** bits preamble.









Recommendation

Demonstrate fast locking times well exceed 400ns locking.

- XAUI PHY Serdes
  - PMA loopback with line mode.
  - Comfortable locking time better than 1052bits (102ns)
- SONET 16-bit Serdes.
  - Employ the line gen. mode with 300-pin loopback.
  - Comfortable locking time better than 892bits (86ns).

Recommend:

- Specifying the 10G EPON CDR locking time as 200ns.
  - Take into account worst-case margin
  - Maintain AC coupling in TP4 between PostAmp and PMA.
  - Still able to take advantage of the continuous RX blocks.