45. Management Data Input/Output (MDIO) Interface

45.1 Overview

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Insert Subclauses 45.2.1.92 through 45.2.1.91 with respective tables, as presented below. Renumber succeeding tables as appropriate.

45.2.1.92 10/1GBASE-PRX FEC ability register (Register 1.182)

The assignment of bits in the 10/1GBASE-PRX FEC ability register is shown in Table 45–69.

Table 45–69—10/1GBASE-PRX FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.182.15:3	Reserved	Value always zero, writes ignored	RO
1.182.2	10/1GBASE-PRX FEC error indication ability	A read of 1 in this bit indicates that the 10/1GBASE-PRX PHY is able to report FEC decoding errors to the PCS layer. In the OLT, this bit always has a value of 1.	RO
1.182.1	10/1GBASE-PRX receiver FEC ability	A read of 1 in this bit indicates that the 10/1GBASE-PRX receiver supports FEC. In the ONU, this bit always has a value of 1.	RO
1.182.0	10/1GBASE-PRX transmitter FEC ability	A read of 1 in this bit indicates that the 10/1GBASE-PRX transmitter supports FEC. In the OLT, this bit always has a value of 1.	RO

[a]RO Read only

45.2.1.92.1 10/1GBASE-PRX FEC error indication ability (1.182.2)

When read as a one, this bit indicates that the 10/1GBASE-PRX FEC is able to indicate decoding errors to the PCS layer (see @@Subclause 77.2.3.3@@ and @@any_reference_in_clause_65@@). When read as a zero, the 10/1GBASE-PRX FEC is not able to indicate decoding errors to the PCS layer. 10/1GBASE-PRX FEC error indication is controlled by the FEC enable error indication bit in the FEC control register (see @@Subclause 45.2.1.85.2@@). In the OLT, this bit always has a value of 1.

45.2.1.92.2 10/1GBASE-PRX receiver FEC ability (1.182.1)

When read as a one, this bit indicates that the 10/1GBASE-PRX receiver supports FEC. When read as a zero, the 10/1GBASE-PRX receiver does not support FEC. In the ONU, this bit always has a value of 1.

45.2.1.92.3 10/1GBASE-PRX transmitter FEC ability (1.182.0)

When read as a one, this bit indicates that the 10/1GBASE-PRX transmitter supports FEC. When read as a zero, the 10/1GBASE-PRX transmitter does not support FEC. In the OLT, this bit always has a value of 1.

45.2.1.93 10/1GBASE-PRX FEC control register (Register 1.183)

The assignment of bits in the 10/1GBASE-PRX FEC control register is shown in Table 45–70.

Table 45–70—10/1GBASE-PRX FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.183.15:3	Reserved	Value always zero, writes ignored	RO
1.183.2	FEC enable error indication	In the ONU, a write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer. Writes are ignored in the OLT.	R/W
1.183.1	Enable FEC for 10/1GBASE-PRX receiver	In the OLT, a write of 1 to this bit enables FEC in the receiver and a write of 0 disables FEC in the receiver. Writes are ignored in the ONU	
1.183.0	Enable FEC for 10/1GBASE-PRX transmitter	In the ONU, a write of 1 to this bit enables FEC in the transmitter and a write of 0 disables FEC in the transmitter. Writes are ignored in the OLT.	

[a]R/W = Read/Write, RO Read only

45.2.1.93.1 FEC enable error indication (1.183.2)

This bit enables the 10/1GBASE-PRX FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10/1GBASE-PRX PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero the error indication function is disabled. Writes to this bit are ignored and reads return a zero if the 10/1GBASE-PRX FEC does not have the ability to indicate decoding errors to the PCS layer (see @@Subclause 45.2.1.84.2@@ and @@Subclause 74.8.3@@). Any write operations to this bit are ignored in the OLT.

45.2.1.93.2 Enable FEC for 10/1GBASE-PRX receiver (1.183.1)

When written as a one, this bit enables FEC for the 10/1GBASE-PRX receiver. When written as a zero, FEC is disabled in the 10/1GBASE-PRX receiver. This bit shall be set to zero upon execution of PHY reset. Any write operations to this bit are ignored in the ONU.

45.2.1.93.3 Enable FEC for 10/1GBASE-PRX transmitter (1.183.0)

When written as a one, this bit enables FEC for the 10/1GBASE-PRX transmitter. When written as a zero, FEC is disabled in the 10/1GBASE-PRX transmitter. This bit shall be set to zero upon execution of PHY reset. Any write operations to this bit are ignored in the OLT.

45.2.1.94 10/1GBASE-PRX FEC corrected blocks counter (Register 1.184, 1.185)

The assignment of bits in the 10/1GBASE-PRX FEC corrected blocks counter register is shown in Table 45–71. See @@Subclause 74.8.4.1@@ for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.184, 1.185 are used to read the value of a 32-bit counter. When registers 1.184 and 1.185 are used to read the 32-bit counter value, the register 1.184 is read first, the value of the reg-

ister 1.185 is latched when (and only when) register 1.184 is read and reads of register 1.185 returns the latched value rather than the current value of the counter.

Table 45–71—10/1GBASE-PRX FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.184.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.185.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.95 10/1GBASE-PRX FEC uncorrected blocks counter (Register 1.186, 1.187)

The assignment of bits in the 10/1GBASE-PRX FEC uncorrected blocks counter register is shown in Table 45–72. See @@Subclause 74.8.4.2@@ for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.186, 1.187 are used to read the value of a 32-bit counter. When registers 1.186 and 1.187 are used to read the 32-bit counter value, the register 1.186 is read first, the value of the register 1.187 is latched when (and only when) register 1.186 is read and reads of register 1.187 returns the latched value rather than the current value of the counter.

Table 45–72—10/1GBASE-PRX FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.186.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.187.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over