MPCP FEC issues:
Impact of *Deficit Idle Count*

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Deficit Idle Count Definition

46.3.1.4 Start control character alignment

On transmit, it may be necessary for the RS to modify the length of the <inter-frame> in order to align the Start control character (first octet of preamble) on lane 0. This shall be accomplished in one of the following two ways:

1) A MAC implementation may incorporate this RS function into its design and always insert additional idle characters to align the start of preamble on a four byte boundary. Note that this will reduce the effective data rate for certain packet sizes separated with minimum inter-frame spacing.

2) Alternatively, the RS may maintain the effective data rate by sometimes inserting and sometimes deleting idle characters to align the Start control character. When using this method the RS must maintain a Deficit Idle Count (DIC) that represents the cumulative count of idle characters deleted or inserted. The DIC is incremented for each idle character deleted, decremented for each idle character inserted, and the decision of whether to insert or delete idle characters is constrained by bounding the DIC to a minimum value of zero and maximum value of three. Note that this may result in inter-frame spacing observed on the transmit XGMII that is up to three octets shorter than the minimum transmitted inter-frame spacing specified in Clause 4; however, the frequency of shortened inter-frame spacing is constrained by the DIC rules. The DIC is only reset at initialization and is applied regardless of the size of the IPG transmitted by the MAC sublayer. An equivalent technique may be employed to control RS alignment of the Start control character provided that the result is the same as if the RS implemented DIC as described.

Impact of the RS-layer *Deficit Idle Count* algorithm on delay variation

1) The RS “effectively maintains the data rate” by “sometimes inserting and sometimes deleting Idle characters” (46.3.1.4). So:

   - When the RS inserts an IDLE, tx-direction RS latency increases by 8 bit times

   - When the RS deletes an IDLE, tx latency decreases by 8 bit times

2) Number of IDLEs deleted may exceed the number of IDLE inserted by as much as 3 – but no more.

   - Hence, RS transmit delay variation due to DIC is 24 bits (.15 TQ)

Impact of *Deficit Idle Count* on data transmitted by the MAC

- The cumulative number of IDLEs deleted by the RS but not yet restored is termed the *DIC value*
  - *DIC value* is maintained by the RS and oscillates between 0 to 3

- At any given time, the *DIC value* indicates the amount of left shift (in bytes) that the RS imposes on the MAC data before transmitting it on the XGMII

Current value for DIC in RS	**Resulting leftward shift of data bytes between MAC layer and XGMII**
0	0
1	1
2	2
3	3

Does *Deficit Idle Count* affect MPCP's calculation of FEC overhead?

- The RS DIC algorithm updates the DIC value at each start-of-packet
  - just as MPCP checks for the parity region at each start-of-packet (by determining whether *fecOffset* >= *216)*

- As we see from the following table, there is *no case* where at start-of-packet (*fecOffset* >= *216)*, but ((*fecOffset - DIC)* < *216). So: No, DIC does not affect MPCP*

fecOffset **of Start character**	**Resulting RS value for DIC**
216	0
217	1
218	2
219	3

Problem and Remedy

1) Problem: Control Multiplexers (OLT and ONU) delay each start-of-packet until the beginning of a 4-byte column boundary

   - We've seen this is unnecessary

   - It's also undesirable:
     - Complex (and incorrect) logic
     - When building REPORT, the ONU must either pre-estimate the amount of extra bytes for column completion, or else use worst case value of IPG=15
     - wasted byte overhead

2) Remedy:

   - Modify the definition of alignmentCorrect (77.2.2.3) to read as follows:

alignmentCorrect

TYPE: Boolean

This variable is an alias for the following condition (fecOffset < FEC_PAYLOAD_SIZE). This variable is set true during the payload part of an FEC codeword.