A "Subset PHY" Approach for 10GBASE-KR Energy Efficient Ethernet

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Overview

- ## Objective
  - Identify an approach that will offer fast transition times from the 10G rate to a 1G rate to reduce energy consumption during periods of low link utilization on BP Ethernet KR links

- ## Two Possible Approaches
  - Rapidly switch between 10GBASE-KR and 1000BASE-KX
  - Define a "Subset" of 10GBASE-KR
  - Subset approach introduced in this presentation

- ## Line code for lower data rate is a simple subset of the higher data rate (standard) mode
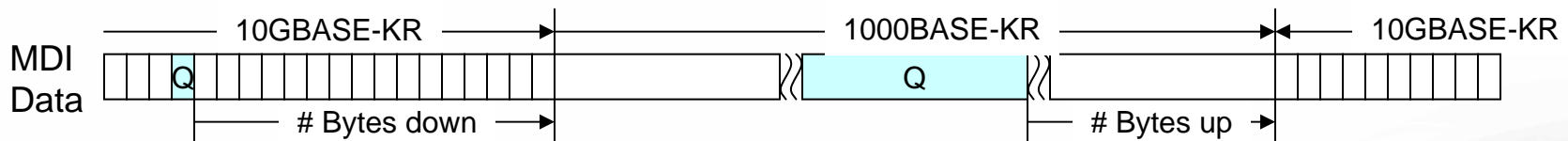 - Subset PHY implemented by simply turning off elements of higher data rate standard parent PHY

- ## Communication Method Using Q-Ordered Sets Introduced
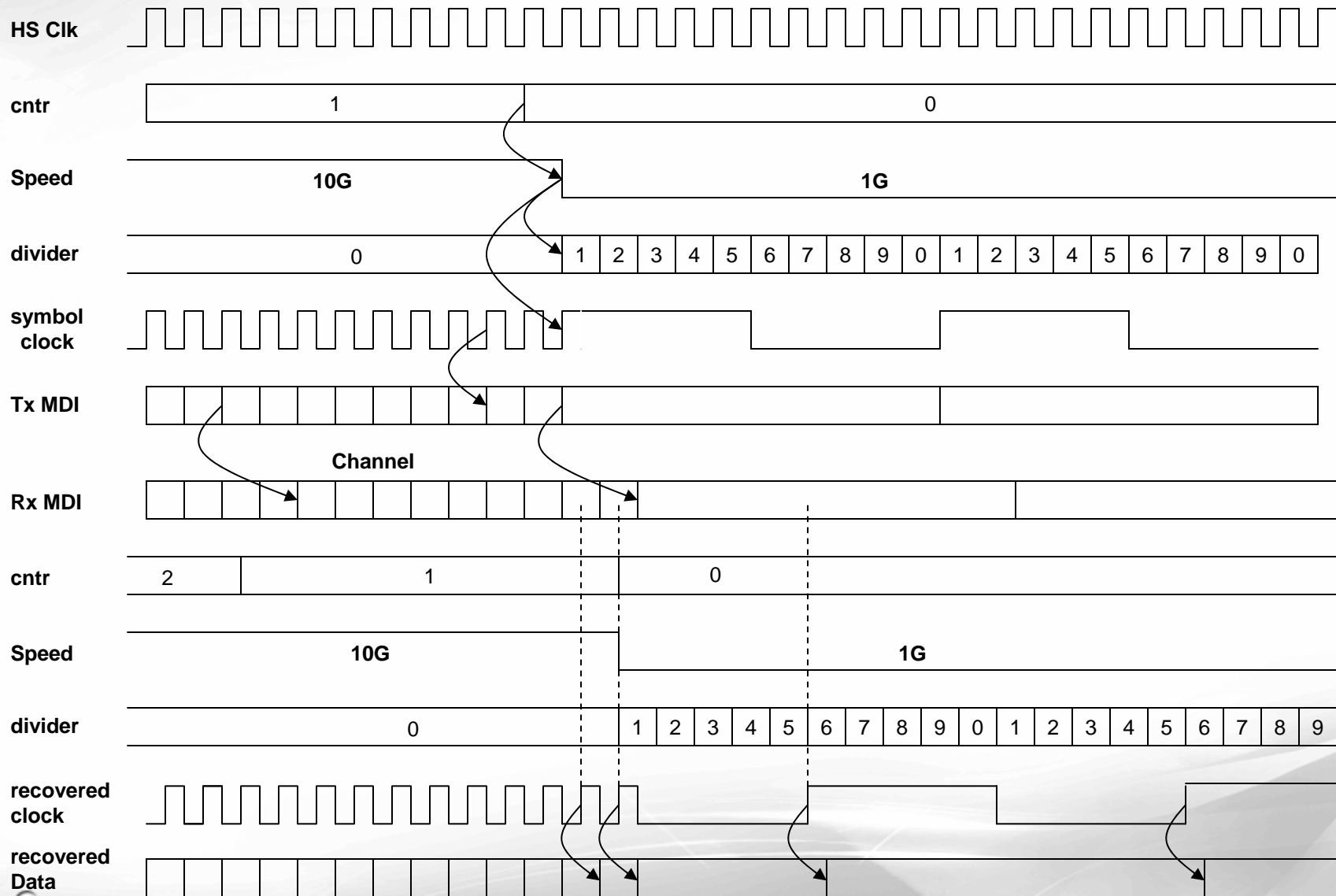
10GBASE-KR Subset Phy

- Define 1 Gigabit Rate as a Subset of 10GBASE-KR by transmitting at 1/10th rate
  - Internal clocks, transmitted symbols, etc. are 1/10th 10GBASE-KR

- Use same 64/66 endec that runs @ 1/10th the rate

- Turn down analog biases, shut off parallel circuits, etc.

- Synchronously change speed up or down

- Allows 64/66 endec to get continuous clocks so it will never loose sync!

- Auto-Negotiate SSP parameters
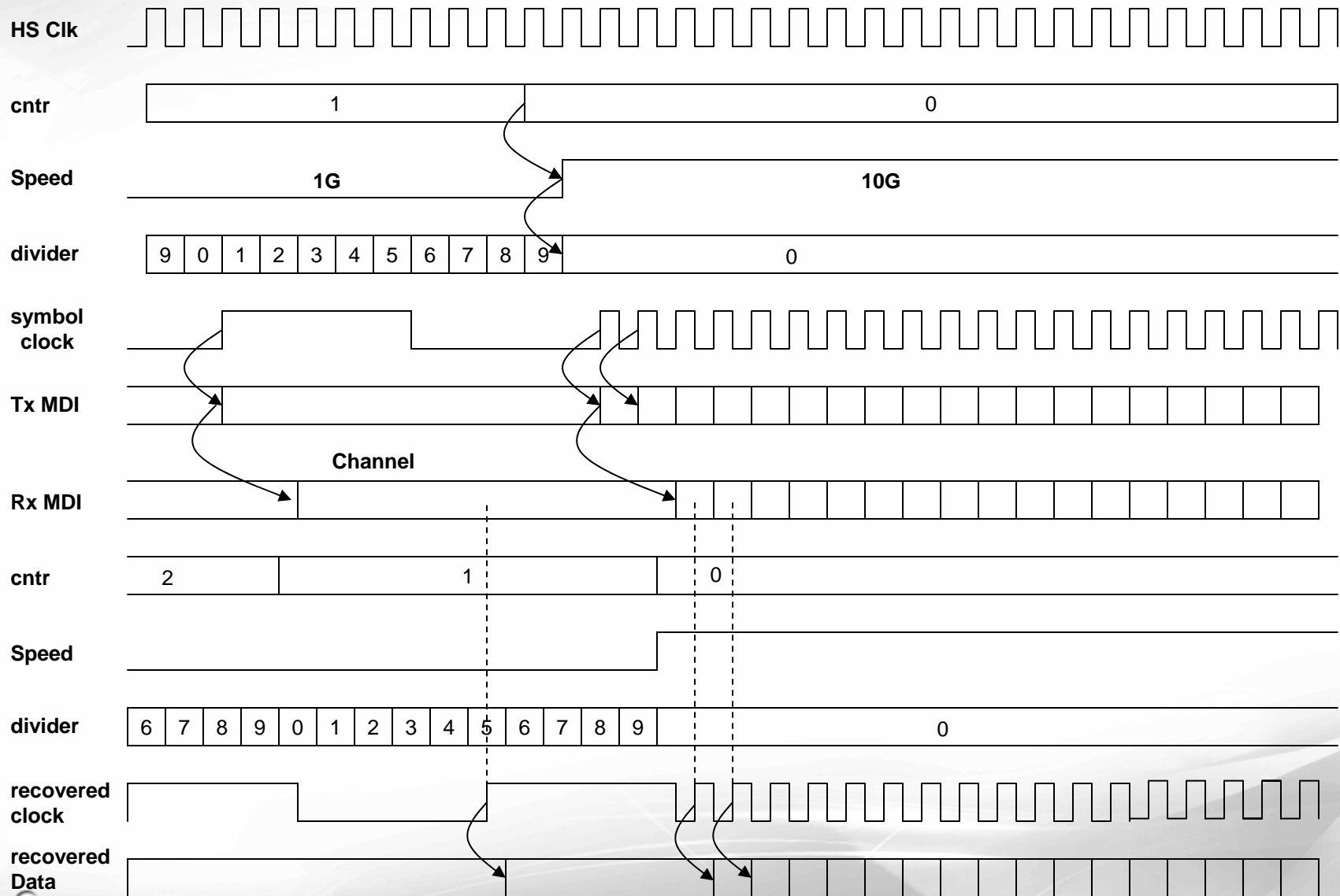
Precise Transition Communication

- Define ||Q|| to indicate the precise symbol where the speed change will occur
  - ||Q_{dn}|| = /Q/D0.0/D=down/n/, n=number >2 to be picked
  - ||Q_{up}|| = /Q/D=up/D0.0/n/, n=number >2 to be picked

- ||Q|| exchanged during IPG

MDI Data — 10GBASE-KR — Q — # Bytes down — 1000BASE-KR — Q — # Bytes up — 10GBASE-KR

Example Down Shift

Example Up Shift

HS Clk

cntr   1   0

Speed   1G   10G

divider   9 0 1 2 3 4 5 6 7 8 9   0

symbol clock

Tx MDI

Channel

Rx MDI

cntr   2   1   0

Speed

divider   6 7 8 9 0 1 2 3 4 5 6 7 8 9   0

recovered clock

recovered Data

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Observations

- ## Simple, Divide-by-10 PLL Sufficient
  - Eliminates complexity to go to another parent clock speed

- ## Allows quick, *synchronous and very precise* transitions

- ## Eliminates complexity of switching between 10G and 1G machines

- ## Simple and Limited Control Overhead
  - No changes to the wire signaling
  - Marginal addition to the control logic of a 10GBASE-KR device
    - Q-ordered sets already defined for 10GBASE-KR. Logic already there

- ## Does not require linking up at other rates to determine coefficients. Coefficients always fresh, never go stale

- ## Transition Times and Power Savings
  - A 4X or greater power savings can be achieved within ~10s of usecs transition times