Feasibility of Asymmetrical Low-Power Idle 1000Base-T

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Outlines

- Differences between 100Base-TX and 1000-BaseT on Low-Power Idle Mode
- Four pairs or one pair ?
- LPI Timing Diagram & Timer Parameters
- Issues of Phase/Coefficients Update
- Asymmetrical Operations of LPI Gphy
- Power estimations (1000Base-T PHY)
- Some Ideas
- Backup - 1000Base-TX Standard Modifications

Differences between 100Base-TX and 1000-BaseT on Low-Power Idle Mode

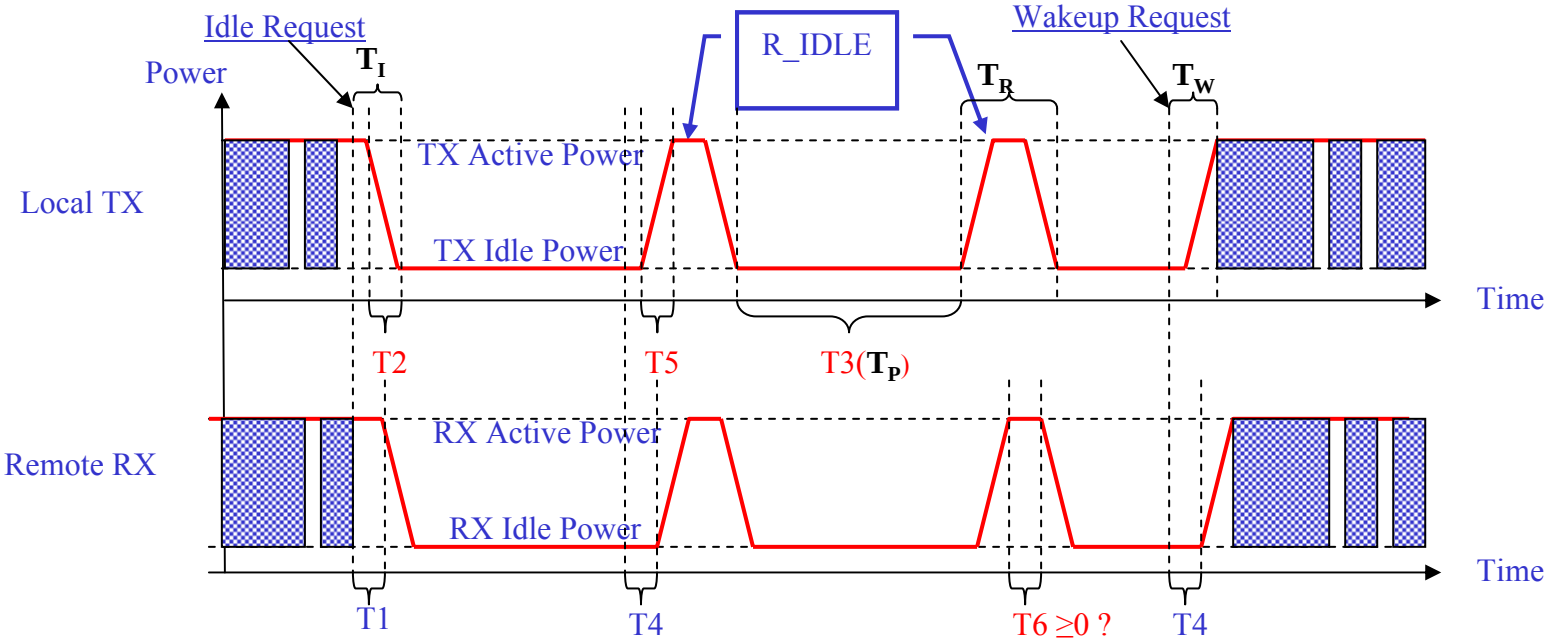
- Pair of line used
  - Gphy uses all four pairs of cable to transmit and receive signal
  - Fast Ethernet uses separate pair of line for Incoming and outgoing signal.
- Echo and Crosstalks cancellation are needed only on Gphy
- Clock Source
  - Gphy uses Loop Timing: If Master is on TX LPI state, then the clock frequency of Slave PHY may drift away from that of Master, which could cause Master to fail on synchronizing received data.
  - Fast Ethernet uses independent clock source for Local and Remote phy with ±100 ppm accuracy
- Low-Power Idle Signaling between MAC and PHY, and between Local PHY and Remote PHY are different

Four pairs or one pair ?

- Benefits to use all 4 pairs to transmit and receive R_IDLE
  - The control logic complexity is reduced. (otherwise, 1 channel needs to memorize the phase offset between channels, or to rotate the refresh channel through the 4 pairs of line.)
  - Can update Echo/NEXT coefficients during LP_IDLE mode
- Benefits to use only 1 pair to transmit and receive R_IDLE
  - Save additional power (quiescent power of LP_IDLE mode) while the other 3 pairs of TX and RX circuit can totally rest (even the signal detection and timing circuit)

  Q: Is it a must to update Echo/NEXT coeff. during LP_IDLE state?
- However, we will propose to use 4 pairs
  - Trade the logic complexity with the small amount of increase of quiescent power of LP_IDLE state (amount to be estimated)
  - If the Refresh duration vs. Refresh period is small enough, the power saving will be negligible by using only 1 pair.

LPI Timing Diagram & Parameters



Timer Parameter	100Base-TX	1000Base-T	Comment
TI (Idle delay)	< 1 us	< 1 us	
TW (Wakeup delay)	< 10 us	< 10 us	Synchronize clock only
TR (Refresh duration)	< 11 us	< 11 us or < 1 ms	Refresh phase only (<11 us) or ECHO/NEXT coef. (< 1 ms)
TP (Refresh period)	< 1 second	< 100 ms (?)	Needs more simulation data

Issues of Phase/Coefficients Update

- Clock Frequency and Phase
  - Slave clock frequency depends on the continuous incoming Master traffic. Small drift of Slave DPLL freq during Master LPI state may cause huge absolute phase accumulation.
  - Drift very slowly and depend on the implementation of Digital VCO
  - Master receiver has limited (but not none) freq/phase tracking capability and FIFO to buffer the incoming data from Slave
  - Synchronize fast during refresh and wakeup mode (< 10 us)
  - → **Determine the Refresh Period (T_P)…negotiable during AN**
- NEXT cancellers coefficients
  - Need all four pairs of line to operate at the same time to update
  - Change very slowly (> hours) and narrowly once determined
- Echo Canceller coefficients
  - Can update without the synchronous operation of other 3 pairs
  - Change very slowly (> hours) and narrowly once determined
  - Are most sensitive to the clock optimal phase
  - Have longest number of taps to update
  - → **Determine the Refresh Duration (T_R)…negotiable during AN**

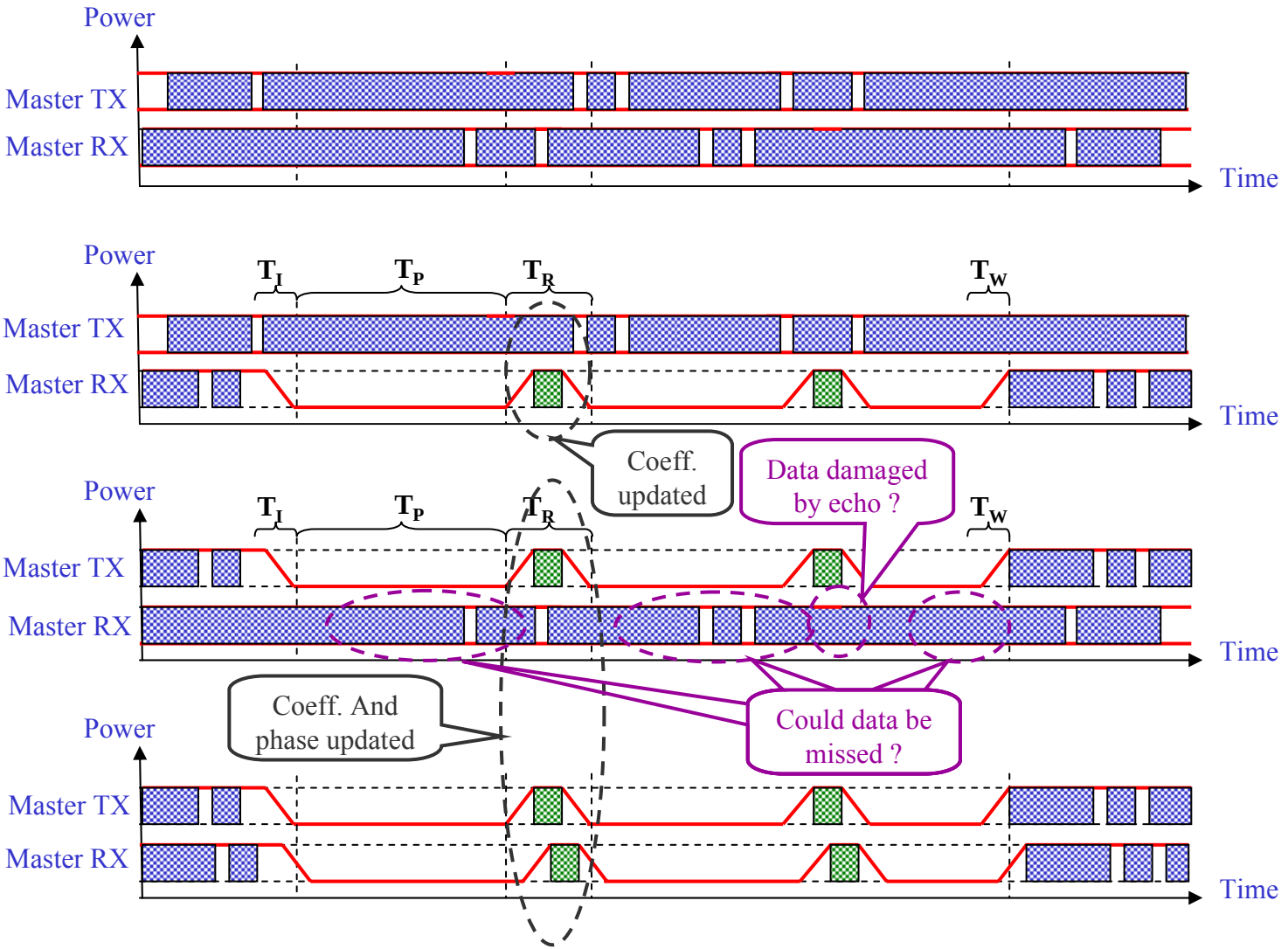
Asymmetrical Operations of LPI Gphy

Symmetrical; Both Master & Slave active
- Clock phase tracked
- No data missed
- Coefficients updated

Asymmetrical; Master Active, Slave LPI
- Clock phase tracked
- No data missed
- Coefficients updated

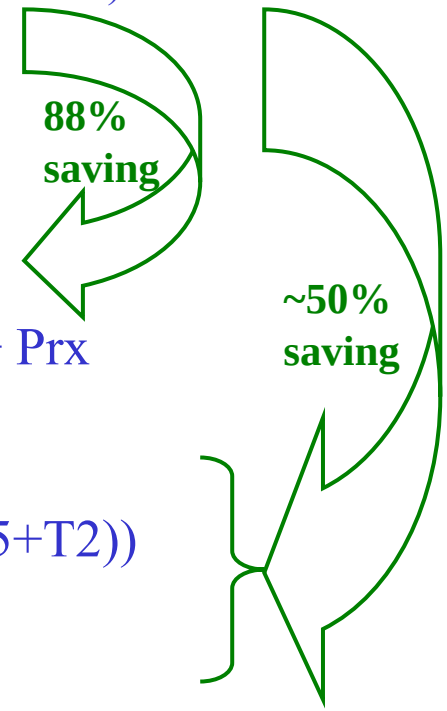
Asymmetrical; Master LPI, Slave Active
- Clock phase tracked ?
- Data could be damaged or missed
- Coefficients updated

Symmetrical; Both Master & Slave LPI
- Clock phase tracked ?
- No Data missed
- Coefficients updated



Power estimations (1000Base-T PHY)

- Power estimation is based on Realtek RTL811x's simulation data.
  - Ptx: TX active power = 229 mW
  - Prx: RX active power = 317 mW
  - Pctl: Control, and clock driver power (w/o MAC, system bus) = 74 mW
- P_full ≒ Pcontrol + Ptx + Prx = 74+229+317
  = **620 mW**
- P_LPI ≒ Pcontrol + (Ptx+Prx)*(T5+T2)/(T3+T5+T2)
  ≒ 74+(229+317)*10us/(10us+10ms)
  ≈ **74 mW** (TX and RX are in LPI)
- P_LPI_TX ≒ Pcontrol + Ptx*(T5+T2)/(T3+T5+T2) + Prx
  ≒ 74+229*10us/(10us+10ms)+317
  ≈ **391 mW** (TX is in LPI)
- P_ LPI_RX ≒ Pcontrol + Ptx + Prx*(T5+T2)/(T3+T5+T2))
  ≒ 74+229+317*10us/(10us+10ms)
  ≈ **303 mW** (RX is in LPI)



- P_MAC(TX) ≒ **38 mW**; P_MAC(RX) ≒ **53 mW**

Some Ideas

1. LAN traffic between terminals and end switch are Asymmetrical most of the time
2. Asymmetrical LPI mode should be allowed and the capability can be advertised in AN pages
3. The R_IDLE of slave device need to synchronize with R_IDLE of master only if both are in LPI mode
4. Refresh Duration (T_R)
   - Negotiable during AN; Implementation dependent
   - Always keeps 0.5~1 ms to update both clock phase & coeff.
   - Or, keeps <10 us to Synchronize clock Phase only; once a while (say 1 min.) prolong to 1ms with different R_IDLE signal to update coefficients (save more power)
5. Refresh Period (T_P)
   - Negotiable during AN; Implementation dependent
   - May vary depending on Maser/Slave LPI mode

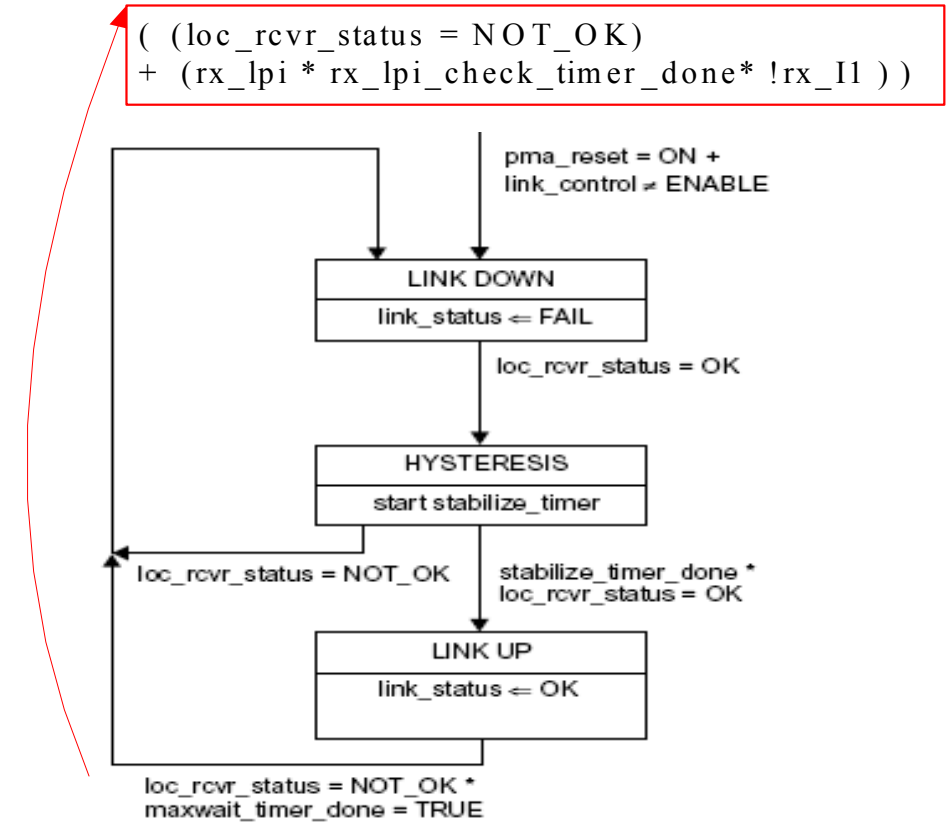
Questions?

Thank you

Backup

1000Base-T Standard Modification
Link Monitor FSM

- rx_lps_check_timer > T3+ T4
- When RX is in LPI, if RX does not receive I1 in rx_lpi_check_timer, it will be re-link.



NOTES
1—maxwait_timer is started in PHY Control state diagram (see Figure 40-14).
2—The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28-16).

Figure 40–16—Link Monitor state diagram

1000Base-T Standard Modification
PCS TX FSM

- Add

TX I1 N times state

TX train state

(IDLE +I1)

- tx_I1_cnt =25
  => 8ns*25=0.2us
- tx_train_timer = 9.8us

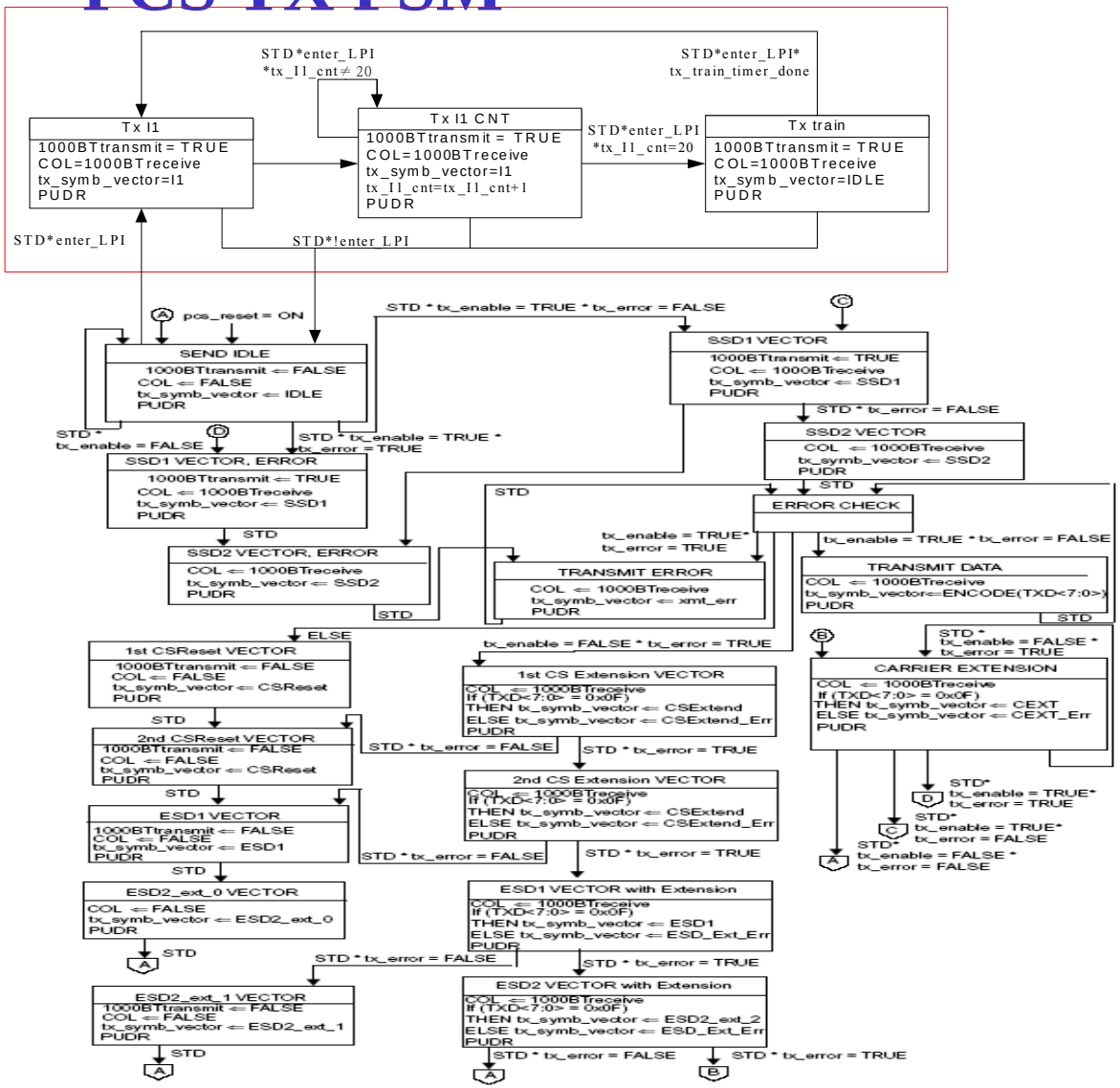


Figure 40–9—PCS Transmit state diagram

1000Base-T Standard Modification
PCS RX FSM

- Add

  Rx I1 state

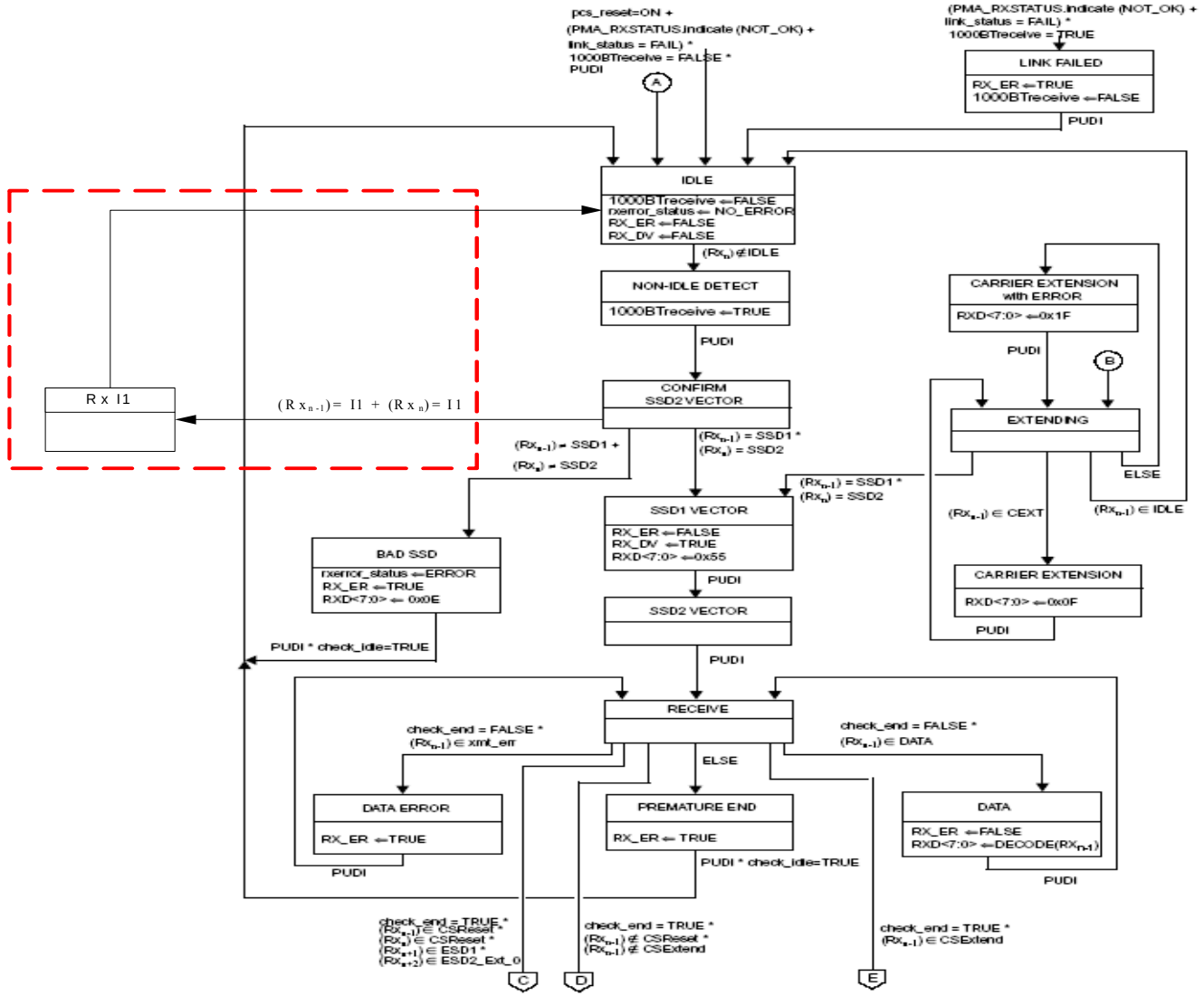


Figure 40–10a—PCS Receive state diagram, part a