SOLARFLARE Communications

EEE Synchronization

1/14/2009 Gavin Parnaby

New Orleans

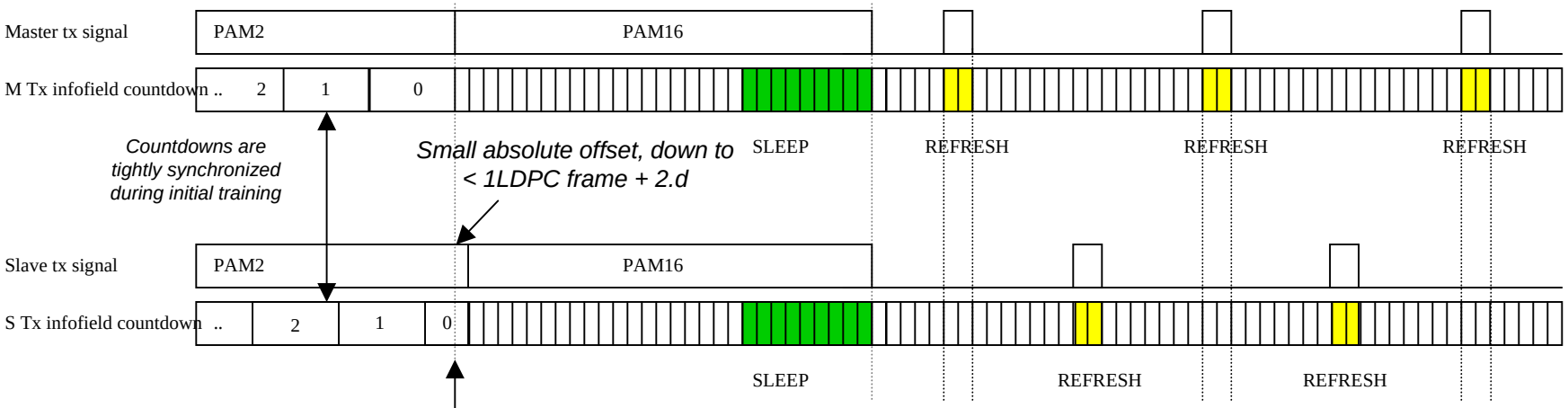
Agenda

- Need specific text in 55.3.5.1 to describe the slave's actions during PAM2 to PAM16 transition
- Current text: 'When the PHYs both support the EEE capability, the slave is responsible for initializing its own transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master's transition to PCS_Test, measured at the slave's MDI on pair A.'
- Needs more detail on how the slave initializes its transition counter

PAM2 to PAM16 transition at slave

- Slave performs transition to PAM16 within 1 LDPC frame of master
- Master knows rx signal will transition to PAM16 within 2 link delays + 1 LDPC frame of the master's transition [<5 LDPC frames at all lengths]
- Master receives a complete frame of PAM-16 and starts rx LDPC frame counter.
- Master uses resulting index to generate refresh_active and active_pair signals

Slave timing diagram



New requirement: Slave is required to synchronize transition to data-mode / PAM-16 with the master's transition
[The 802.3an requirement is within 1ms]
This guarantees that the transmit and receive LDPC frame counters are synchronized to within 1 LDPC frame + d on the master side.

The slave must initialize its transition counter so that it transitions to PAM16 during the slave's PHY frame 0.
Slave may transition to PAM16 at any time within PHY frame 0.
Therefore the slave's final PHY frame is not guaranteed to be a complete frame (indeed, it is unlikely it is a complete frame).

Quiet/refresh control generated as previously described using appropriate LDPC frame counter

Text

- Add to 55.3.5.1, page 161, line 51

  ‘When the PHYs both support the EEE capability, the slave PHY is responsible for initializing its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY’s transition to PCS_Test, measured at the slave PHY’s MDI on pair A. The slave PHY shall initialize its transition counter so that the slave PHY’s transition to PCS_Test occurs during the PHY frame when the slave PHY’s transition counter = 0. The master PHY is responsible for detecting the slave PHY’s transition to PAM16. The master PHY counts the slave PHY’s LDPC frames from this point and uses this counter to generate the rx_refresh_active and rx_active_pair signals appropriately.’