45. Management Data Input/Output (MDIO) Interface

Insert 45.2.1.76a after 45.2.1.76 (as renumbered by IEEE Std 802.3av™-2009):

45.2.1.76a 10GBASE-T fast retrain status and control register (Register 1.147)

Table 45–53a—10GBASE-T fast retrain status and control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.147.15:11	LP fast retrain count	Counts the number of fast retrains requested by the link partner	RO/NR
1.147.10:6	LD fast retrain count	Counts the number of fast retrains requested by the local device	RO/NR
1.147.5	Reserved	Ignore on read	RO
1.147.4	Fast retrain ability	1 = Fast retrain capability is supported 0 = Fast retrain capability is not supported	RO
1.147.3	Fast retrain negotiated	1 = Fast retrain capability was negotiated 0 = Fast retrain capability was not negotiated	RO
1.147.2:1	Fast retrain signal type	11 = Reserved 10 = PHY signals Link Interruption during fast retrain 01 = PHY signals Local Fault during fast retrain 00 = PHY signals IDLE during fast retrain	R/W
1.147.0	Fast retrain enable	1 = Fast retrain capability is enabled 0 = Fast retrain capability is disabled	R/W

[a] RO = Read only, R/W = Read/Write, NR = Non Roll-over

45.2.1.76a.1 LP fast retrain count (1.147.15:11)

These bits map to fr_rx_counter as defined in 55.4.5.1. The counter is a 5-bit count of the number of 10GBASE-T fast retrains requested by the link partner. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.76a.2 LD fast retrain count (1.147.10:6)

These bits map to fr_tx_counter as defined in 55.4.5.1. The counter is a 5-bit count of the number of 10GBASE-T fast retrains requested by the local device. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.76a.3 Fast retrain ability (1.147.4)

When read as a one, bit 1.147.4 indicates that the PHY supports fast retrain, as defined in 55.4.2.5.15. When read as a zero, bit 1.147.4 indicates that the PHY does not support fast retrain.

45.2.1.76a.4 Fast retrain negotiated (1.147.3)

When read as a one, bit 1.147.3 indicates that the PHY negotiated fast retrain, as defined in 55.4.5.1 during the most recent autonegotiation. When read as a zero, bit 1.147.3 indicates that the PHY did not negotiate fast retrain. See 45.2.7.10.5a.

45.2.1.76a.5 Fast retrain signal type (1.147.2:1)

For PHYs that support fast retrain, these bits map to fr_sigtype as defined in 55.3.5.2.2. When Fast retrain signal type is set to 00, the PMA sends IDLE characters on the receive path during fast retrain. When Fast retrain signal type is set to 01, the PMA sends Local Fault on the receive path during fast retrain. When Fast retrain signal type is set to 10, the PMA sends Link Interruption on the receive path during fast retrain.

45.2.1.76a.6 Fast retrain enable (1.147.0)

For PHYs that support fast retrain, this bit controls fr_enable as defined in 55.4.5.1. When PMA reset is executed, this bit is set to one.

Note: Setting this bit to zero while a link is up will cause the PHY to stop supporting fast retrain and the link will drop if the link partner initiates a fast retrain.