46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII))

Change 46.1.7.3 for carrier indication definition:

46.1.7.3 Mapping of PLS_CARRIER.indication

10 Gb/s operation supports full duplex operation only. The RS never generates this primitive for PHYs that do not support EEE or Link Interruption.

For PHYs that support EEE capability, CARRIER_STATUS is set in response to LPI_INDICATION as shown in Figure 46–10a. For PHYs that support Link Interruption, CARRIER_STATUS may be set in response to link_fault. CARRIER_STATUS is set to CARRIER_ON if LPI_CARRIER_STATUS is TRUE or if link_fault is Link Interruption. CARRIER_STATUS is otherwise set to CARRIER_OFF.

Change 46.3.4 as follows:

46.3.4 Link fault signaling

Link fault signaling operates between the remote RS and the local RS. Faults detected between the remote RS and the local RS are received by the local RS as Local Fault. Only an RS originates Remote Fault signals.

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data or LPI, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault or Link Interruption status is received by an RS, the RS stops sending MAC data or LPI, and continuously generates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data or LPI.

Status is signaled in a four byte Sequence ordered_set as shown in Table 46–5. The PHY indicates Local Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x01 in lane 3. The RS indicates a Remote Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x02 in lane 3. Though most fault detection is on the receive data path of a PHY, in some specific sublayers, faults can be detected on the transmit side of the PHY. This is also indicated by the PHY with a Local Fault status.

For operation with links that may be temporarily interrupted, optional detection of a third fault condition, Link Interruption, is provided. Link Interruption is indicated by the PHY receive function by continuously sending the Link Interruption ordered_set as defined in Table 46-5.

Table 46–5—Sequence ordered_sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	0x00	0x00	0x03	Link Interruption
Sequence	≥ 0x00	≥ 0x00	≥ 0x03~~3~~4	Reserved
NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications				

The RS reports the fault status of the link. Local Fault indicates a fault detected on the receive data path between the remote RS and the local RS. Remote Fault indicates a fault on the transmit path between the local RS and the remote RS. The RS shall implement the link fault signaling state diagram (see Figure 46–10a).

Change 46.3.4.2 as follows:

The link fault signaling state diagram uses the following variables and counters:

col_cnt
: A count of the number of columns received not containing a fault_sequence. This counter increments at RX_CLK rate (on both the rising and falling clock transitions) unless reset.

fault_sequence
: A new column received on RXC<3:0> and RXD<31:0> comprising a Sequence ordered_set of four bytes and consisting of a Sequence control character in lane 0 and a seq_type in lanes 1, 2, and 3 indicating either Local Fault~~, or~~ Remote Fault or Link Interruption.

last_seq_type
: The seq_type of the previous Sequence ordered_set received
  Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
  Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
  Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

link_fault
: An indicator of the fault status.
  Values: OK; No fault.
  Local Fault; fault detected by the PHY.
  Remote Fault; fault detection signaled by the remote RS.
  Link Interruption; link temporarily unavailable, signaled by the PHY.

reset
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
  Values: FALSE: The device is completely powered and has not been reset (default).
  TRUE: The device has not been completely powered or has been reset.

seq_cnt
: A count of the number of received Sequence ordered_sets of the same type.

seq_type

The value received in the current Sequence ordered_set

Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

Change the last two paragraphs of 46.3.4.3 as follows:

The variable link_fault is set to OK following any interval of 128 columns not containing a Remote Fault, ~~or~~ Local Fault or Link Interruption Sequence ordered_set.

The RS output onto TXC<3:0> and TXD<31:0> is controlled by the variable link_fault.

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.
b) link_fault = Local Fault or link_fault = Link Interruption
The RS shall continuously generate Remote Fault Sequence ordered_sets.
c) link_fault = Remote Fault
The RS shall continuously generate Idle control characters.

Insert a new section, 46.3a before 46.4:

46.3a.2.1 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

LPI_CARRIER_STATUS

The LPI_CARRIER_STATUS variable indicates how the CARRIER_STATUS parameter is controlled by the LPI_REQUEST parameter. The LPI_CARRIER_STATUS is either TRUE or FALSE as determined by the Transmit LPI state diagram in Figure 46-10a.

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values:FALSE: The device is completely powered (default).
TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.

Values:FALSE: Do not reset the RS (default).
TRUE: Reset the RS.

tw_timer

A timer that counts, in microseconds, the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If DTE XS XAUI stop enable bit is asserted (5.0.9), the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx}$ - $T_{w\_sys\_rx}$ for the XGXS as shown in Table 78-4.

The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

46.3a.2.2 State Diagram

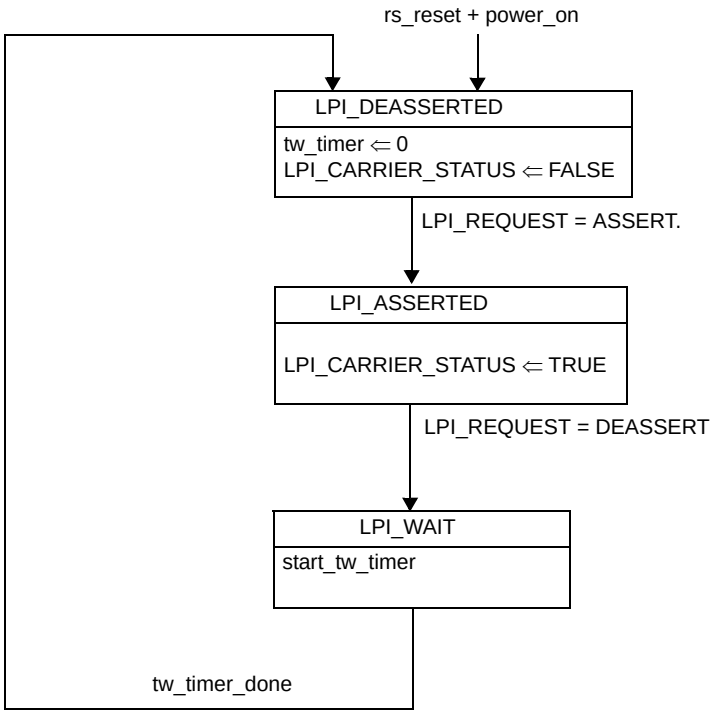

Figure 46–10a—Transmit LPI State Diagram

46.3a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

46.3a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the XGMII. The receive system should be aware that data frames may arrive at the XGMII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

If the PHY XS XAUI stop enable bit (4.0.9) is asserted, the PHY XS may stop signaling on the XAUI in the receive direction to conserve energy. The receiver should negotiate an additional 9.5 μs for the remote Tw_sys (equal to Tw_sys_tx - Tw_sys_rx for the XGXS as shown in Table 78–4) before setting the PHY XS XAUI stop enable bit.

46.5 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[1]

Insert the following row into table 46.5.2.3:

46.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LPI	Implementation of LPI	46.1.7		O	Yes [ ] No [ ]

Insert the new subclauses 46.5.3.3a and 46.5.3.3b after 46.5.3.3:

46.5.3.3a LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	46.3.1.2	As defined in Table 46–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI in Rx direction	46.3.2.2	As defined in Table 46–4	LPI:M	Yes [ ] N/A [ ]
*L3	TX_CLK stoppable during LPI	46.3.1.5	At least 128 cycles after LPI assertion	LPI:O	Yes [ ] No [ ]
L4	TX_CLK restart before LPI deassert	46.3.1.5	At least 1 positive edge before LPI deassertion	L3:M	Yes [ ] N/A [ ]
L5	RX_CLK stoppable during LPI	46.3.2.4		LPI:O	Yes [ ] No [ ]

46.5.3.3b Link Interruption

Item	Feature	Subclause	Value/Comment	Status	Support
LINT	Detection of Link Interruption	46.3.4		O	Yes [ ] No [ ]
LINT1	CARRIER_STATUS response to Link Interruption	46.1.7.3	Set to CARRIER_ON if link_fault is Link Interruption	LINT:O	Yes [ ] No [ ]

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