Low-Power Idle based EEE 100Base-TX

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IEEE 802.3az Task Force

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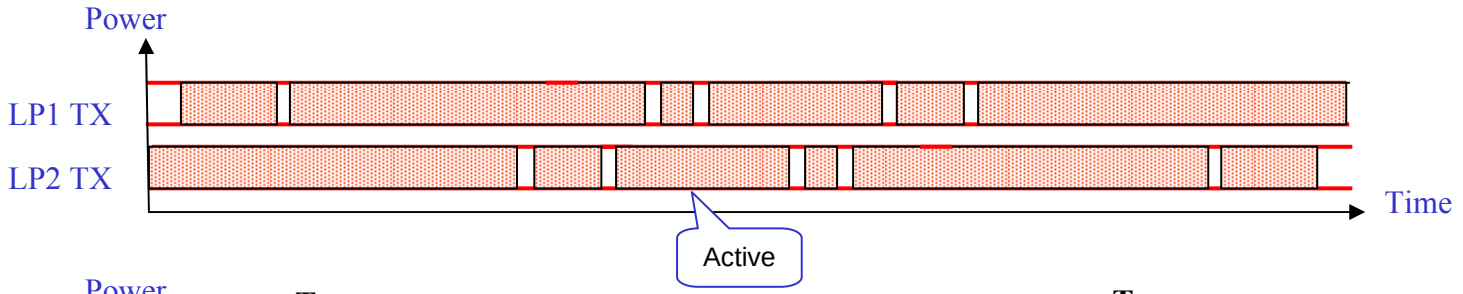
Outlines

Revised version of chou_01_0108

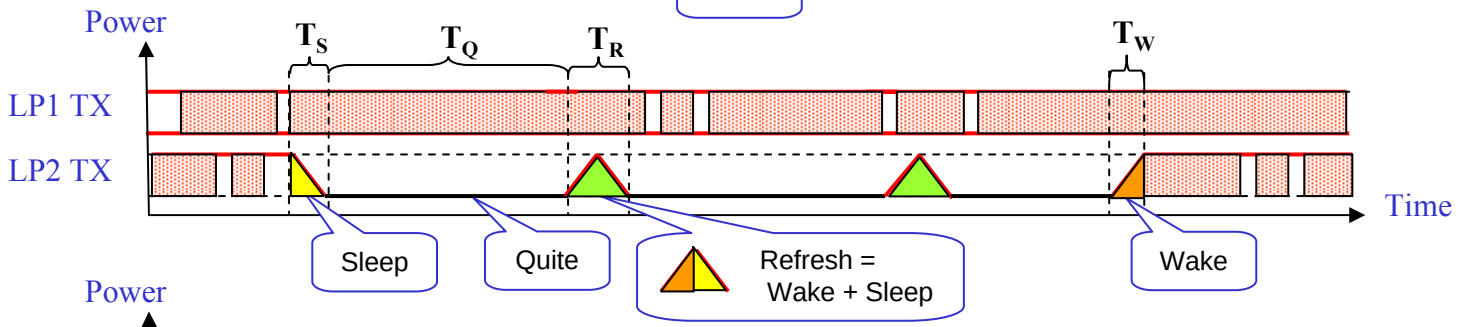
- Line States of EEE FE PHY (new)
- EEE FE Fully Asymmetric Operations (new)
- LPI Line State Transition Diagrams (revised)
  - Sleep State
  - Wake State
  - Refresh State
- LPI State Diagrams (revised)
  - LPI Line State Diagrams (PHY)
  - LPI Operating State Diagrams (MAC)
- Simulation result of LPI Transition
- Single Ethernet PHY Block Diagram
- Estimation of Power Consumptions
- Signals between two EEE enabled FE parties
  - Signals between MAC and PHY (MII)
  - Signals between PHYs

Line States of EEE FE PHY

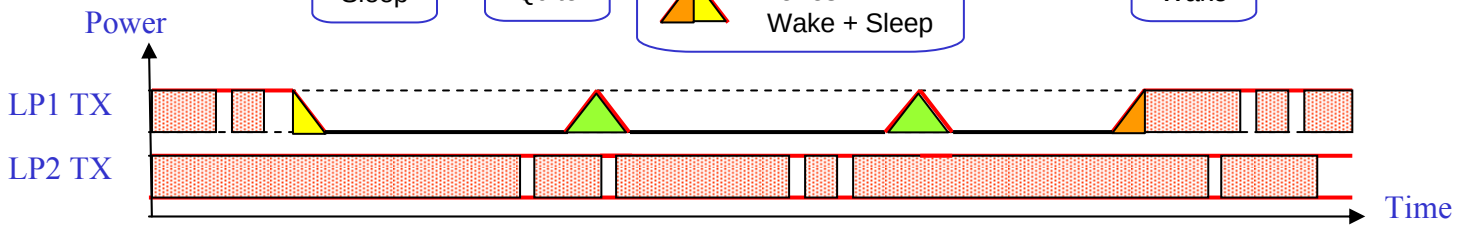
Case 1. Symmetrical; Both Master & Slave Active



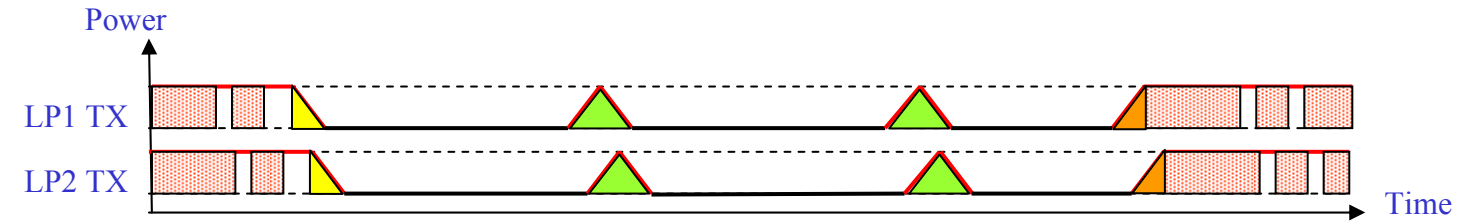
Case 2. Asymmetrical; LP1 Active, LP2 Low-Power



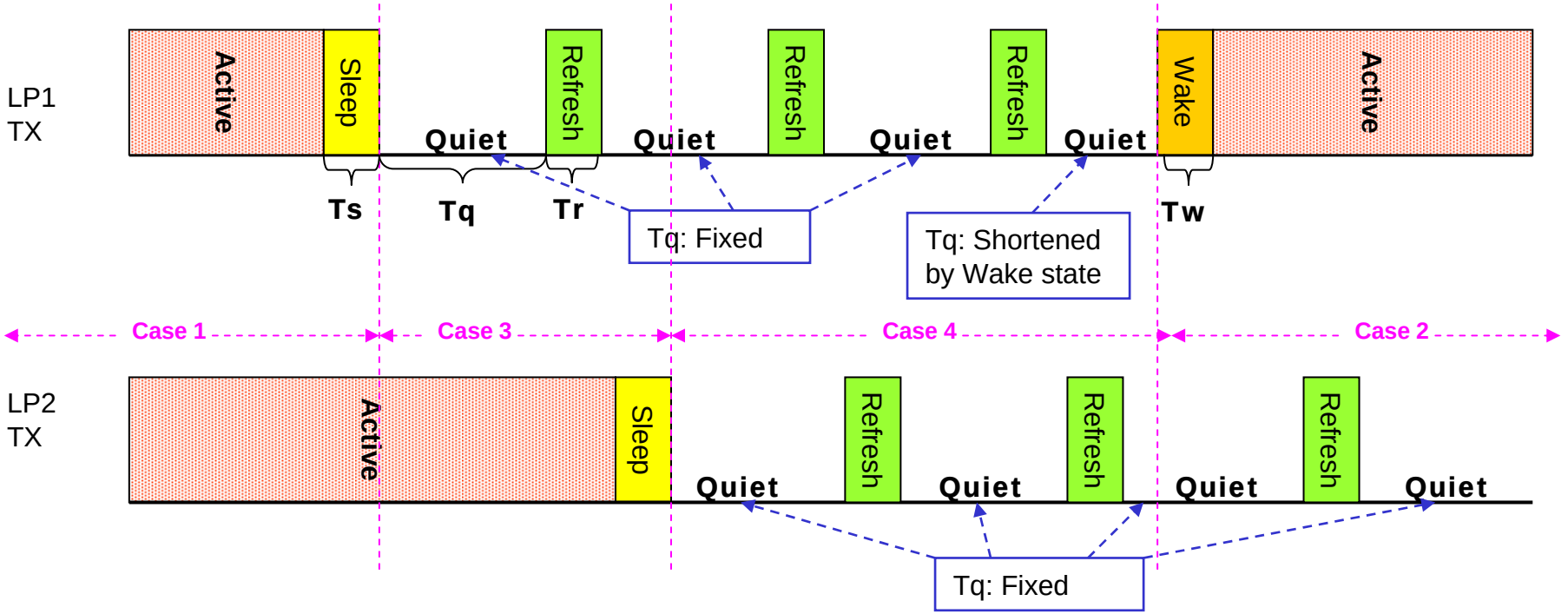
Case 3. Asymmetrical; LP1 Low-Power, LP2 Active



Case 4. Symmetrical; Both parties are Low-Power

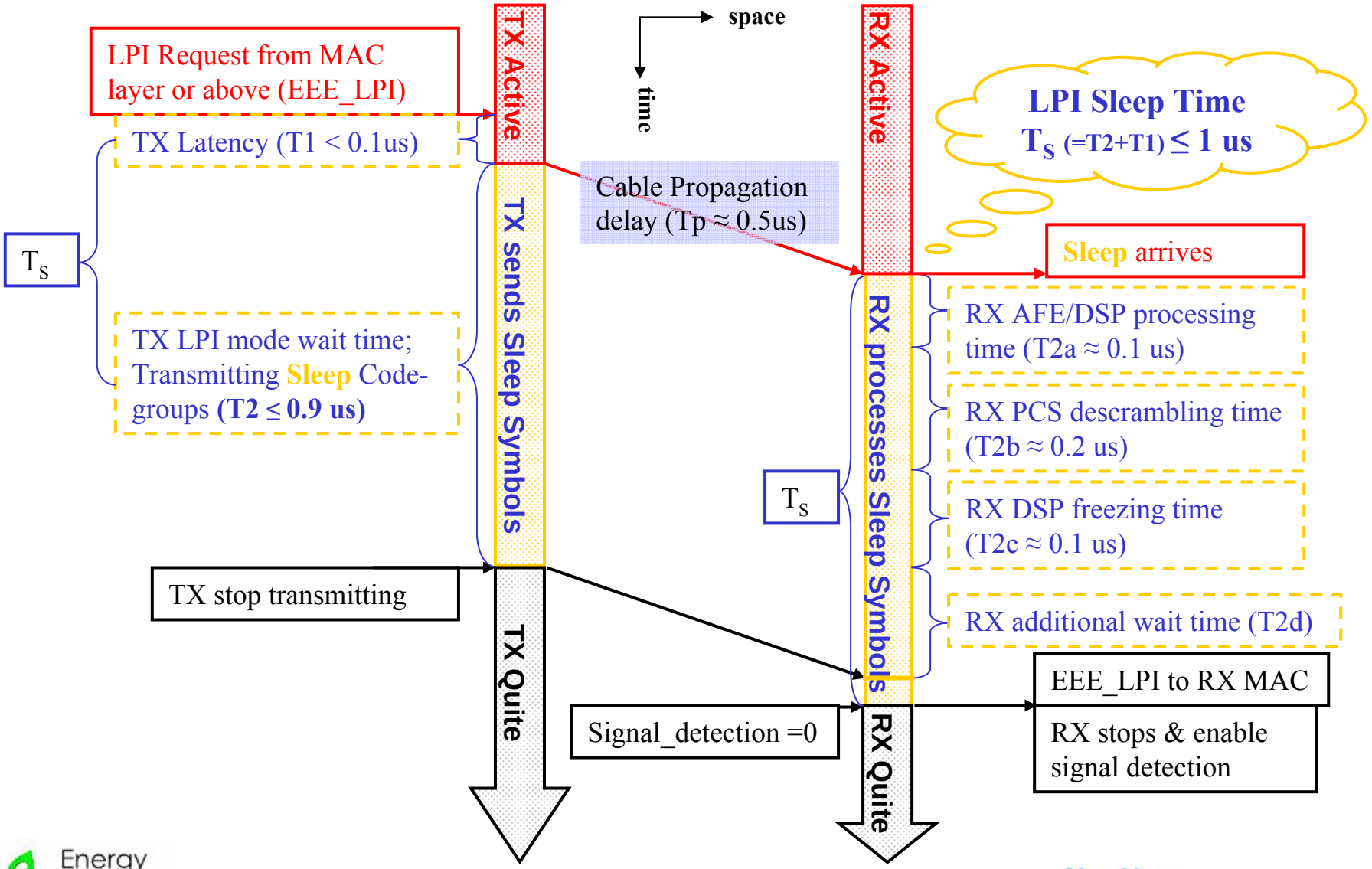


EEE FE Fully Asymmetric Operations

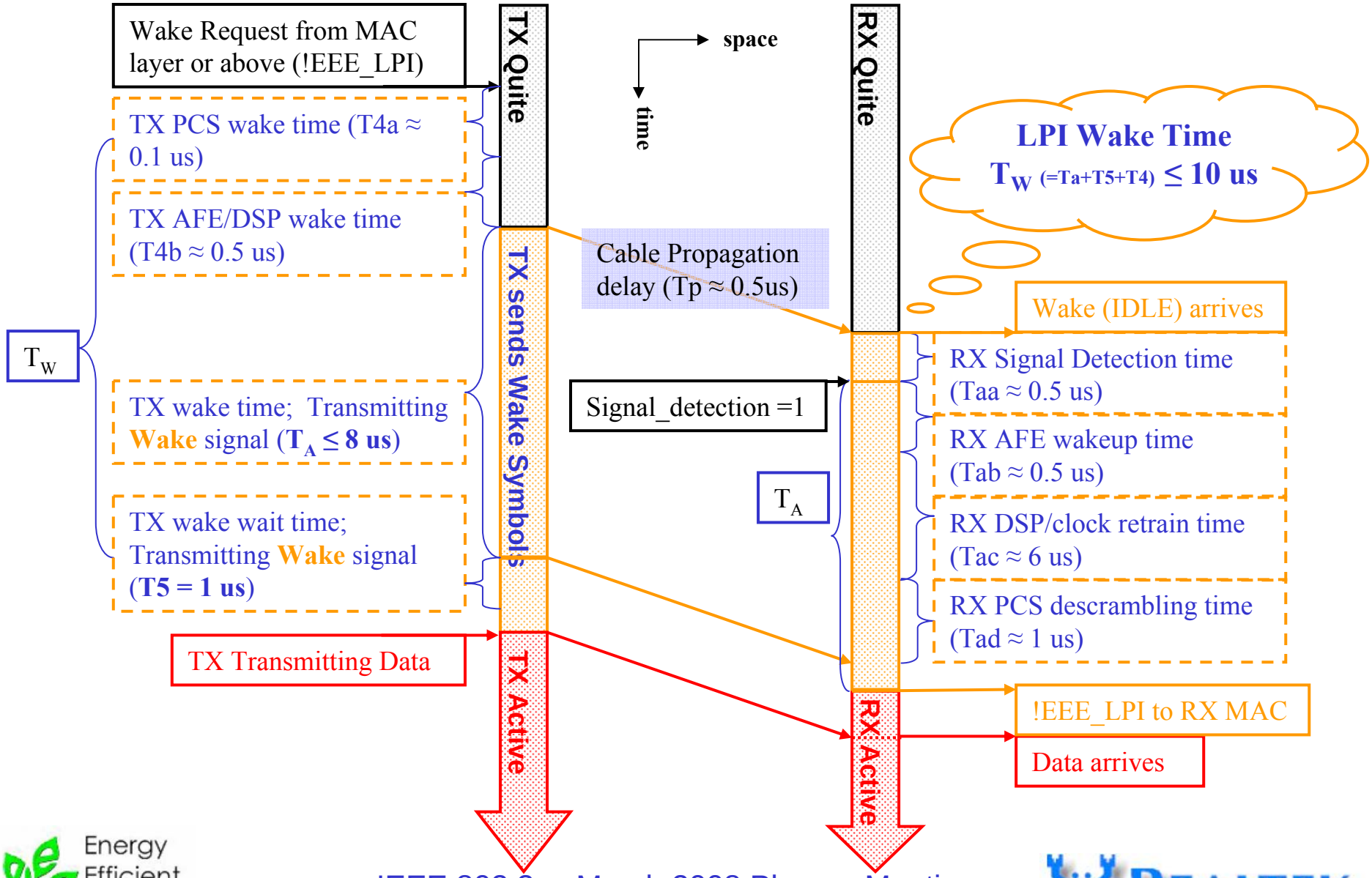


Line State	Timing Parameter (suggested)	Signal (suggested)
Sleep	Ts = 1us	New 4B5B code-group
Quite	Tq =10 - 100ms	Electric differential DC 0V
Wake	Tw = 10us (T_A=8us internal)	Existing IDLE code-group
Refresh	Tr = 10us	Wake + Sleep

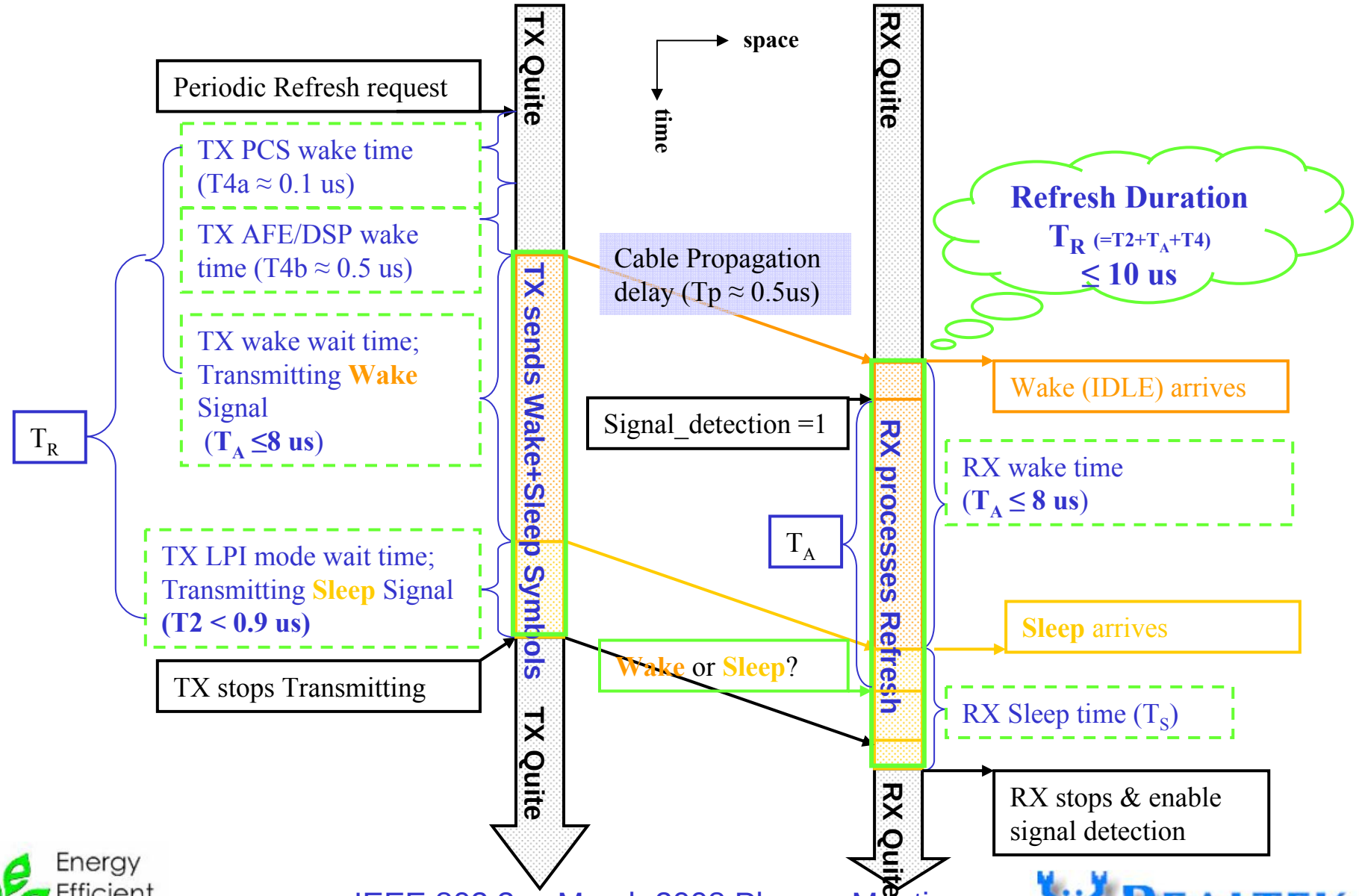
LPI Transition Diagram (Sleep)



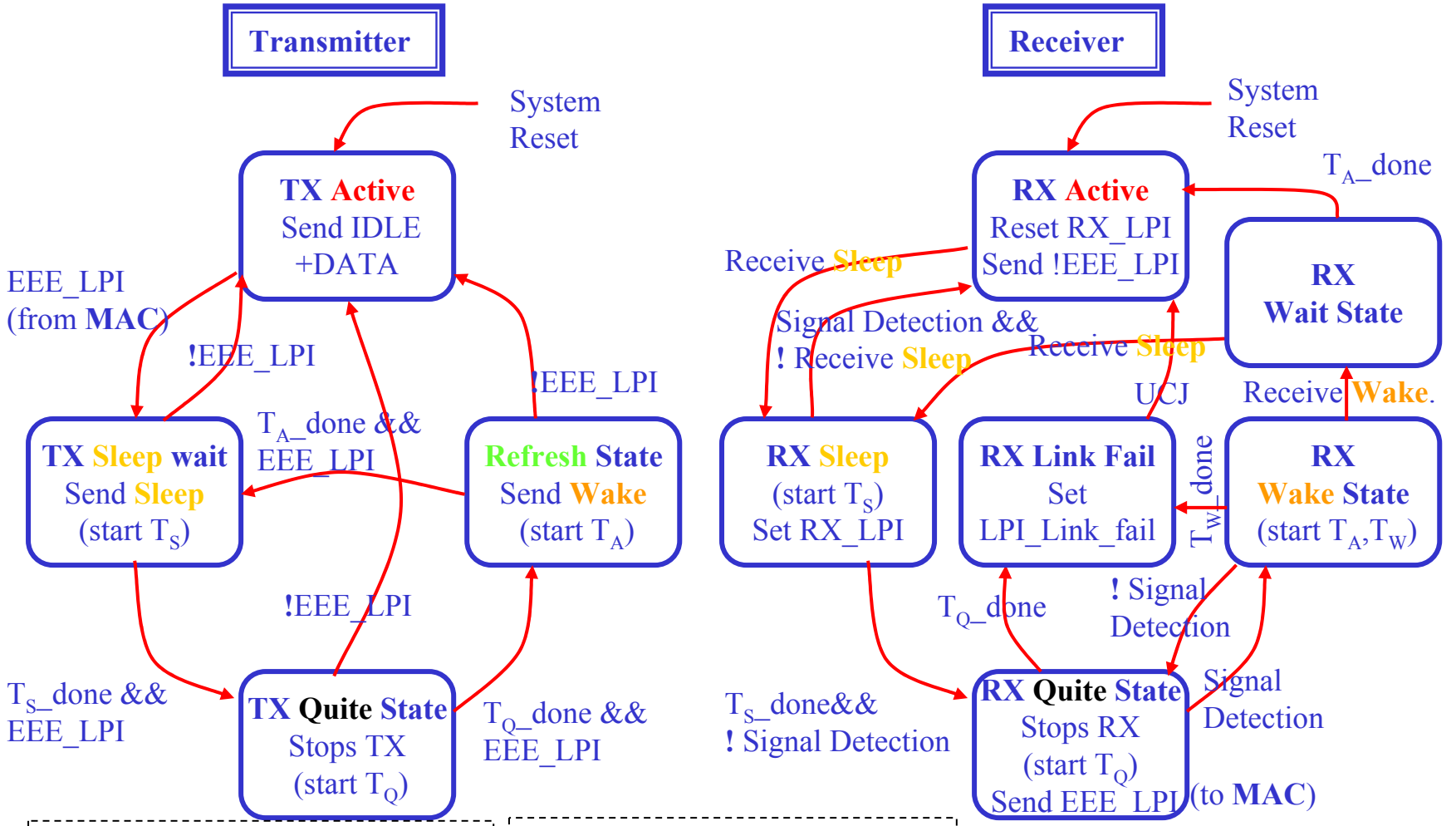
LPI Transition Diagram (Wake)



LPI Transition Diagram (Refresh)



LPI Line State Diagrams (PHY)

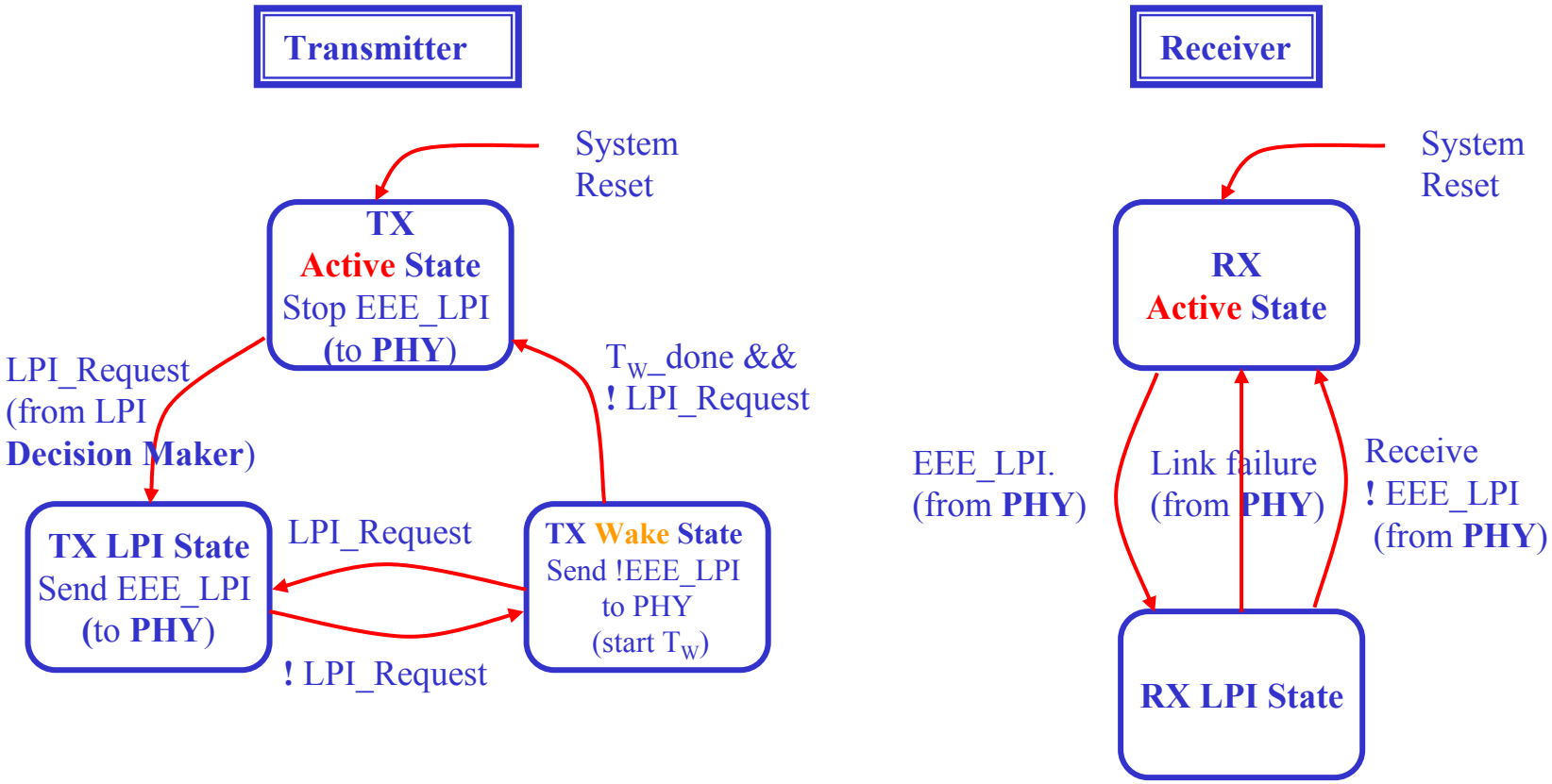


Note: Addition to Figure 24-8 Transmitter state diagram

Note: RX_LPI, LPI_Link_fail, new signals for Figure 24-15 Link_monitor State Diagram

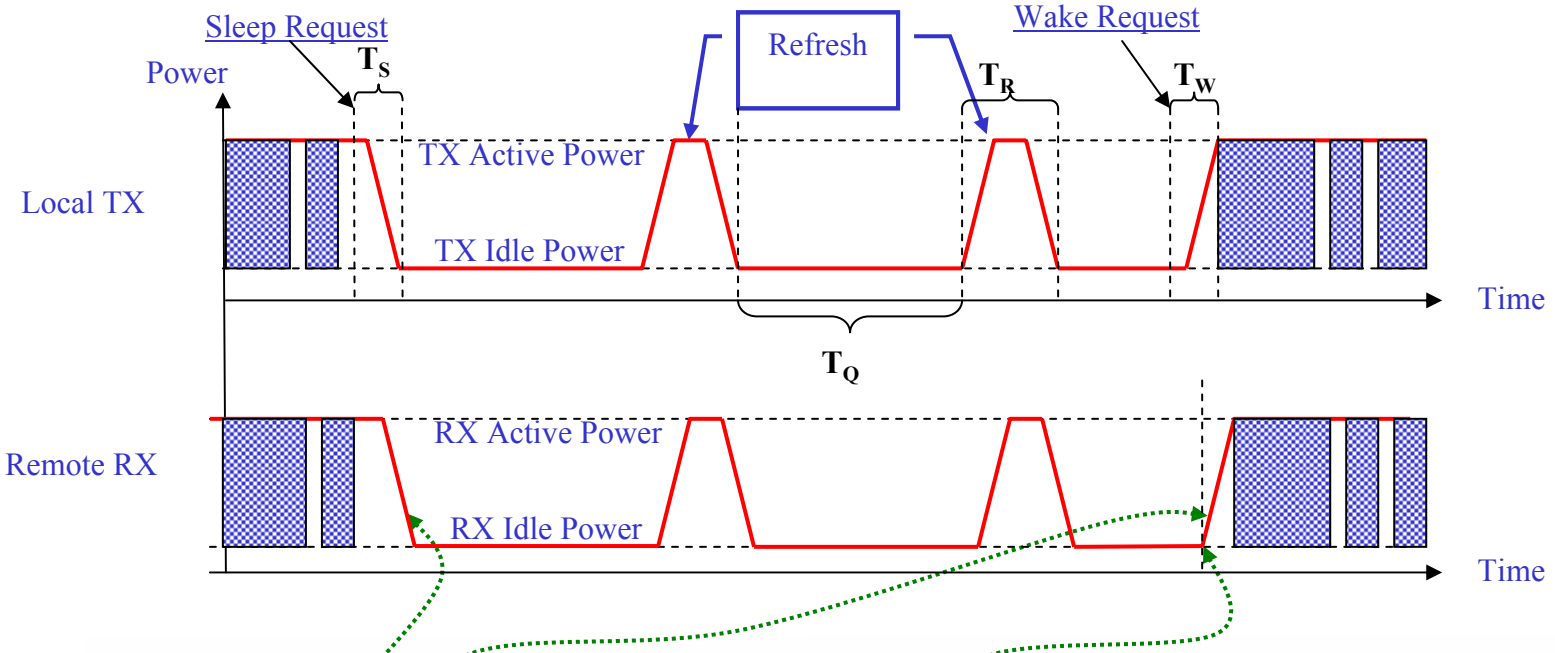
Note: Addition to Figure 24-11 Receiver state diagram

LPI Operating State Diagrams (MAC)

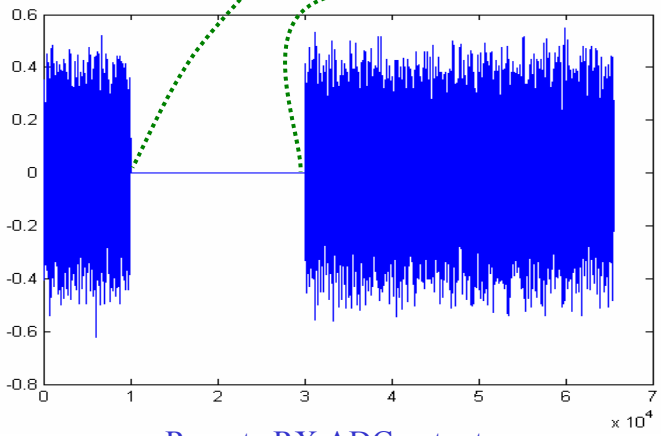


Note: New EEE state diagrams

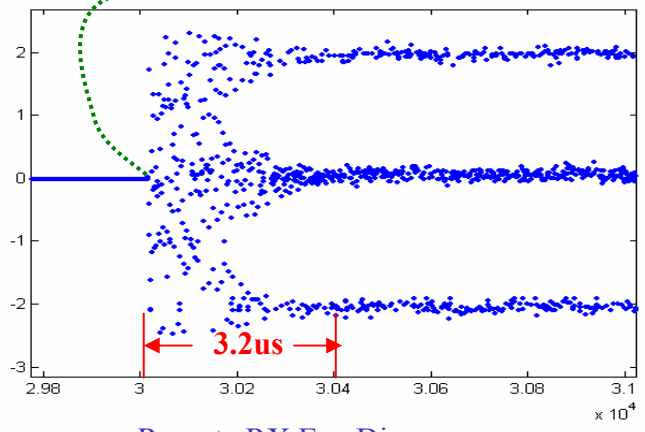
Simulation Result of LPI Transition



Note: Local and Remote Frequency offset = 600ppm & **opposite clock phase**
Timing Loop starts from scratch. (w.c.)



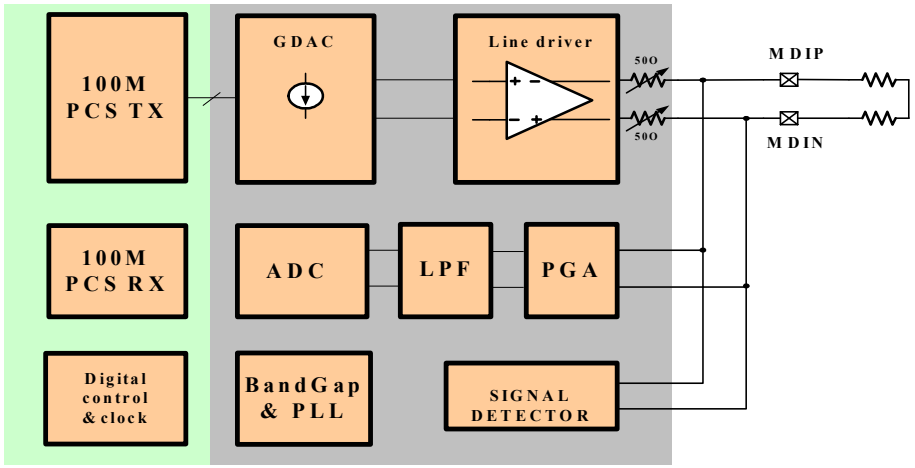
Remote RX ADC output



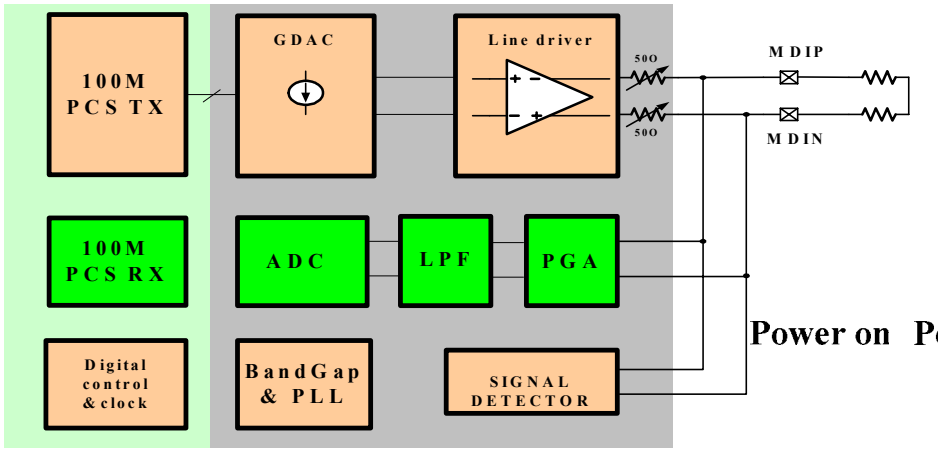
Remote RX Eye Diagram

Single Ethernet FE PHY Block Diagram

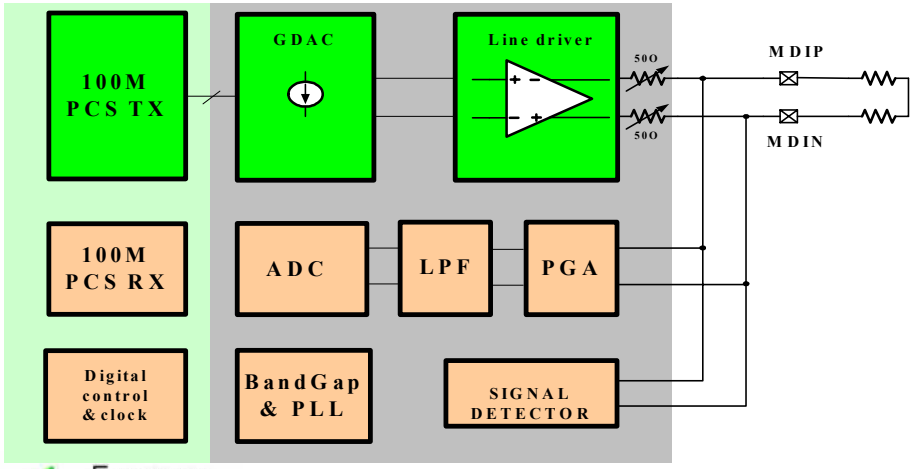
Fully Active (Case 1)



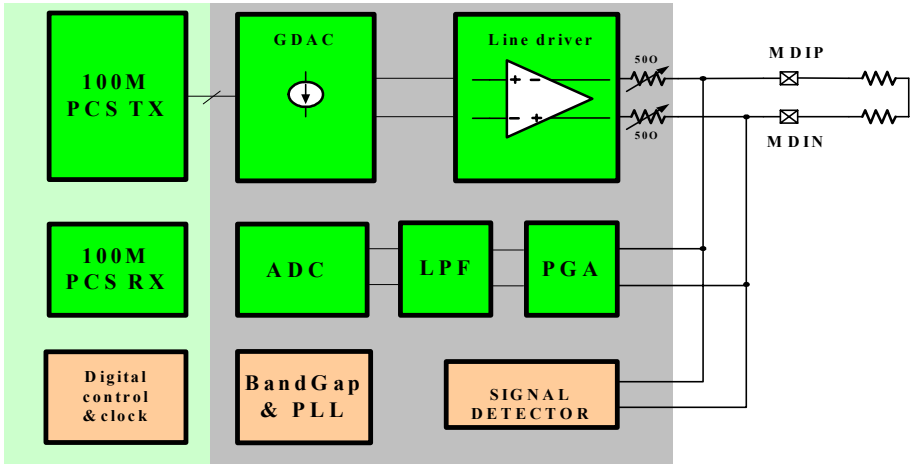
RX LPI (Case 2)



TX LPI (Case 3)



Fully LPI (Case 4)



Power estimations (100Base-TX PHY)

- Power estimation is based on Realtek RTL811x's simulation data.
  - Ptx: TX active power = 64 mW
  - Prx: RX active power = 125 mW
  - Pcontrol: Control, and clock driver power (w/o MAC, system bus) = 60 mW
- Fully Active (Case 1) ＝Pcontrol + Ptx + Prx＝60+64+125
  ＝**249 mW**
- RX LPI (Case 2) ≒Pcontrol + Ptx + Prx*(Tr)/(Tr+Tq))
  ≒60+64+125*11us/(11us+100ms)
  ≈ **124 mW** (RX in LPI)
- TX LPI (Case 3) ≒Pcontrol + Ptx*(Tr)/(Tq+Tq) + Prx
  ≒60+64*11us/(11us+100ms)+125
  ≈ **185 mW** (TX in LPI)
- Fully LPI (Case 4) ≒Pcontrol + (Ptx+Prx)*(Tr)/(Tr+Tq)
  ≒60+(64+125)*11us/(11us+100ms)
  ≈ **60 mW** (Both TX and RX in LPI)

- Additional Power: P_MAC(TX) ≒**29 mW**; P_MAC(RX) ≒**43 mW**

Signals between two EEE FE parties

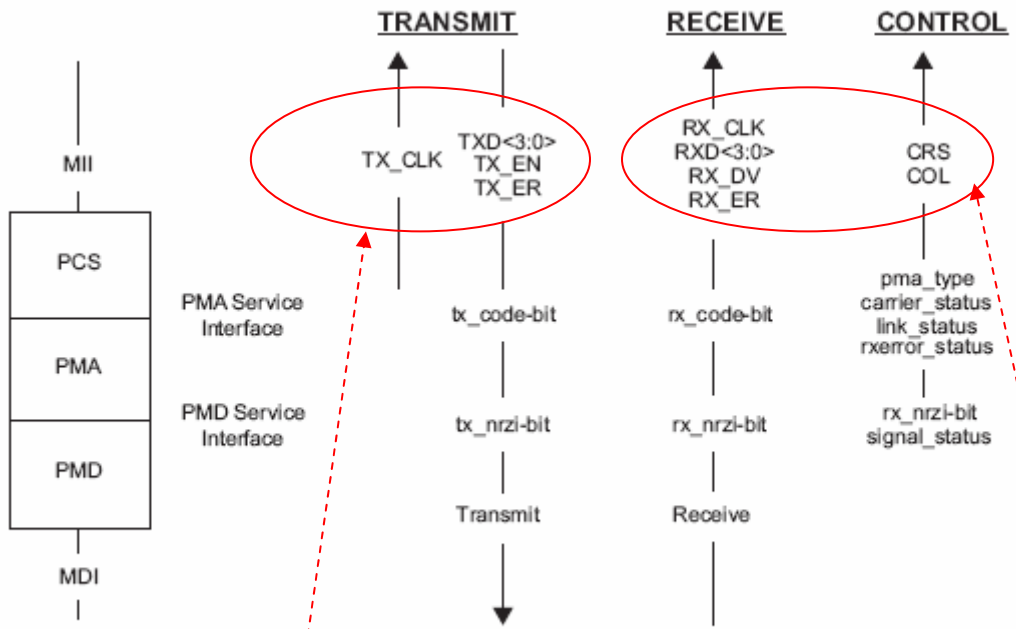


Figure 24–3—Interface mapping

MAC and PHY

TX Signaling
*** EEE_LPI**
RX Signaling
*** EEE_LPI**

PHY and remote PHY

TX Signaling
*** Sleep Signal**
*** Wake Signal**

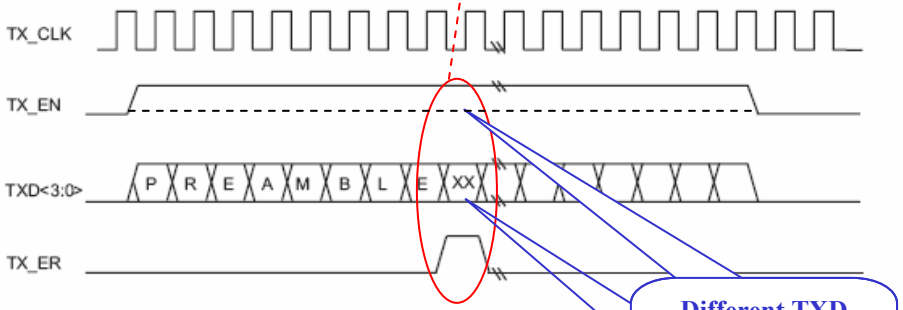


Figure 22–5—Propagating an error

Different TXD value at TX_EN=0 to convey LPI state

Figure 22–8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

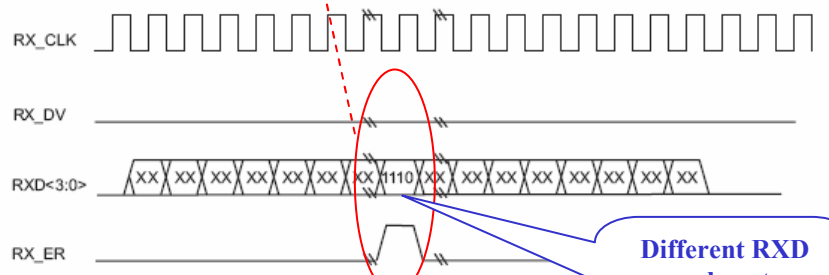


Figure 22–8—False Carrier indication

Different RXD value at RX_ER=1 to convey LPI state

Signals between MAC and PHY (MII)

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

EEE_LPI Opcode from MAC to PHY

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

EEE_LPI Opcode from PHY to MAC

Note: From 802.3az Task Force Dove_01_0108.pdf

Signals between PHYs - Sleep/Wake Request Code-groups

Table 24–1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretatio
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
INVALID	0 0 0 0 0	V	Undefined	Invalid code
INVALID	0 0 0 0 1	V	Undefined	Invalid code
INVALID	0 0 0 1 0	V	Undefined	Invalid code
INVALID	0 0 0 1 1	V	Undefined	Invalid code
INVALID	0 0 1 0 1	V	Undefined	Invalid code
INVALID	0 0 1 1 0	V	Undefined	Invalid code
INVALID	0 1 0 0 0	V	Undefined	Invalid code
INVALID	0 1 1 0 0	V	Undefined	Invalid code
INVALID	1 0 0 0 0	V	Undefined	Invalid code
INVALID	1 1 0 0 1	V	Undefined	Invalid code

Normal IDLE code-group to Wake or Refresh the Remote PHY

Unused code-group for Low-Power Line Signal to Request Sleep or Refresh the Remote PHY

Summary

- Symmetric and Asymmetric operations are no difference on LPI 100Base-TX.
- Refresh is merely a Wake-followed-by-Sleep signal.
- Short and fixed transition time (around and smaller than 10 us) across different line states.
- Faster transition time (Wake, Refresh) can be achieved with shorter Quite time.
- Minimum modification of existing Standard.
- Incorporate Loss of Link Detection during LPI mode.
- Future Works:
  - Criteria of Signal Detection.
  - Simulation verification of State Diagrams and Timing parameters.

Thank you

Questions?