A pathway to Asymmetric EEE GPHY

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Outlines

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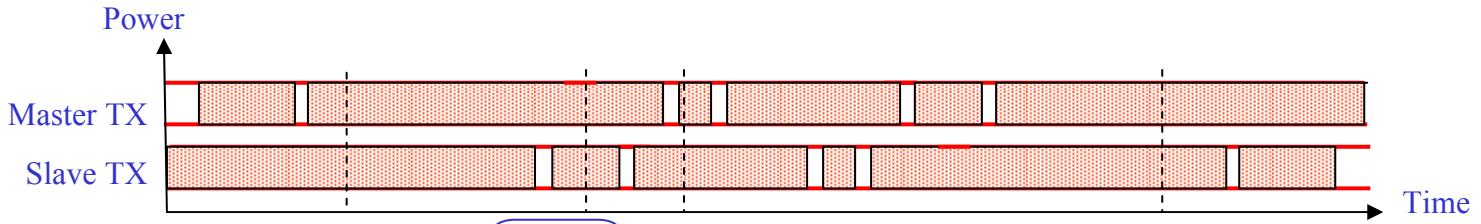
- Concerns of Asymmetric EEE GPHY
- Effects of Clock Phase Offset
- How to specify the Quiet Duration
- Current GPHY Symmetric only Operation
- Free GPHY Partially Asymmetric Operation
- Also Free, GPHY Fully Asymmetric Operation
- Summary

Objectives

- Status quo
  - The LPI EEE community fully recognize the necessity of symmetrical EEE GPHY operation (**healey_01_0108**)
  - Asymmetrical EEE GPHY operation is deemed too complicated and thus overlooked (**chou_02_0108**)
- In this presentation, it will be shown
  - A first type of asymmetrical operation is free, and thus **there is no reason for not adopting it**
  - A second type of asymmetrical operation is also free, but with potential SNR degradation.
    However, the SNR degradation can be tightly controlled by nailing down proper parameters.
    Therefore, there is no reason for not adopting it.

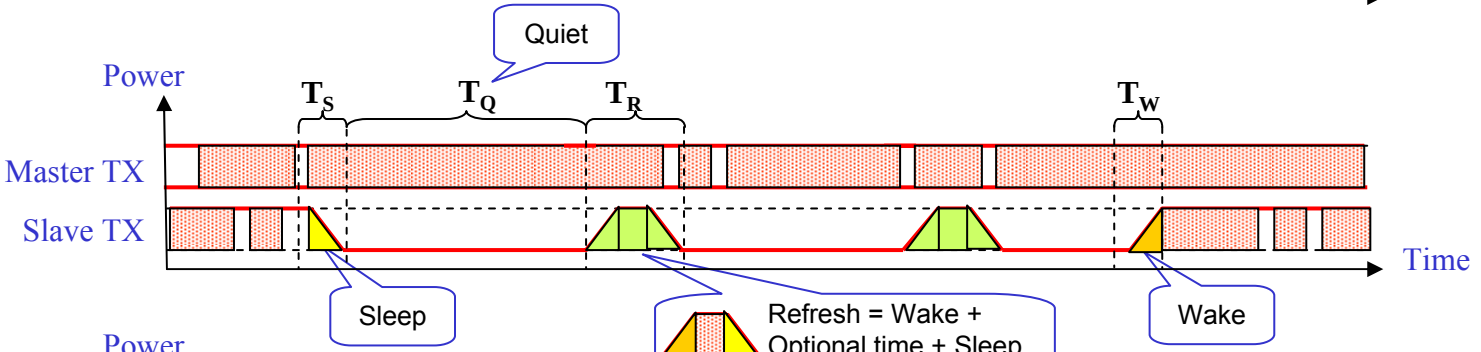
Line States of Asymmetric EEE GPHY

Case 1. Symmetrical; Both Master & Slave Active



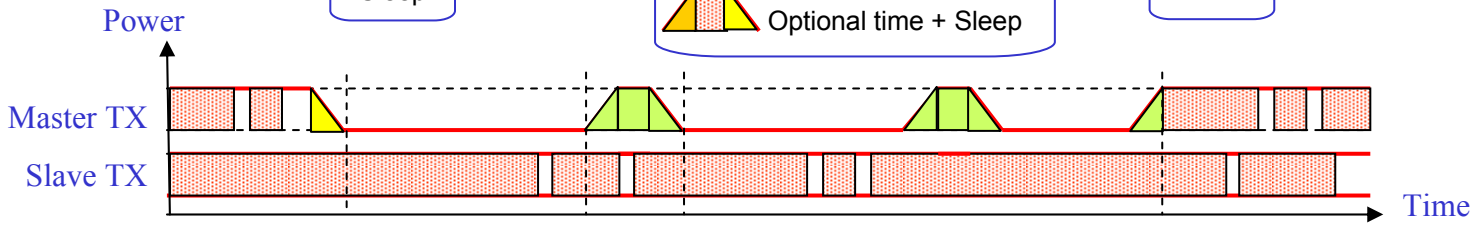
Case 2. Asymmetrical; Master Active, Slave Low-Power

- Slave sends Refresh freely with Tq= Tq-max



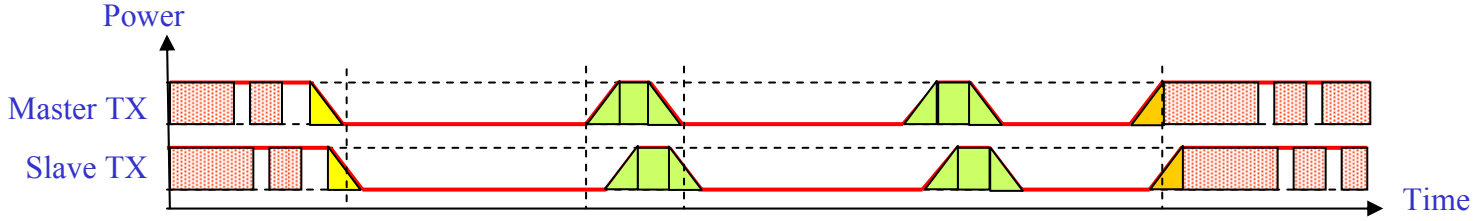
Case 3. Asymmetrical; Master Low-Power, Slave Active

- Master sends Refresh with shorter Tq≤Tq-max



Case 4. Symmetrical; Both Master & Slave Low-Power

- Master initiate Refresh
- Slave sends Refresh tracking Master Refresh



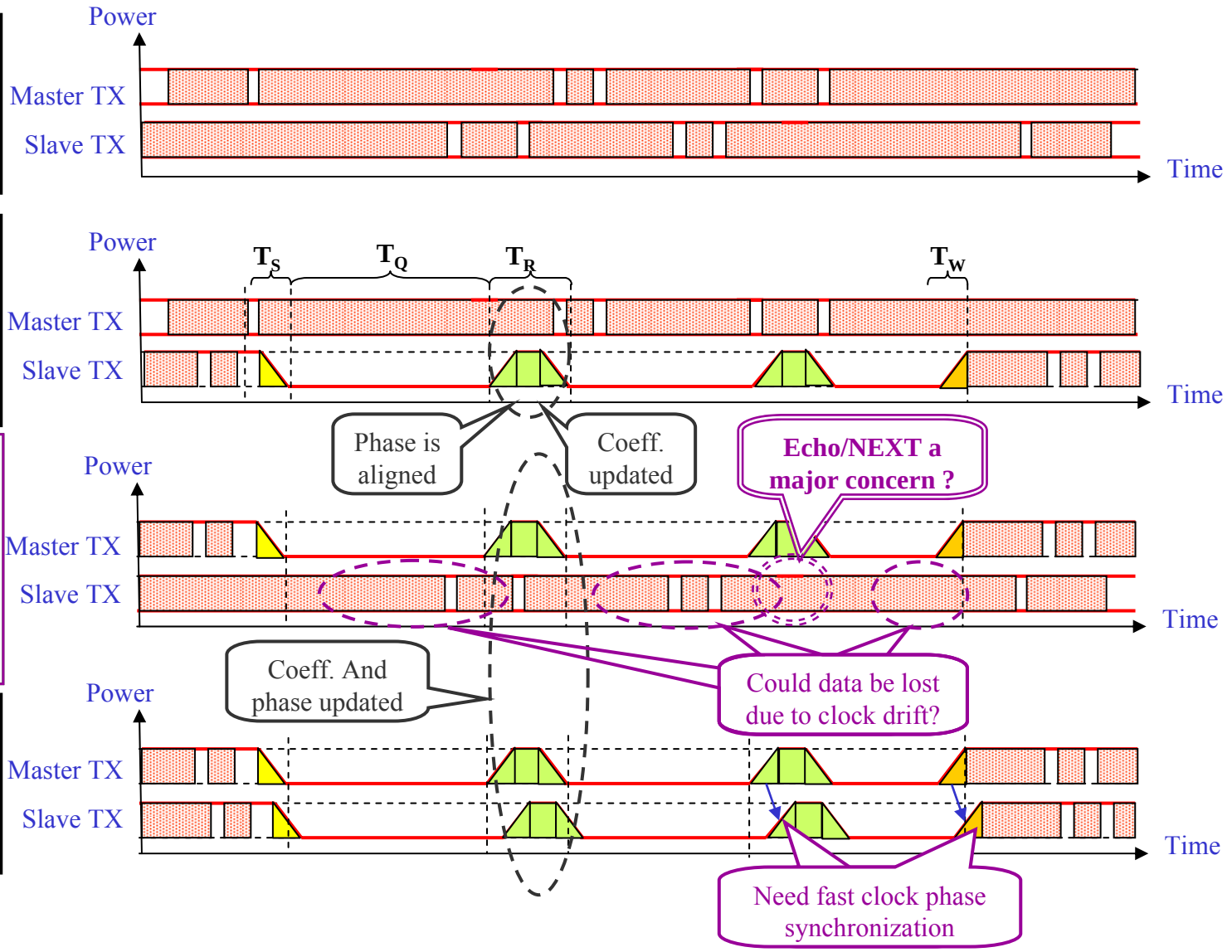
Concerns of Asymmetric EEE GPHY

1. Symmetrical; Both Master & Slave active
- Clock phase tracked
- No data missed
- Coefficients updated

2. Asymmetrical; Master Active, Slave LPI
- Clock phase tracked
- No data missed
- Coefficients updated

3. Asymmetrical; Master LPI, Slave Active
- Clock phase tracked ?
- Data corrupted or lost due to echo/next
- Coefficients updated

4. Symmetrical; Both Master & Slave LPI
- Clock phase tracked ?
- Don't care lost Data
- Coefficients updated



Effects of Clock Phase Offset

Causes of Clock Phase Offset.

- Slave clock synchronization relies on the continuous incoming Master traffic. (Loop-timing).
- May drift away on **Case 3 & 4** when Master ceases transmission. Quick clock re-synchronization is required.

❑ Echo/ NEXT Cancellation Residue may become excessive

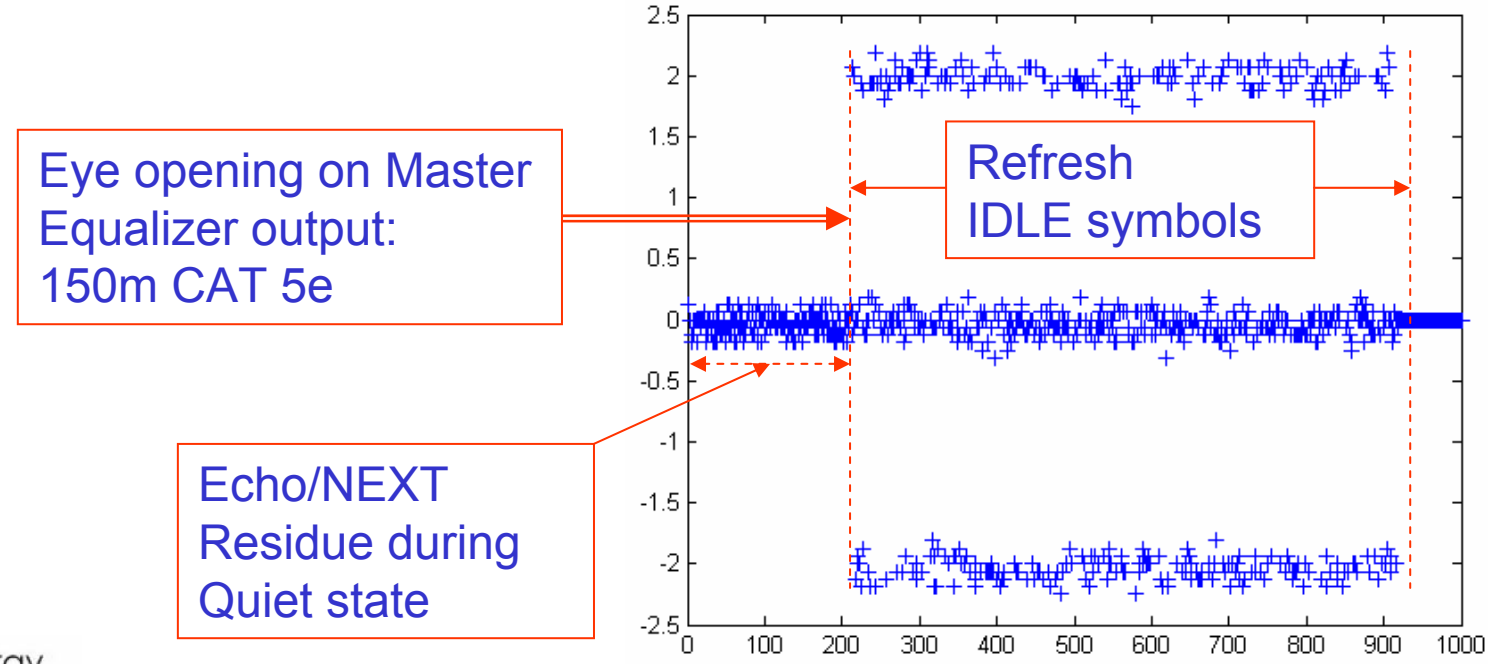
- If clock offset between Master TX and RX is accumulated when Master RX keeps tracking drifted Slave Clock.
- Can be avoided if the Master RX clock phase is frozen during the TX Quiet state until the echoed Refresh signal kicks in.

❑ RX Equalizer (FFE/FBE) may not be optimized

- If the Master RX clock phase is frozen during the **TX** Quiet state.
- Can be avoided if Master RX is tracking Slave traffic all the time.

Case 2 is the same as Case 1

- Like in Case 1, the Slave PHY always tracks the Master Clock phase. (due to loop timing)
  - The Echo/NEXT of Refresh signal is fully cancelled on Slave.
  - The Master PHY can receive Slave Refresh with eye opened immediately.
- No added complexity to implement Case 2.



Case 4 is a necessary evil

- A must-have feature of LPI GPHY.
- If Quiet Duration (Tq) is short enough, then
  - The eye is still open when Master Refresh hits Slave PHY.
  - The Slave tracks Master clock quickly and echoes Refresh.
- Otherwise
  - The Eye is severely blurred or closed.
  - Timing Recovery loop of Slave RX needs start from scratch.
  - An implementation dependent fast clock synchronization logic may be needed to shorten the duration of Refresh and Wake.
- On either case, the Echo/NEXT coefficients are all frozen until clock phase is realigned.
- The Quiet Duration (Tr) is determined by the drift speed of clock phase between Master and Slave PHYs.
- Therefore, the Quiet Duration (Tq) and Refresh Duration (Tr) are inter-dependent in this case.

Issues in Case 3

- Equalizer and Echo/NEXT coefficients are optimized under the best sampling clock phase
- If the clock phase drifts, coefficients become non-optimum and SNR degrades.
- The clock phase and frequency of slave PHY will drift anyway during the Quiet duration of master PHY.
- Trade-off between non-optimum Echo/NEXT and non-optimum equalizer :
  - **If recovered clock tracks slave traffic,** then Echo/NEXT **Cancellers are not optimized**.
  - **If the recovered clock is frozen until the Refresh signal starts,** then **Equalizer is not optimized** (**See traeber_01_0308.pdf**)
  - Need to pick the lesser evil in SNR degradation.
- In either case, the SNR degradation can be controlled by limiting the maximum possible phase drifts.

Case 3 is workable

- A clock phase drift leads to a SNR degradation
- Given a maximum allowable SNR degradation, a maximum allowable clock phase drift is determined
- Budgeting all factors leading to the clock phase drift to ensure the clock phase drift stays under the limit
- All factors are implementation dependent. We just need to choose conservative numbers that can be comfortably implemented in a practical design.
- Under practical implementation, the Quiet Duration (Tq) needs to be specified to ensure the clock phase drift is within the limit

How to determine the Quiet Duration?

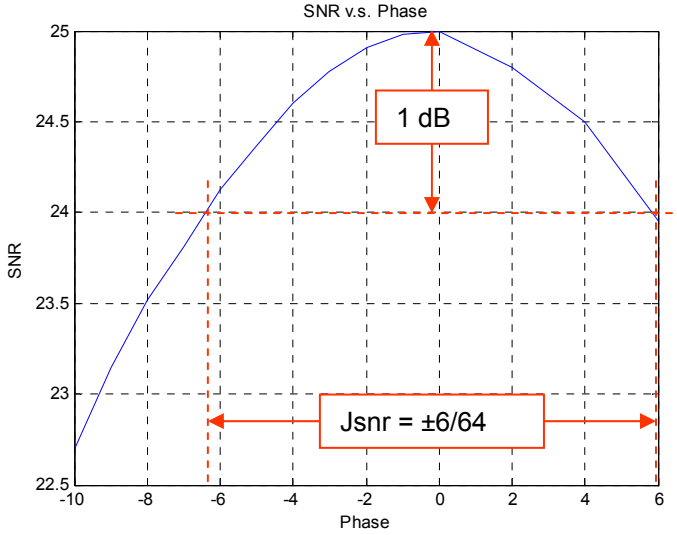
- Leverage the Formula from **traeber_01_0308.pdf**

$$T_q = 1e6 * \frac{\Delta\varphi_{acc}}{\Delta F[ppm]}$$

- Find the proper value of $\Delta\Phi_{acc}$ and ΔF[ppm]
  - $\Delta\Phi_{acc}$ (=UI*Δ) depends on $\Delta = J_{SNR} - J_{RX} - J_{TX}$
    1. J_{SNR} : The maximum **Master** clock phase offset allowed for acceptable SNR degradation .
    2. J_{RX} : Low frequency phase jitter of Clock generator for Slave DPLL
    3. J_{TX} : Low frequency phase jitter of Master TX PLL
  - ΔF[ppm] depends on $\Delta F = F_R + F_E + F_D$(ppm)
    1. F_R : Resolution of frequency value holder of **Slave** DPLL.
    2. F_E : Residual Error of Recovered Clock freq value at the time of freezing due to timing loop dynamics.
    3. F_D : Frequency drift of Referenced clock source (Xtal) of PLL.

An Example of Quiet Duration

- $\Delta\Phi_{acc}$ (=UI*Δ) =0.08*UI, Δ=J_{SNR} -J_{RX}-J_{TX} (UI) = 0.08
  1. J_{SNR} = 0.10 (UI) for 1 dB SNR degradation (Canceller residue limited)
  2. J_{RX} = 0.01 (UI) is conservative (80ps) for practical design of 125MHz clock
  3. J_{TX} : =0.01 (UI) is conservative (80ps) for practical design of 125MHz clock
- ΔF[ppm] = F_R+F_E+F_D (ppm) = 0.25 + 0.15 (design dependent) = 0.4
- UI=8ns, Δ=0.08, ΔF[ppm] =0.4 (ppm) with conservative estimate, => **Tq = 1.6ms** (c.f. Tr is in the order of 10us)

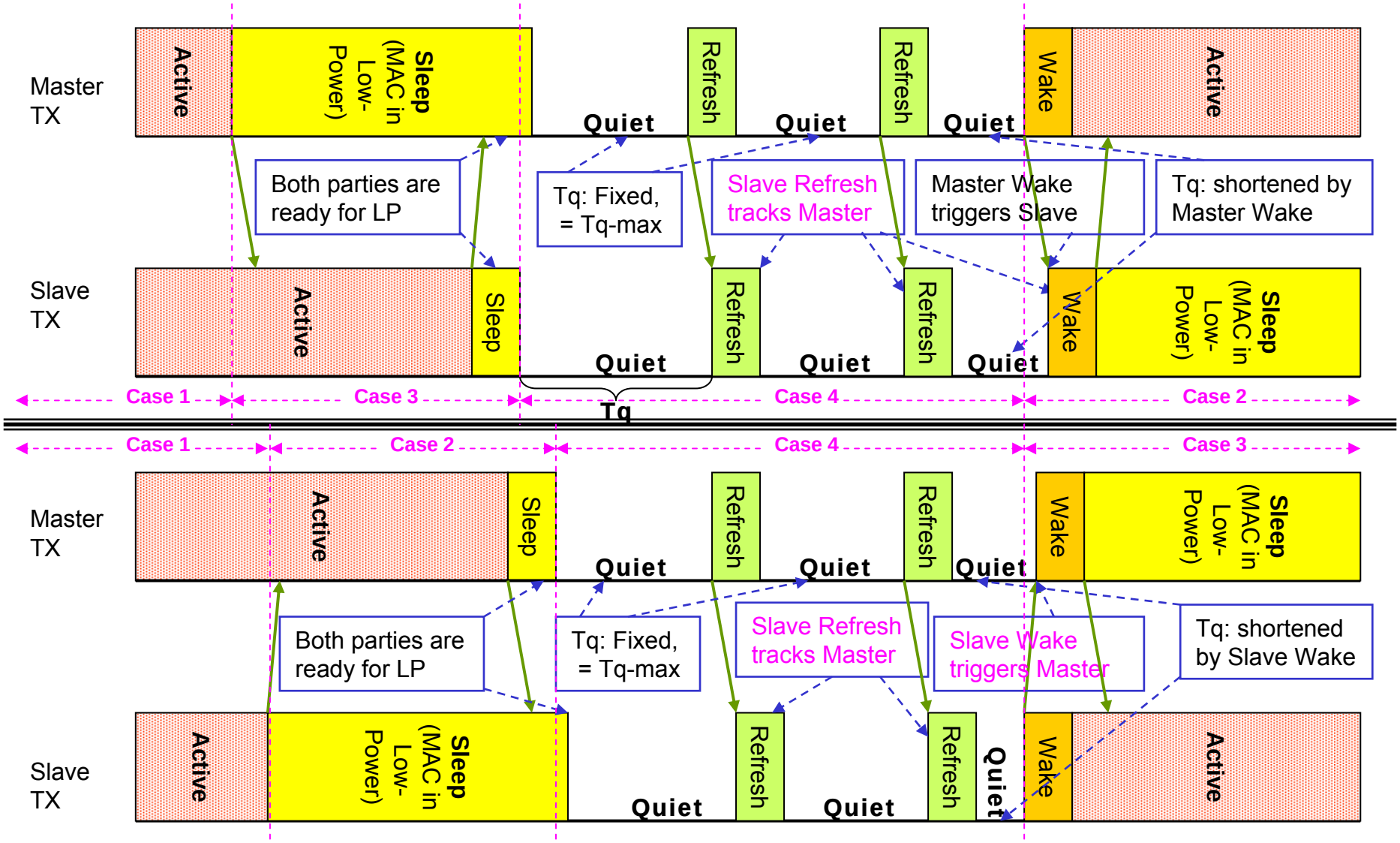


Master RX clock phase tracks Slave and drifts.

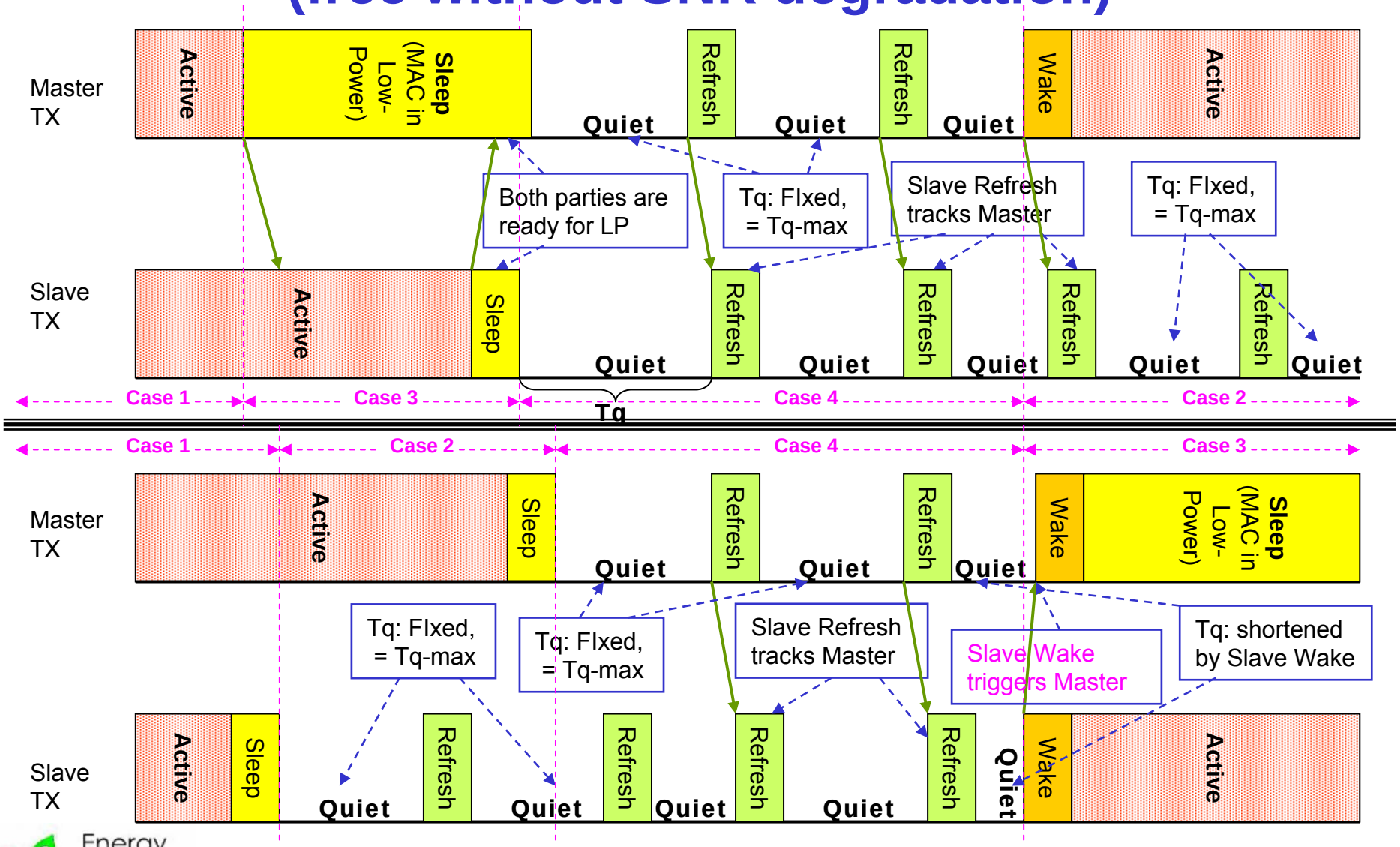
Freq value holder	Freq Resolution (Fr)
S15.13f	~2 ppm
S17.15f	~0.5 ppm
S18.16f	~0.25 ppm

S15.13f is fixed-point register with 13 fractional bits. It requires 2^13=8000 symbols to update one clock phase (=1/64 UI). 1UI=512000 sym. Therefore ΔF=1/512000≈2 ppm

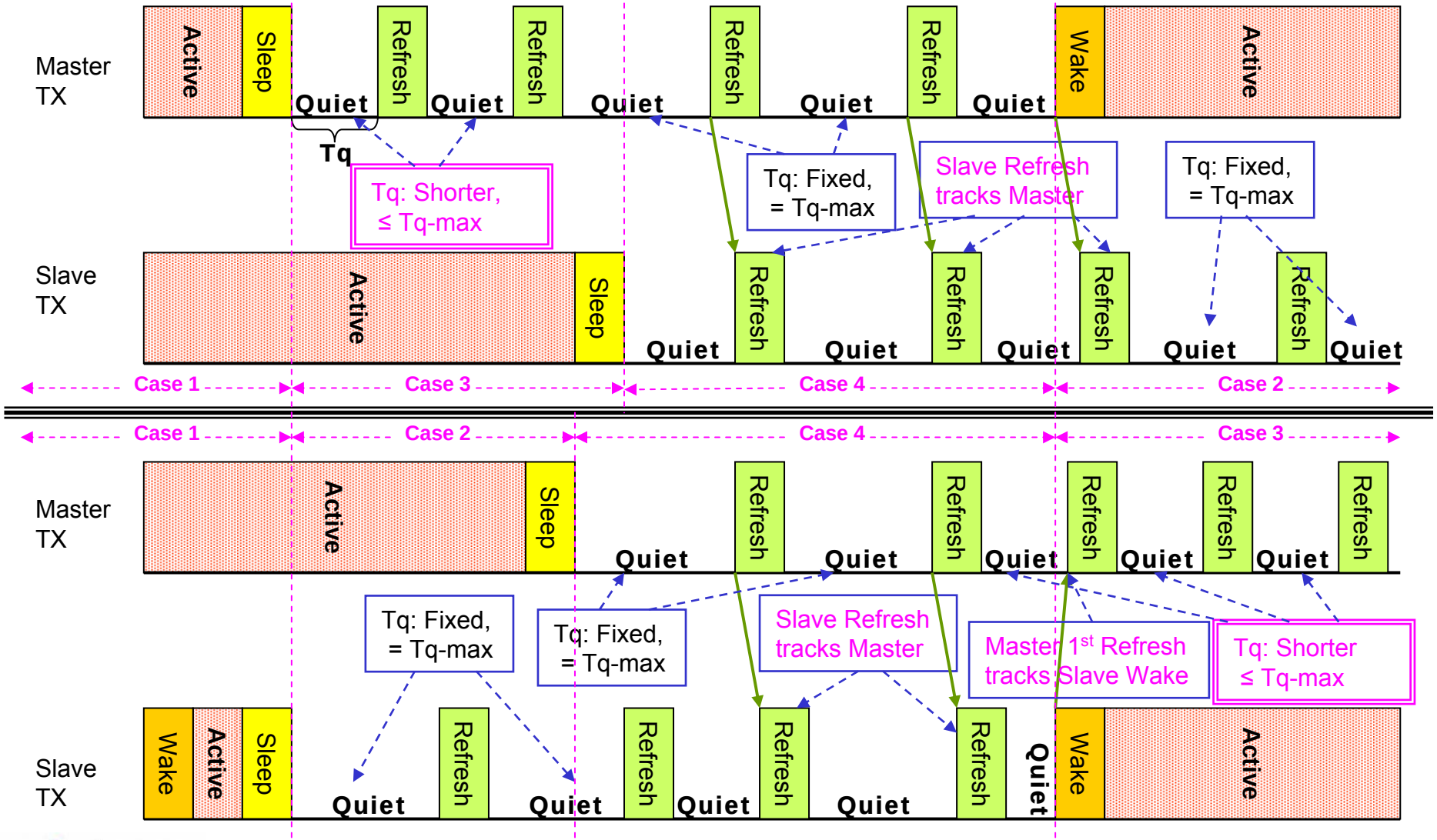
GPHY Symmetric only Operation (status quo)



GPHY Partially Asymmetric Operation (free without SNR degradation)



GPHY Fully Asymmetric Operation (Free with controllable SNR degradation)



Summary

- Asymmetric EEE GPHY Can homogenously work with Asymmetric EEE MAC and System interface.
  - Master active, slave LPI (Case 2): Natural one way operation.
  - Master LPI, slave active (Case 3): Most sensitive to Timing drift.
    Master needs to send Refresh with comfortable **Quite duration**.
    In this situation, it is not more complicated than case 4.
  - Master and slave LPI (Case 4): Slave needs to send Refresh by tracking Master's Refresh.
    Time for clock synchronization depends on the clock phase offset which in term depends on the **Quite duration**.
- The **Quiet duration** is the key parameter. It can be well estimated with good margin and be negotiated using AN, or adjusted using MCF.
- Beneficial to allow Asymmetric modes which can save more power and have no additional cost to implement.

Thank you

Questions?

Backup

Master TX Jitter

- **40.6.1.2.5 Transmitter timing jitter**
- When in test mode 2 or test mode 3, the peak-to-peak jitter Jtxout of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.
- When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than 1.4 ns. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, *H*jf1(*f*), having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus Jtxout shall be less than 0.3 ns.

$$H_{jf1} = \frac{jf}{jf + 5000};\ f \text{ in Hz}$$

Unbounded Low freq Jitter

TX CLK output jitter **NOT** Internal PLL clock output

Slave TX Jitter

- When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 40.6.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than 1.4 ns after the receiver **is properly receiving the data** and has set bit 10.13 of the GMII management register set to 1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, *H*jf2(*f*), having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus Jtxout shall be no more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by *H*jf1(*f*).

Slave CDR jitter **NOT** internal PLL clock output jitter

- For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least 10^5 clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

800 us

1.25e7b

$$H_{jf2} = \frac{jf}{jf + 32000};\ f \text{ in Hz}$$

Observations of Clause 40.6.1.2.5

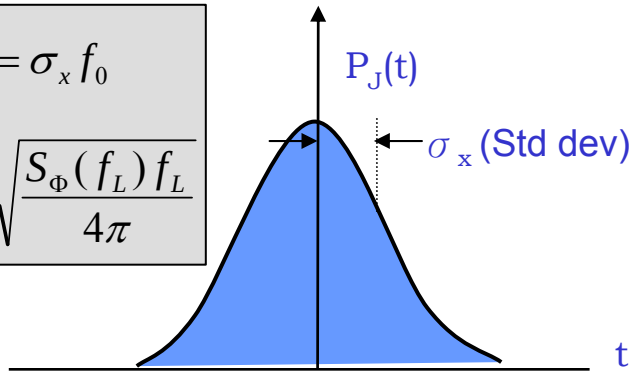
- Low frequency phase noise, Long term jitter, and low frequency drift of a PLL all imply the same effect. They can be tracked in a closed loop PLL system.
- The Jitter appears on the output of TCLK driver is **not** identical to the jitter of the clock output of internal TXCLK PLL which is used to sample the RX data stream.
  - The TCLK is affected by various source of noise coupling and distortion on circuit path.
  - Normally, the TXCLK PLL output jitter is much smaller and can be expressed in rms jitter σ_{JT} of a normal distribution w.r.t its referenced clock.
  - For example, for 125MHz clock generator (8ns period), σ_{JT} = 50 ps is not uncommon. This jitter is mainly caused by high frequency noise.
- The Slave TCLK jitter is measured on the clock output of CDR, which is **frozen** during Quiet state. It is thus similar to Master TCLK and is only related to PLL output of Slave clock generator in addition to some fixed length word effects of Timing Loop DSP.
  - Again, clock jitter can be expressed in rms jitter σ_{JR} of a normal distribution w.r.t its referenced clock.
  - The Timing Loop DSP effect can be expressed in F_R and F_E
- The Jitter spec in this clause is External-referenced Jitter including high frequency component. The sampling clock phase offset is self-referenced Jitter (N-Cycle jitter).
  - Both type of jitters depend on the length of time interval of measurement.
  - The external-referenced jitter is unbounded with std dev. σ_J. The peak-to-peak jitter depends on the population of samples (measurement time).
  - The self-referenced jitter of is also unbounded with max std dev = sqrt(2)* σ_J . The actual standard deviation changes in proportional to the square root of the length of measurement interval.

TCLK Jitter proposal

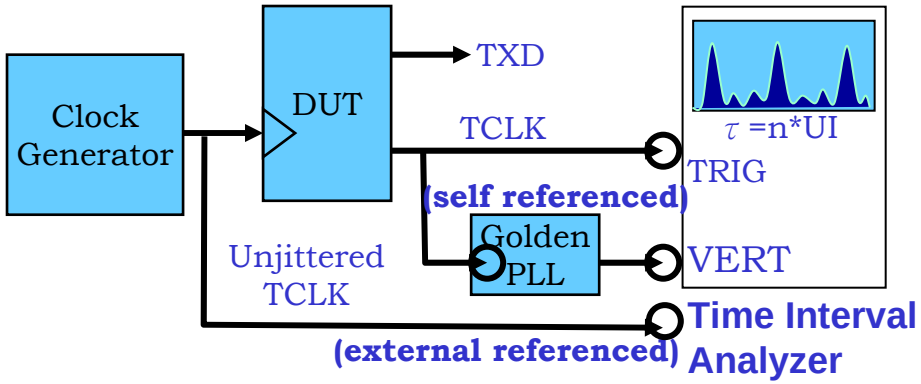
- In view of that 100ms measurement interval covers 1.25e7 symbols which represent ±5.4 σ of external-referenced jitter population,
  - $\sigma = J_{TX\ p\text{-}p}|Tq=100ms /(5.4*2)= 1.4ns/(5.4*2) = 0.13ns = 0.016UI$ (8ns period)
- And the Clock phase offset produced during the Quiet duration Tq is self-referenced N-Cycle Jitter. (please refer to next slide.)
  - $\sigma_{JTX}|Tq=100ms = sqrt(2)*\sigma = 0.023UI = 0.18ns$
  - $\sigma_{JTX}|Tq=1ms = \sigma_{JTX}|Tq=100ms *sqrt(1/100)= 0.0023UI$
  - $J_{TX\ p\text{-}p}|Tq=1ms = 4.5 * \sigma_{JTX} =0.02UI$
    Note: 1.25e5 samples (1ms) represents ±4.5 σ population.
- **A New Jitter constraint of TCLK needs to be adopted to explicitly specify the requirement of Master TCLK Jitter for Asymmetric LPI GPHY.**
  - **Tentative: The N-cycle jitter (self-referenced) measured over 125000 symbols interval (1ms) of TCLK should not exceed 0.2ns. (0.025UI)**
  - **Informative: The maximum frequency deviation of Slave TCLK from Master TCLK due to DSP error and crystal frequency drift is 0.4 ppm .**

N-Cycle Jitter of Close Loop PLL

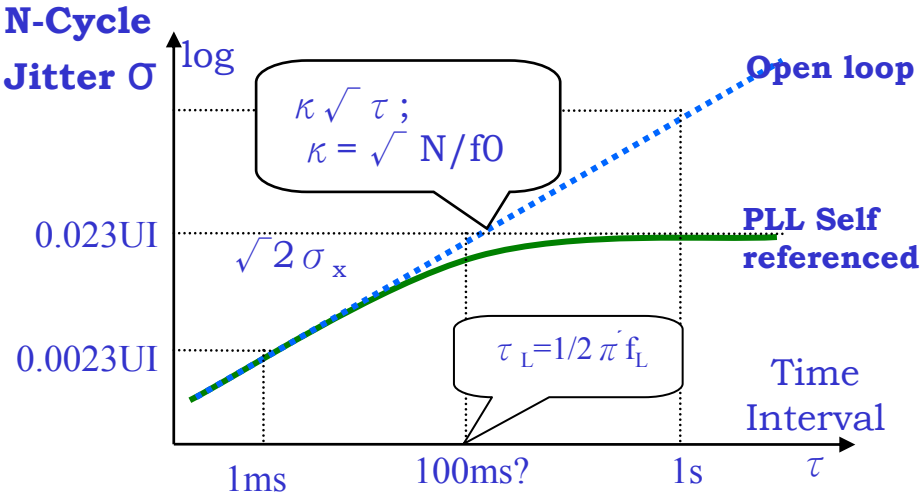
$$J_{UIrms} = \frac{\sigma_x}{T_0} = \sigma_x f_0$$
$$= \sqrt{\frac{N}{4\pi f_L}} = \sqrt{\frac{S_\Phi(f_L) f_L}{4\pi}}$$



Jitter distribution (external referenced)



Time Domain Jitter Output Test



$$S_\Phi(f) = \frac{N/f_L^2}{1+(f/f_L)^2}$$