LPI Synchronization Feasibility Questions

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Overview

- **The 10GBASE-T PHY is quite sensitive to symbol clock jitter.**
- **In the LPI proposal, the timing recovery loops need to "free-wheel" when the PHY is powered down during the LP_IDLE state.**
- **How will the presence of crystal frequency drift impact system performance and the ability to recover from the LP_IDLE state?**
  - BER degradation, dropping link, and packet corruption are not allowed.

Synchronization Questions

- **With worst-case clock drift, can the PHY recover from a power-down of up to 1000 frames without introducing bit errors or needing to retrain?**

- **With 1 R_IDLE frame and 1000 LP_IDLE frames, can the PHY track the introduced drift over a long period of time without introducing bit errors or dropping the link?**

Extreme Case Clock Phase Offset During Single LP_IDLE Interval

- **Per IEEE802.3an, Master PHY symbol rate is 800 MHz +/- 50 ppm.**
- **Consider an extreme case with linear drift over the entire operating range of 100 ppm over a 10-minute period (600 ppm/hr or 1.7e-7/second):**

Let F_s be the symbol rate Hz.
Let r_d be the constant crystal frequency drift rate in 1/sec.
Let t be the drift duration in seconds.
Then the phase offset $\phi(t)$ of the drifting clock relative to nominal is given by:

$$\phi(t) = 2*\pi*F_s*r_d*t^2$$

Example: F_s = 800 MHz, r_d = 1.7e-7, t = 320 usec (1000 LDPC frames, max LP_IDLE period)

$\phi(T_i)$ = 2*pi*800e6*1.7e-7*(320e-6)^2 = 8.8e-5 radians or 0.0014% of a symbol period.

➢ **A phase offset of 1.4e-5 of a symbol period has a negligible impact on performance and will not require a full retrain.**

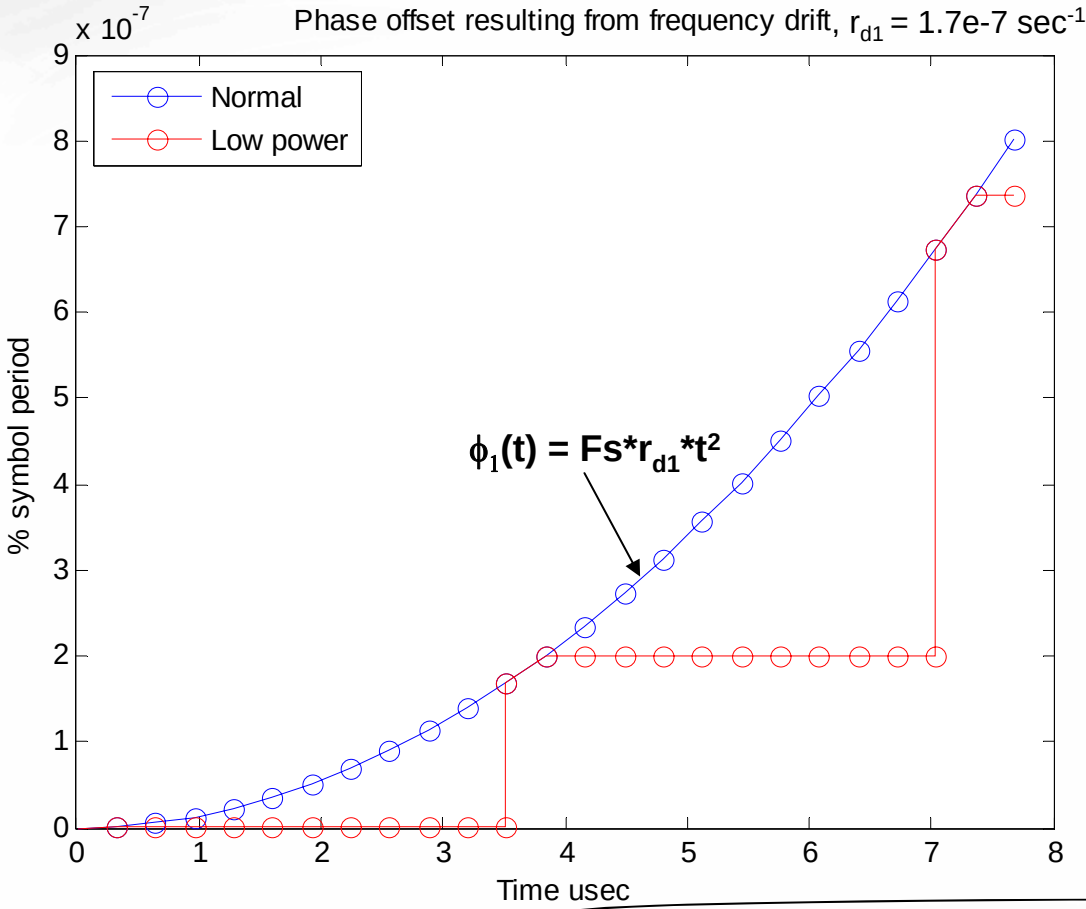
Synchronization Questions

- **With worst-case clock drift, can the PHY recover from an outage of up to 1000 frames without needing to retrain? Yes, under given assumptions, seems to be no issue here. √**

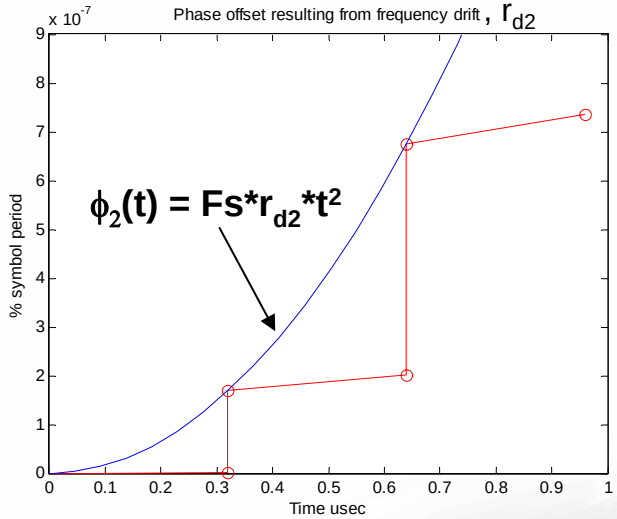
  Next consider the accumulation of phase offset in each LP_IDLE period.

- **With 1 R_IDLE frame and 1000 LP_IDLE frames, can the PHY track the introduced drift over a long period of time without degrading the BER or dropping the link?**

Impact of Frequency Drift on R_IDLE Frames



$$r_{d2} = r_{d1}[(N + M)/M]^2$$



Rn: R_IDLE Frames, M =1
L: LP_IDLE Frames, N = 10

Drift Rate Experiment

- With continuous timing adaptation (i.e. normal mode), introduce a linear drift rate of [(N+M)/M]^2 times 0.17 ppm/sec to emulate the frequency drift tracking that occurs only during refresh frames.

LP_IDLE, N (LDPC frames)	R_IDLE, M (LDPC frames)	Continuous Adaptation Equivalent Relative Drift Rate (ppm/sec)
10	1	21
100	4	110
100	1	1700
400	1	27000
1000	1	170000

- Lab experiments show feasibility of handling drift rates up to about 1000 ppm/sec[1]. Sufficient to handle (N,M) = (10,1) and (100,4), but insufficient for (N,M) = (100,1), (400,4) (400,1) (1000,4) or (1000,1).

[1]Result presented as a representative data point; other implementations may yield greater or less tracking capability.

Synchronization Conclusions

- **With worst-case clock drift, can the PHY recover from an outage of up to 1000 frames without needing to retrain? Yes, under given assumptions. Seems to be no issue here. √**
- **With 1 R_IDLE frame and 1000 LP_IDLE frames, can the PHY track the introduced drift over a long period of time?**

  Broadcom experiments indicate that synchronization may not be feasible to permit the higher N:M ratios in the LPI proposal.
  - This may limit the amount of energy savings achievable.
  - Shorter LP_IDLE periods, N, are also impacted by power-up transients to a greater degree, thereby potentially further reducing energy savings.

LPI Feasibility Study: Next Steps

Ability to recover from the LP_IDLE state is directly impacted by choice of N and M (on and off periods)

- **Determine the worst-case allowable clock drift. This is a critical parameter and should be explicit in the EEE specification.**
- **Based on the worst-case clock drift and 802.3az requirement of recovery from low-power state no BER degradation, determine practical limits on N and M and determine the amount of energy savings achievable.**
- **If these limits are deemed unacceptable, consider investigating alternate synchronization schemes.**

Back-up

Reference Frequency Drift Specification

- **Specification, "SCTE 79-1 DOCSIS 2.0 Part 1: Radio Frequency Interface" has a +/- 5ppm clock frequency accuracy requirement and a drift rate specification of 1e-8 per second over a temperature range of 0 to 40 degrees C.**
  - Stringent synchronization requirements for 128QAM S-CDMA. (Same constellation as DSQ128).
  - This standard originated in IEEE 802.14.
  - Corresponds to a ramp over the entire operating frequency range in 17 minutes.
  - Scaling for a +/- 50 ppm clock would imply a drift rate of 1e-7 per second.
  - This specification relates to an enterprise cable modem aggregation system that typically sits in a temperature-controlled head-end.
- **Considering a ramp over the entire scaled frequency range in 10 minutes yields the 1.7e-7 per second drift rate used as the extreme-case example in this presentation.**

Phase Offset Due To Frequency Drift

Let F_s be the symbol rate Hz.

Let r_d be the constant crystal frequency drift rate in 1/sec.

Let t be the drift duration in seconds.

Nominal Master symbol clock waveform:

$$x(t) = \sin(2*\pi*F_s*t)$$

Drifting Master symbol clock frequency:

$$F_{sd}(t) = F_s(1 + r_d*t)$$

Drifting Master symbol clock waveform:

$$x_d(t) = \sin(2*\pi*F_{sd}*t) = \sin(2*\pi*F_s(1 + r_d*t)*t) = \sin(2*\pi*F_s*t + 2*\pi*F_s*r_d*t^2)$$

Then the unwrapped phase offset $\phi(t)$ of the drifting clock relative to nominal is given by:

$$\phi(t) = \arcsin(x_d(t)) - \arcsin(x(t)) = 2*\pi*F_s*t + 2*\pi*F_s*r_d*t^2 - 2*\pi*F_s*t = 2*\pi*F_s*r_d*t^2$$