Low-Power Idle for 1000bT

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Energy Efficient Ethernet

IEEE P802.3az EEE Task-Force
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Never stop thinking

Supporters:

- Your name here.

Objectives

- Outline reliable asymmetrical LP_IDLE for 1000baseT
- Outline Timing to be the only critical parameter for LP_IDLE
- Outline Dimensioning Criterion for min/max of T_q
- Propose an LP_IDLE signaling fitting the needs for
  - 302.3-clause 40
  - Performance Figure of Merits for robust LP_IDLE
- Propose Priority Resolution Function for LP_IDLE ANEG parameter

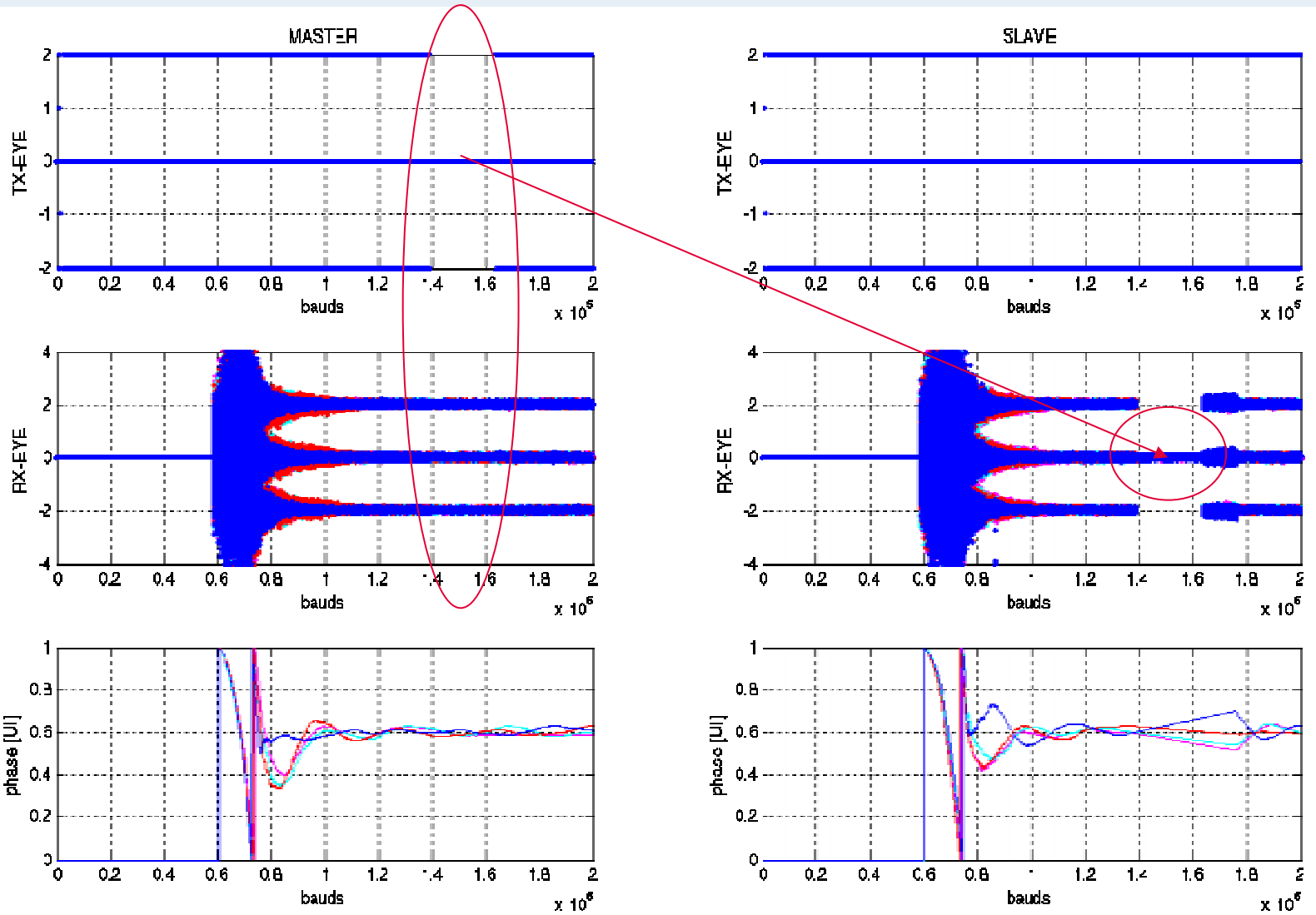
Agenda

- Asymmetrical LP_IDLE possibility for 1000baseT
- The technological challenge: Echo or Timing?
- SNR-drop versus phase-mismatch
- Discussion of Sleep/Wake Signaling
- Auto-Negotiations Priority Resolution

Asymmetrical LP_IDLE - Recap

- chou_01_0108 showed reliable asymmetrical LP_IDLE for 100baseTX
- chou_02_0108 showed the demand for asymmetrical LP_IDLE as well for 1000baseT with concerns about residual echo if only Master performs in LP_IDLE transitions but SLAVE stays ACTIVE.
- healey_01_0108 proposed special but simple signaling for LP_IDLE (enter and exit)

Asymmetrical LP_IDLE for 1000bT
An Demonstrative Simulation



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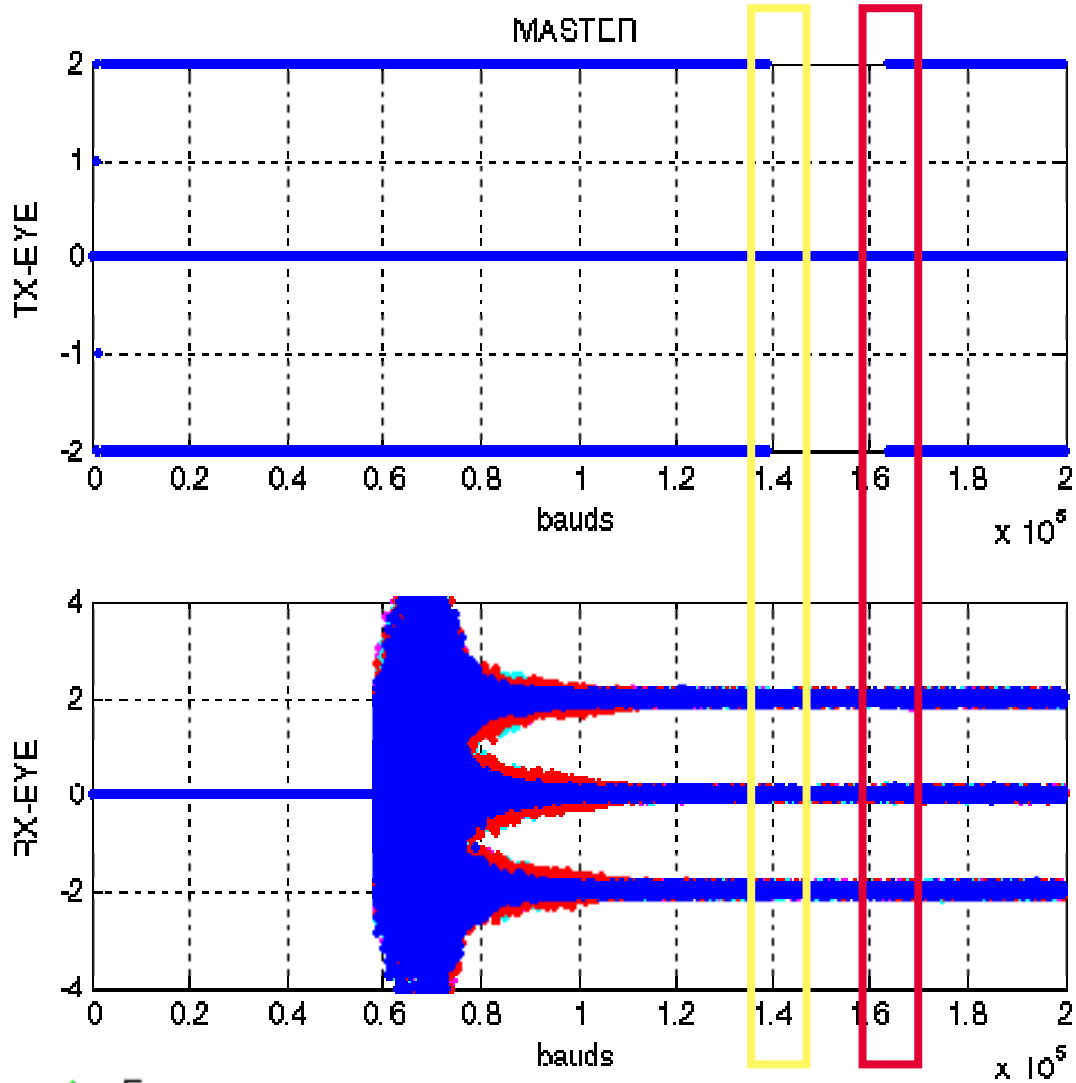
Asymmetrical LP_IDLE for 1000bT
Looking at the **ECHO/NEXT**



- Transition from
  IDLE/REFRESH
  into
  QUIET
  is not critical since ECHO/NEXT is synthesized by cancellers
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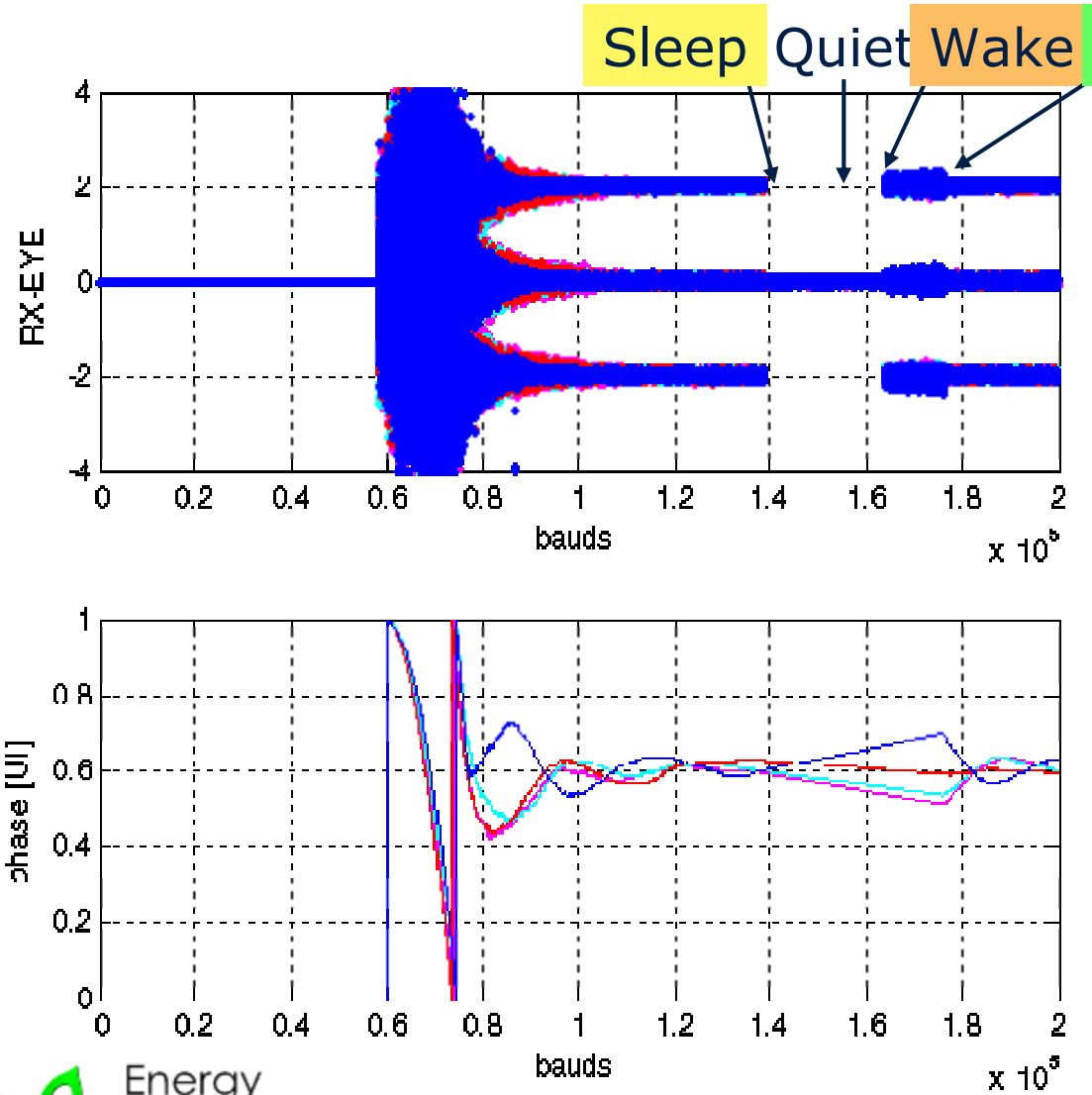
  into
  IDLE/REFRESH
  is not critical since ECHO/NEXT is synthesized by cancellers
- … as long as SEND_Z is used to switch off the transmitter!

LP_IDLE generation using SEND_Z primitive

- ECHO-/NEXT-Canceller can only cancel the transition transients when on/off function is not part of the echo-/next-channel
- Using SEND_Z appears logical and follows the standard.
- Simple enhancement of the PHY state diagram as of 802.3-clause 40 is possible.
- Transmit Modes Map to the existing primitives:
  - QUIET SEND_Z
  - SLEEP SEND_I
  - REFRESH SEND_I
  - WAKE SEND_I
  - ACTIVE SEND_N

Asymmetrical LP_IDLE for 1000bT
Looking at the **PHASE**

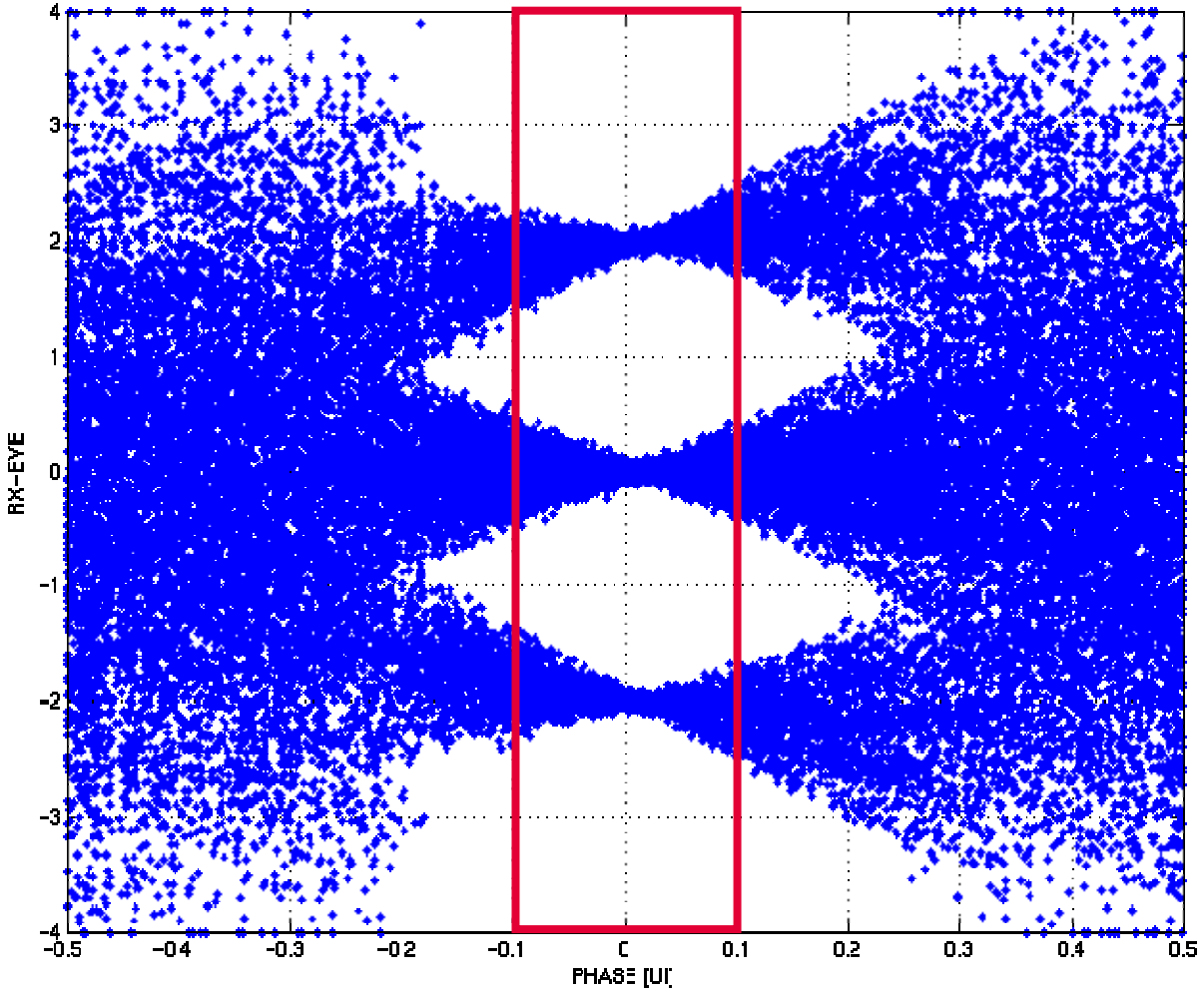


- Transition into QUIET forces MASTER to freeze rx-phase and SLAVE to freeze rx-freq.
- MASTER and SLAVE operate self-timed during QUIET.
- SLAVE is misaligned with its rx-freq by Δf which causes its rx-phase to diverge
- Since SLAVE must loop its timing inherently the MASTER rx-phase diverges
- In theory only timing must be re-acquired during REFRESH/IDLE.
- Since EYE is still open refresh is very fast

1000baseT has similar requirements as 100baseTX

- 100baseTX has same baud-rate as 1000baseT
- ECHO- and NEXT are not affected by the LP_IDLE (as shown before)
- FREQ/PHASE is the only issue
- Since IDLE Line-Code is the same as for 100baseTX also the Figure of Merits are similar for 1000baseT

Eye-Opening over RX-Phase (Filters frozen)



- RX-EYE closes the more phase-offset is accumulated.
- SNR-drop of 6dB (coding gain of Viterbi-Decoder) allowable.
- Maximal phase-offset of +/-0.1*UI shall be tolerable
- Hence T_q must be small enough not to accumulate 0.1*8ns=800ps
- This criterion can be used to dimesion T_q

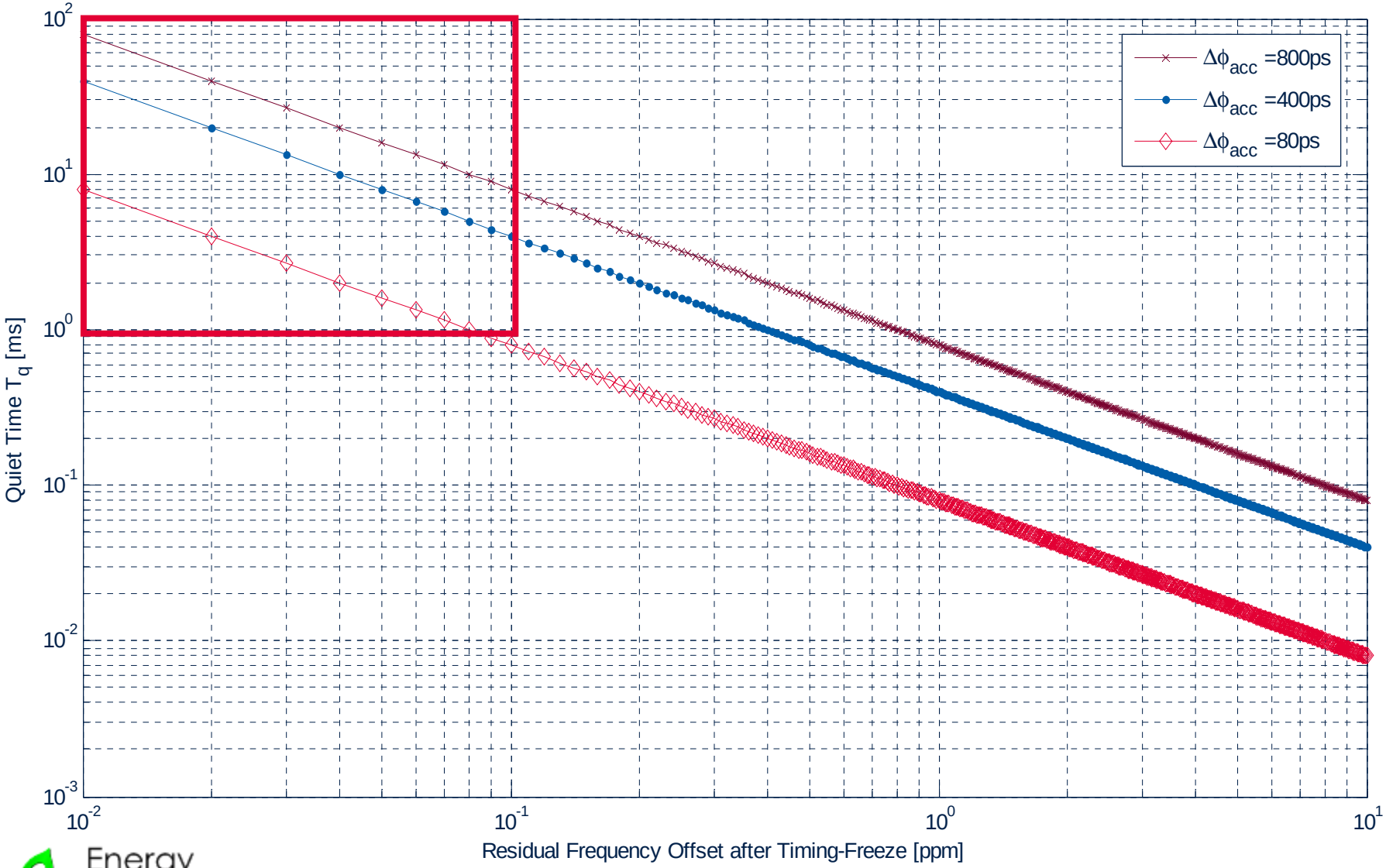
Quick Estimation of T_q

- The accumulated phase-offset calculates to
  $\Delta\phi_{acc}=UI*\Delta=800ps$ ($\Delta\phi_{acc}=800ps$ for $\Delta=0.1$, UI=8ns)
- The number of baud-symbols during LP_IDLE calculates to
  $N_q=T_q/UI$ ($N_q=12.5e6$ for $T_q=100ms$)
- The phase-error at Sleep is allowed to be maximally
  $\Delta\phi_{baud}=\Delta\phi_{acc}/N_q$
- The maximally allowed frequency offset of the estimated receive timing at the loop-filter output is calculates to
  $\Delta F[ppm]=1e6*(\Delta\phi_{baud}/UI)=1e6*(\Delta\phi_{acc}/T_q)$
- In General the maximum Quiet Time depending on the Frequency locking quality calculates to

$$T_q = 1E6 \cdot \frac{\Delta\varphi_{acc}}{\Delta F[ppm]}$$

- Assuming 0.01ppm locking quality yields **T_q=80ms** quiet time.

Shmoo Plot for T_q



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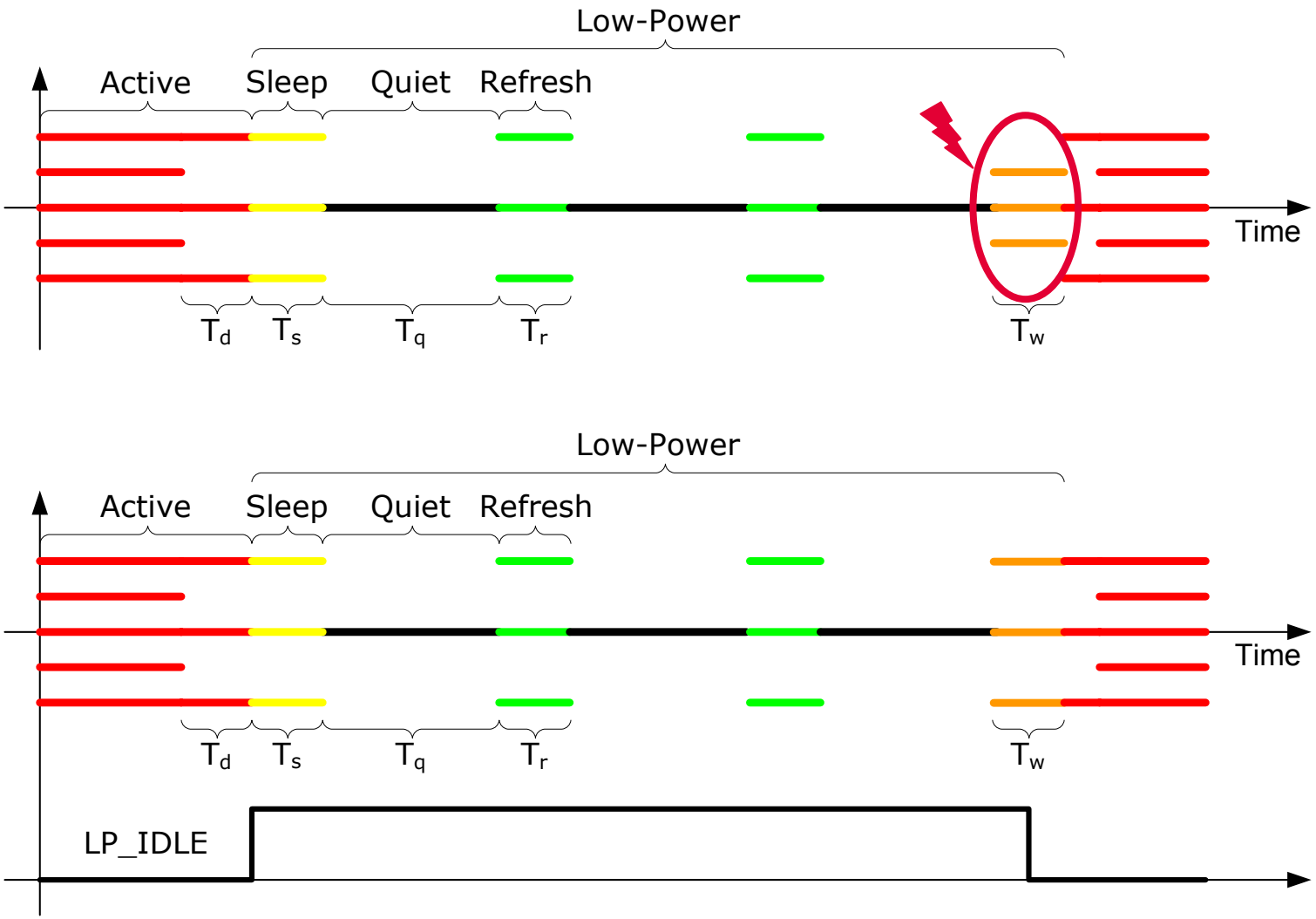
Wake-Signaling (1/2)

- The larger the allowed SNR-drop the larger T_q can be
- healey_01_0108 propose to use {-1,0,+1} symbol alphabet for Wake Signaling.
- This generates 2 issues:
  - (1) The use of 5-PAM slicer is required which reduces the SNR-margin by approximately 6dB
  - (2) The signal power is reduced by 6dB
- Consequently it is proposed using the conventional line-code of {-2,0,+2} for all IDLE signals (SLEEP, REFRESH, WAKE, IDLE)
- LP_IDLE shall be indicated using FLAGs in the PCS
- Using FLAGs is similar to the 4B5B Code-Group approach suggested for 100baseTX

Wake-Signaling (2/2)



LP_IDLE Indication using FLAGs in PCS

The bit $Sd_n[2]$ is used to scramble the GMII data bit $TXD_n[2]$ during data mode and to encode loc_rcvr_status otherwise. It is defined as

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] \text{ if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 \text{ else if } (loc\_rcvr\_status = \text{OK}) \\ Sc_n[2] \text{ else} \end{cases}$$

existing

$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if } (tx\_enable_{n-2}=1) \\ Scn[3] \wedge 1 & \text{else if (LP\_IDLE)} \\ Scn[3] & \text{else} \end{cases}$$

new

Priority Resolution for Parameters T_q, T_r, T_s and T_w

- LD_IDLE is to save power but not to harm:
  - Interoperability
  - Performance
  - Reliability
- Thus the Priority Resolution Function for LP_IDLE ANEG parameters must favor performance over power-efficiency
- Hence the weakest PHY must win:
  - $T_q = \min(T_q^{master}, T_q^{slave})$
  - $T_w = \max(T_w^{master}, T_w^{slave})$
  - $T_s = \max(T_s^{master}, T_s^{slave})$
  - $T_r = \max(T_r^{master}, T_r^{slave})$

Conclusion

- 1000baseT has shown to be operable for asymmetric mode
- 1000baseT operates the same in asymmetric and symmetric LP_IDLE
- 1000baseT just requires REFRESH synchronization in symmetric mode
- 1000baseT has shown to be similar to 100baseTX LP_IDLE
- Line-Code should not change during Wake to maximize EYE-opening
- LP_IDLE Signaling shall be done using LP_IDLE modifier in the PCS on bit $Sd_n[3]$ similar to loc_rec_status on $Sd_n[2]$
- Quiet shall be achieved using the SEND_Z functionality of the PCS
- Sleep, Refresh and Wake shall be of same line-code but might be of different duration
- ANEG LP_IDLE parameters shall be priority-resolved according to the weakest PHY wins method

Areas for Further Investigation

- Measurements and Analysis of Oscillator frequency drift
- Simulation of typical Loop-Filter Settings targeting min-max values for the following LP_IDLE Timing parameters:
  - Tr (Refresh)
  - Tq (Quiet)
  - Ts (Sleep)
  - Tw (Wake)

Thank You!

BACKUP