EEE Backplane Architecture

Hugh Barrass (Cisco)

With changes based on suggestions from Velu Pillai

Training for backplane (10GBASE-KR)

Current draft describes training frames transmitted during LPI refresh & wake

The training frame serves 2 purposes during LPI

- Random data allows equalizers to train
- Conveys sleep/wake (also last frame for rapid block lock)

Alternate mechanism could use scrambled LPI/Idle

- Same spectral content – same equalizer training
- Sleep/wake conveyed by LPI/Idle
- Poses problem for block lock (or FEC framing lock)

Alternate means to assist block lock

Instead of “last training frame” – reset the scrambler after Tx_quiet transitions from true to false

- Explicit scrambler_reset from TX LPI s/m
- Also FEC block starts on transition (first 66b after scrambler reset)

As transmission starts, a known pattern is sent

- Until transmission changes to non-LPI (i.e. Idle)
- Either 66b or FEC block lock can be very rapid

This requires no intervention from PMD

- PCS controls entire cycle, datapath passes through PMA & PMD

Division of labor in non-BASE-T PHYs

Behavior modified to use scrambled LPI/Idle instead of training frames (both FEC & non-FEC operation supported)

Which sublayers are responsible for control?

- Common sublayers for different media
- Similar behavior at different speeds

Primarily looking at 10Gbps – 10GBASE-R

- Clause 49 - PCS, 51 – PMA, also 74 - PMA
- Specific PMDs may need extra definition – Clause 72 backplane
- Other speeds & similar PHYs: 48/71; 36/70

Usual functions of sublayers

PCS – coding, state control, lane alignment, link quality

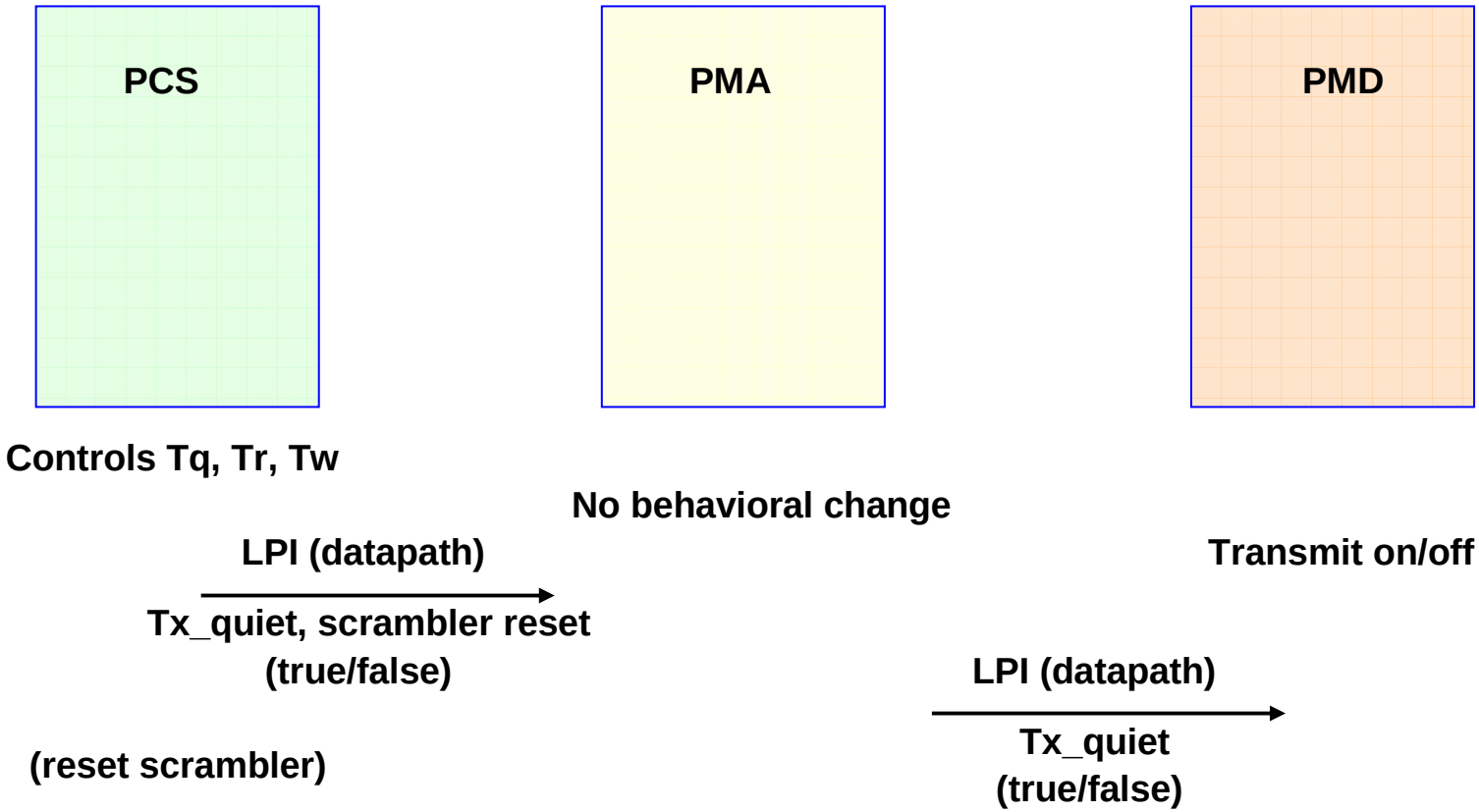
PMA – serialize/deserialize, clock/data recovery

FEC is defined as a function within PMA

PMD – signal detect, equalization

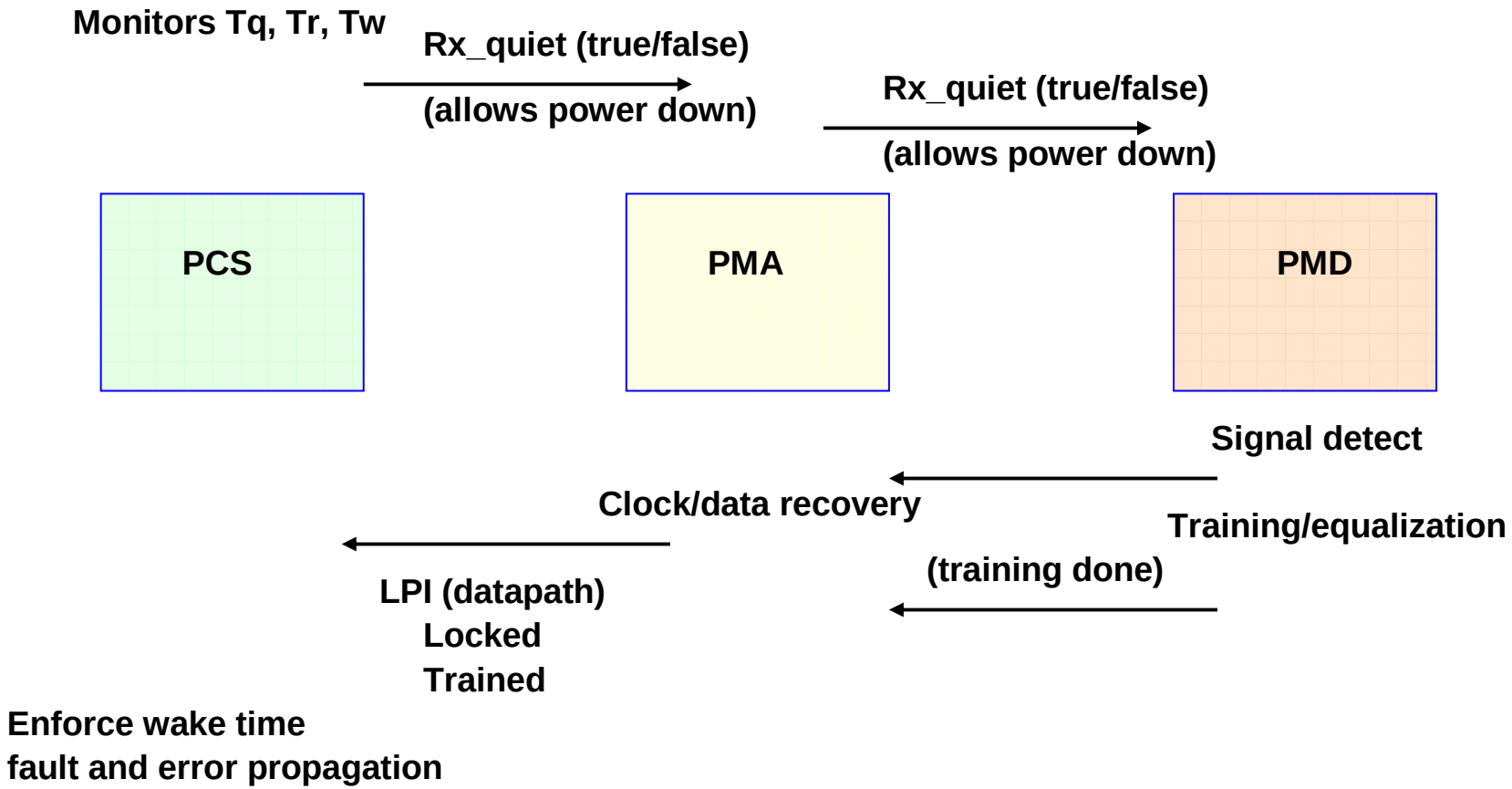
Simple transmit path behavior

PCS/PMA/PMD in relation to LPI



Simple Receive path behavior

PCS/PMA/PMD in relation to LPI



PCS functions and interfaces

Functions:

Transmit side: Tq, Tr, Tw state machine, reset scrambler

Receive side: Monitor state machine, override link state; detect wake time fault; detect Tq violation, rapid block lock

Also, scrambler reset timing Tsron, Trsoff

Interfaces:

Transmit side: Tx_quiet, scrambler_reset (true, false)

Receive side: Rx_quiet (true, false); signal_detect; lock; training_done

PMA/PMD functions and interfaces

Functions:

PMA transmit side – no functional change

- FEC – force block start

PMD transmit side – Tx on/off

PMA receive side – implementation change – fast lock

- FEC – fast block lock (refresh & wake)

PMD receive side – signal_detect; training_complete

Interfaces:

As for PCS – PMA (& FEC) must pass through

Extra note regarding scrambler reset

For the PCS LPI Tx state machine:

When in state TX_WAIT, if scrambler_reset_enable & tx_tw_timer_done – transition to new state. Hold scrambler in reset while in the new state (for 1uS).

For the scrambler:

Reset all the scrambler registers, otherwise scrambler operates as normal.