Enhanced EEE proposal for 10GBASE-KR

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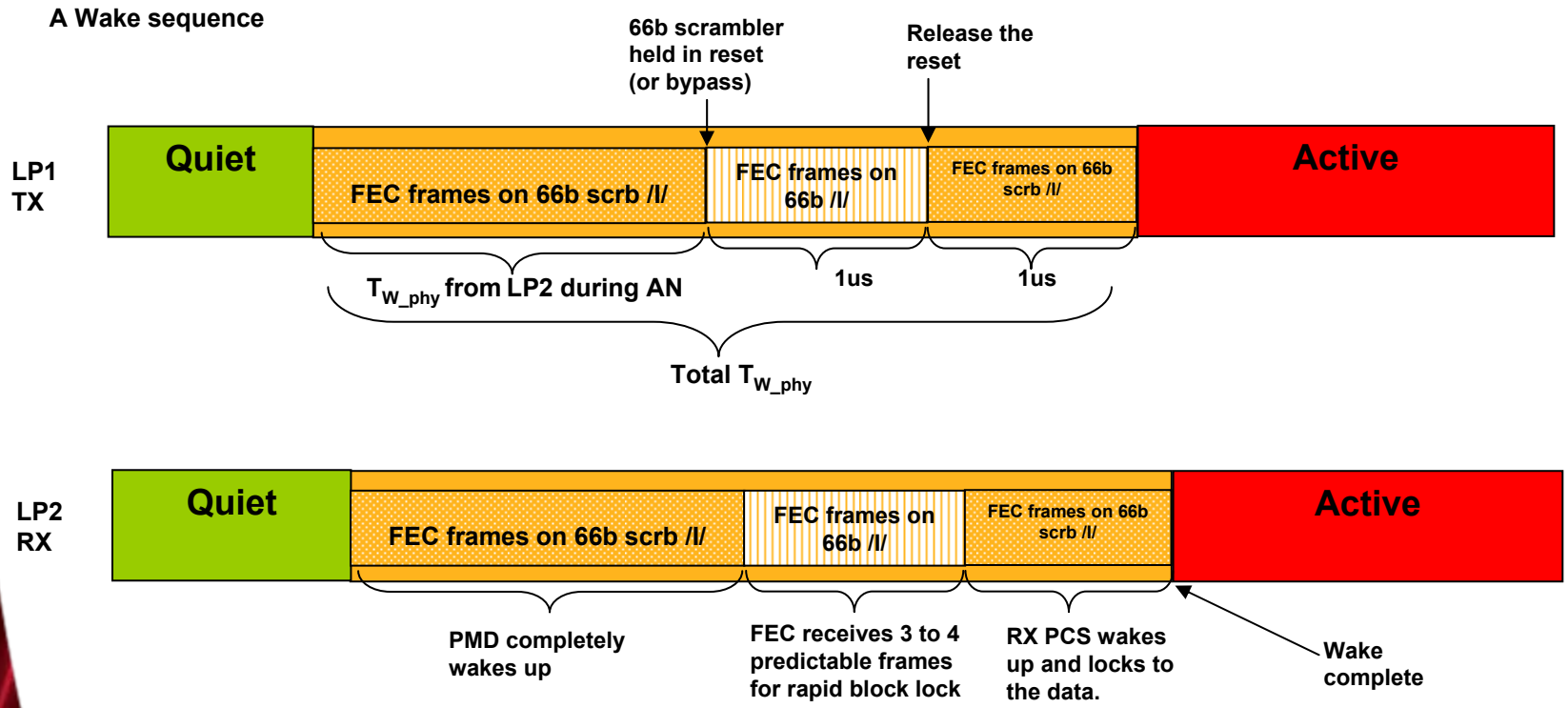
Refresh and Wake without training frame.

- EEE_BP_Arch_01.ppt presented by Hugh Barrass simplified the baseline proposal and aligned it with the other LPI baselines
- Benefits of the simplified proposal:
  - No training frames.
  - No need for synchronizing the last wake frame and FEC frame.
  - PMD does not need any control state machine.
  - Very little inter-sublayer interfaces.
  - Sublayers keeps their functionality as defined.
  - Simple to adopt this method for Optical-R Phys, XFI etc.
- However there are some issues:
  - FEC encoder is receiving a 66b scrambled data during the refresh and wake period. Which means the FEC encoded frames are totally scrambled. FEC decoder will start seeing this data after several micro secs, that means after several 10K bits (1usec = 10k bits). A rapid block lock cannot match to a totally scrambled sequence after several thousands of bits.
  - Generally bulk of the refresh time is used for training the equalizer and a small portion is for the PCS to lock to the codeword and identify the refresh pattern. In this proposal FEC needs to lock during the refresh period, which means the refresh and wakes times needs to be almost the same.

A Hybrid Approach

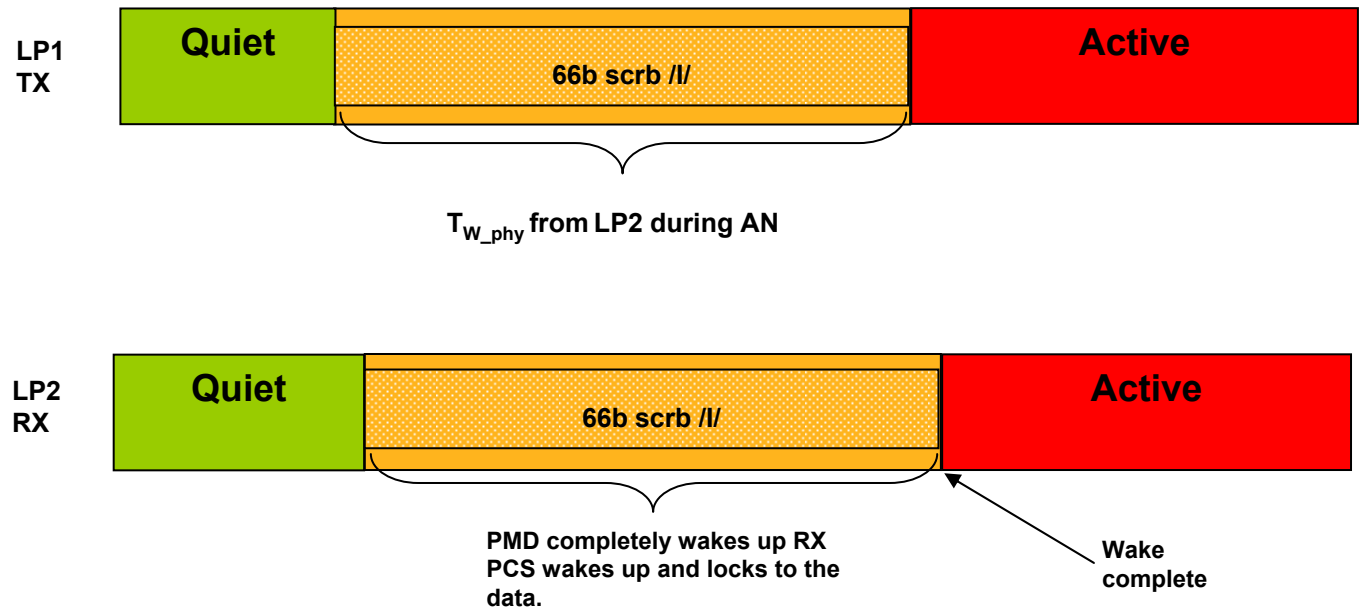
- This enhanced proposal keeps the simplification in line with the other baselines and also solves the issues related to FEC rapid block lock.
- During the refresh and wake time period:
  - Initially allow scrambled data for better equalizer training.
  - Then follow it with a deterministic FEC frames for rapid block lock.
- Refresh time period:
  - Making the refresh and wake time the same seems to be a minimal impact to the power saving.



When FEC is not enabled.

- No need to keep the 66b scrambler in reset (or bypass)
  - Keeping it in reset will send out a repetitive pattern.
    - Not ideal for the receiver CDR.
    - 66b descrambler will not keep the lock.
- Hence if the FEC is disabled CL49 LPI transmit state machine should skip the FEC rapid lock state.
  - This will also make the state diagram useable for Optical-R PHY and XFI interfaces as it is.

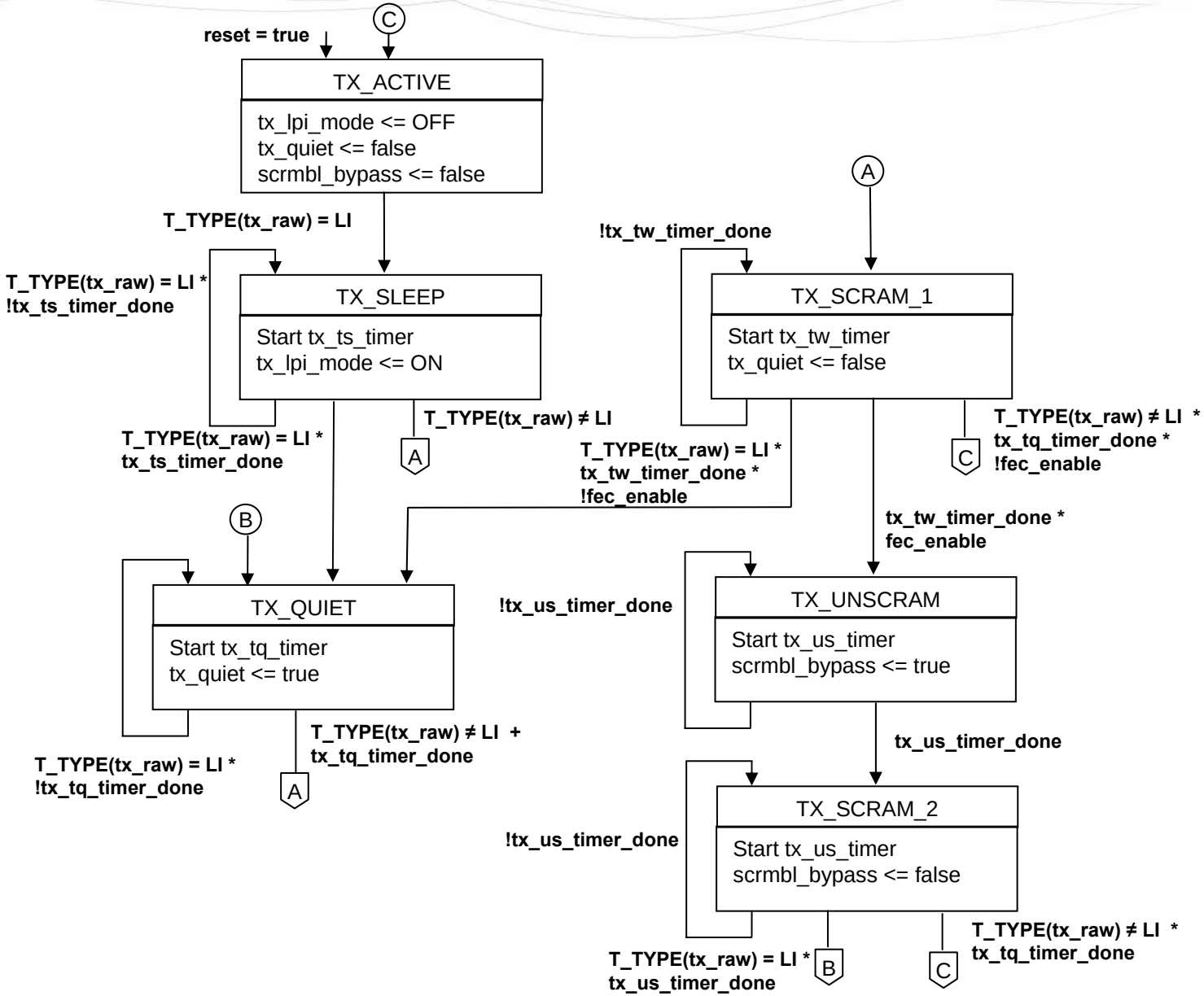
A Wake sequence for KR with no FEC / Optical-R / XFI



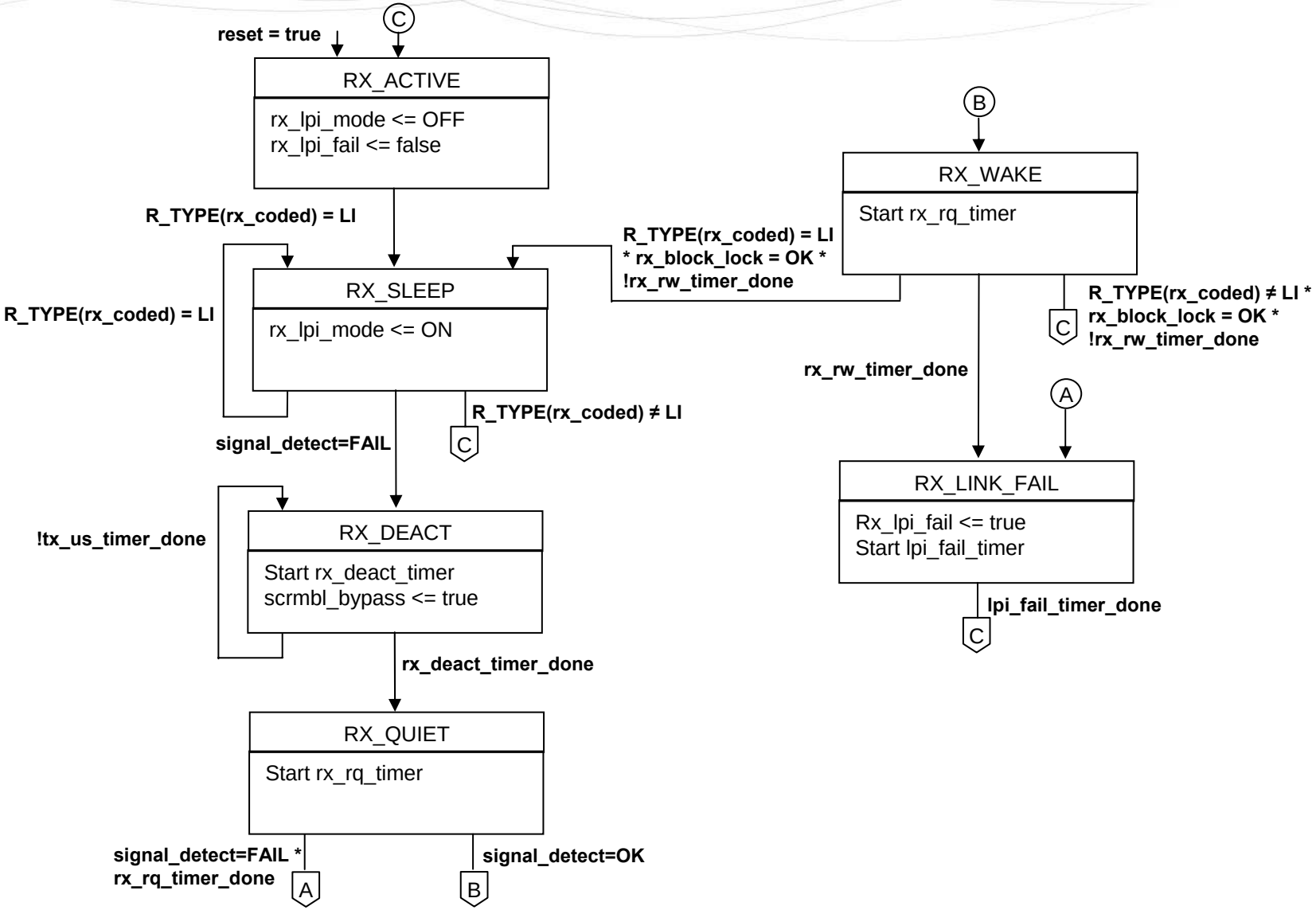
List of changes to the Clauses

- Clause 49
  - CL49 PCS transmit and receive state machine remains the same as it is now.
  - CL49 LPI transmit state machine needs changes:
    - State transitions to handle the new refresh and wake sequencing.
    - Should be looking at FEC enable status through sublayer interface.
  - Need to define a reset state for CL49 scrambler or a bypass.
  - CL49 LPI receive state machine needs changes:
    - State transitions to handle the new refresh and wake sequencing.
- Clause 72
  - Remove all the LPI transmit and receive state diagrams.
  - Only the sublayer interface for TX_disable, transmit signal parameters and receive side sigdet needs to remain.
- Clause 73
  - No addition changes than what is there today.
- Clause 74
  - We need to add a sub clause to explain the rapid block lock and to expect the predictable frame during refresh and wake period. But the frame itself is outside the scope of this standard.
- Timer values
  - Needs to be revisited.

Clause 49: LPI Transmit state diagram



Clause 49: LPI Receive state diagram



Thank You