EEE Compatible MII/GMII Interface

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Joseph Chou, Dachin Tseng, Albert Kuo

Realtek Semiconductor Corp.

Supporters

- Brad Booth (AMCC)
- Dan Dove (ProCurve Networking by HP)
- Paul Gyugyi (Nvidia)
- Robert Hays (Intel)
- Adam Healey (LSI)
- Brian Murray (LSI)
- Mario Träber (Infineon)

Purposes

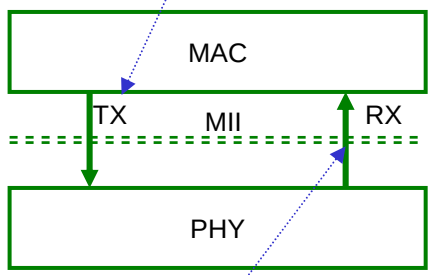
- Support LPI based EEE proposal
- Review the signaling between MAC and PHY interfaces of LPI 100Base-TX and 1000Base-T
- Save as much power as possible on MII/GMII Interfaces by **optionally halting the clock**.
- Meet the EEE state transition time requirement.
- Minimum modification to existing Standard.

Signals between MAC and PHY (MII)

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

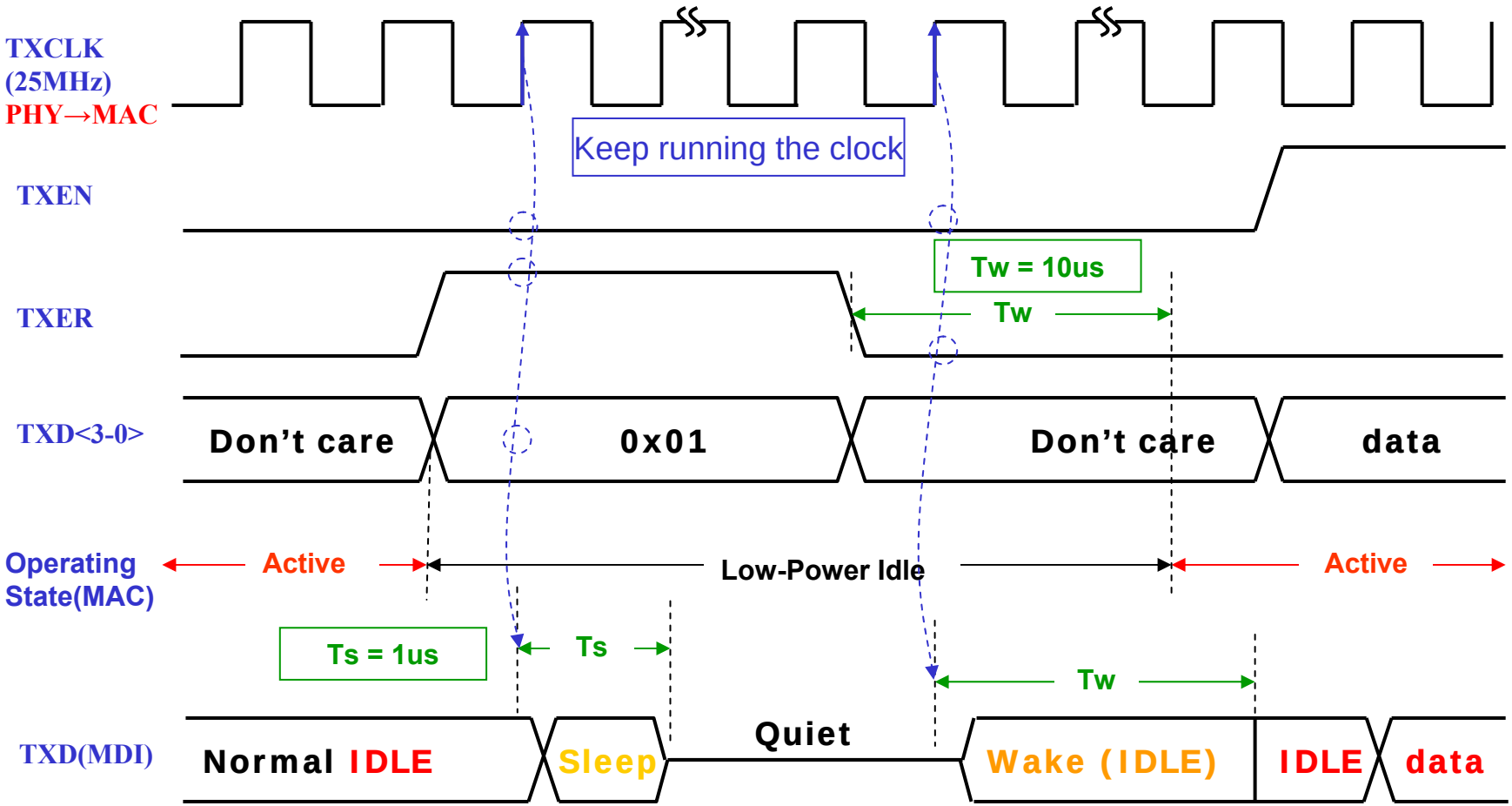
EEE_LPI Opcode from MAC to PHY



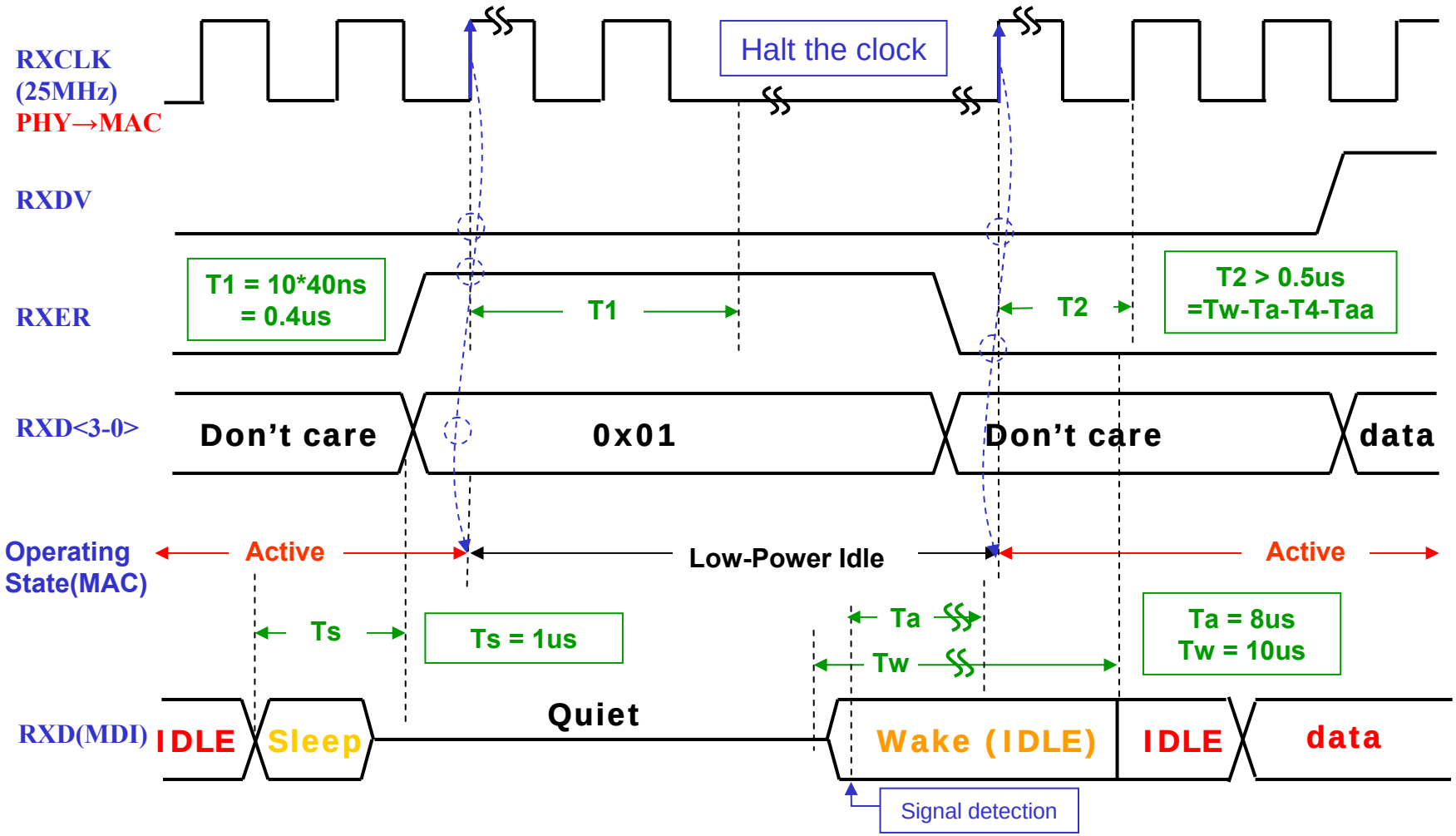
EEE_LPI Opcode from PHY to MAC

Note: From 802.3az Task Force Dove_01_0108.pdf

MII Interface – Transmitter Path



MII Interface – Receiver Path

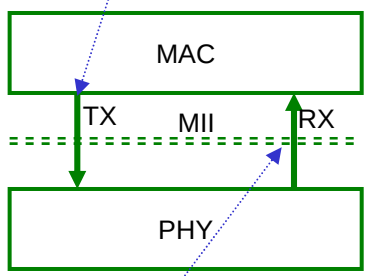


Signals between MAC and PHY (GMII)

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Low Power IDLE	EEE Low Power IDLE
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01	Low Power IDLE	EEE Low Power IDLE
0	1	02 through 0D	Reserved	—

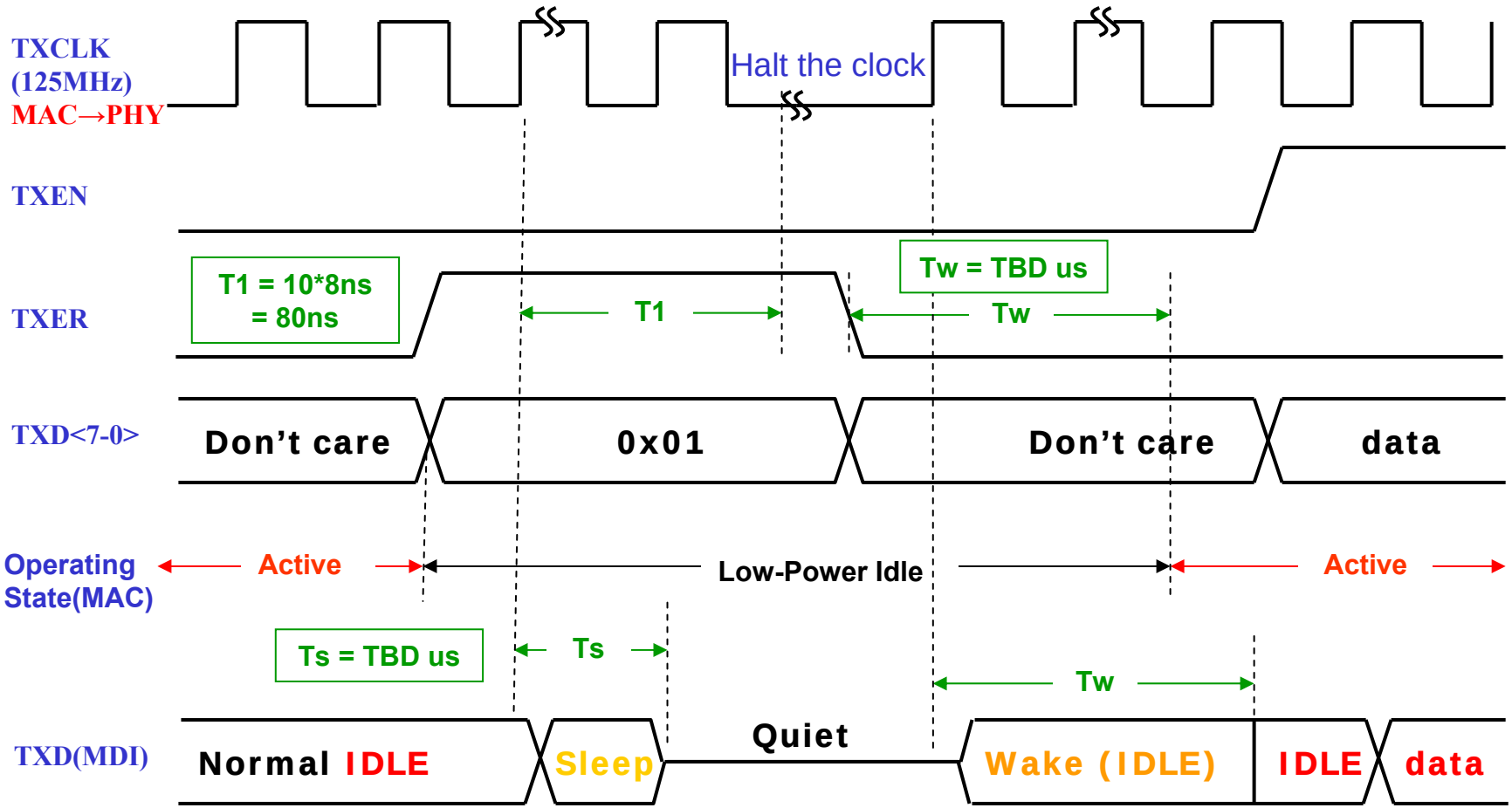
EEE_LPI Opcode from MAC to PHY



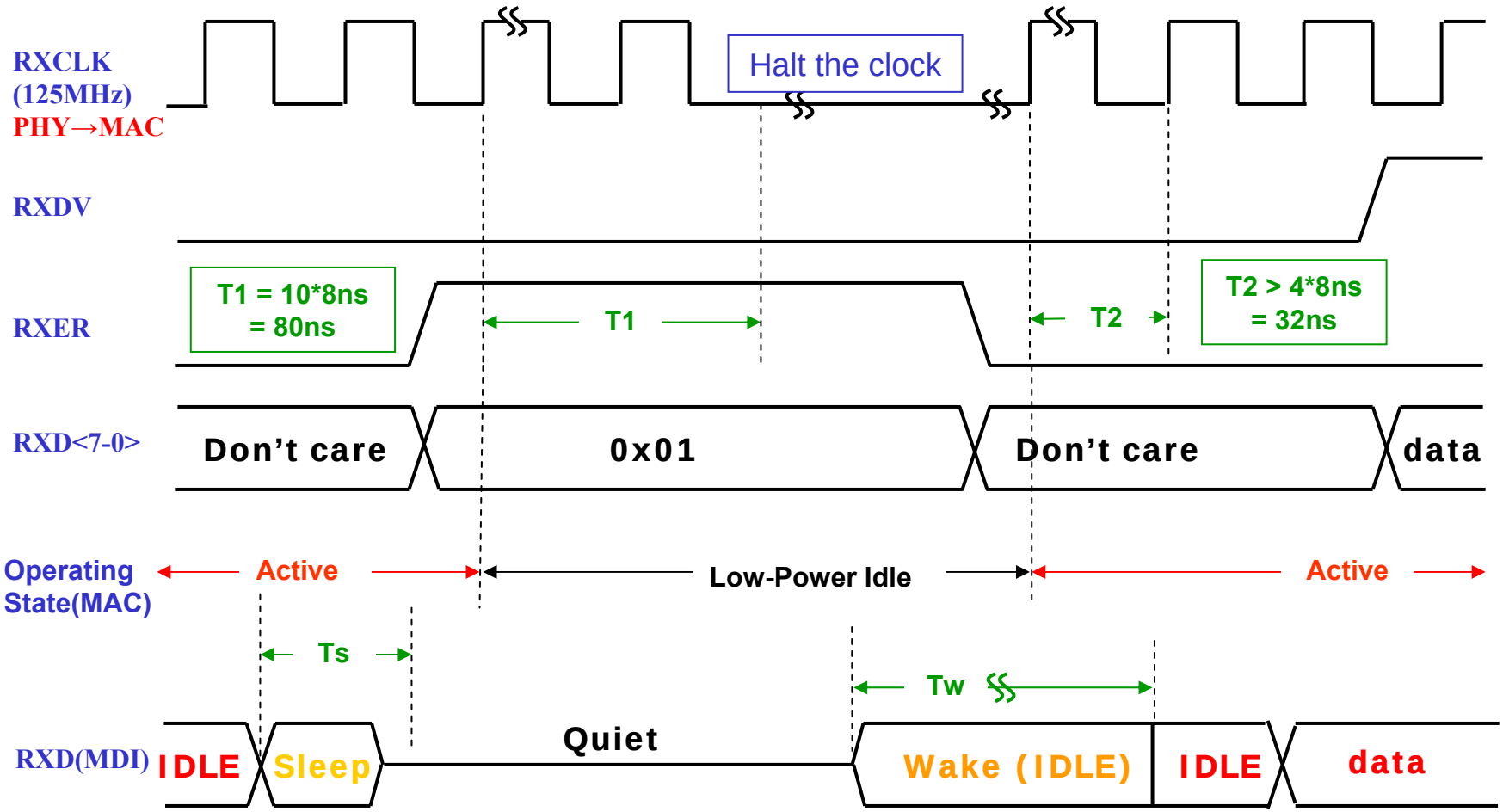
EEE_LPI Opcode from PHY to MAC

Note: From 802.3az Task Force Dove_01_0108.pdf

GMII Interface – Transmitter Path



GMII Interface – Receiver Path



Estimated Power Saving and Option

Power consumption: Each clock pin consumes as much as 6mW to 25mW at 3.3V I/O power supply depending on the loading.

- For MII interface
  - Only RXCLK can be turned off
    ➔ saves 6~25mW
- For GMII interface
  - Both RXCLK and TXCLK can be turned off
    ➔ saves 12~50mW

Option: Is it a mandatory or optional capability?

Thank you

Questions?

Straw Poll

- Do you support halting clocks of MII and GMII interfaces during Low Power Idle operating state to save more power?

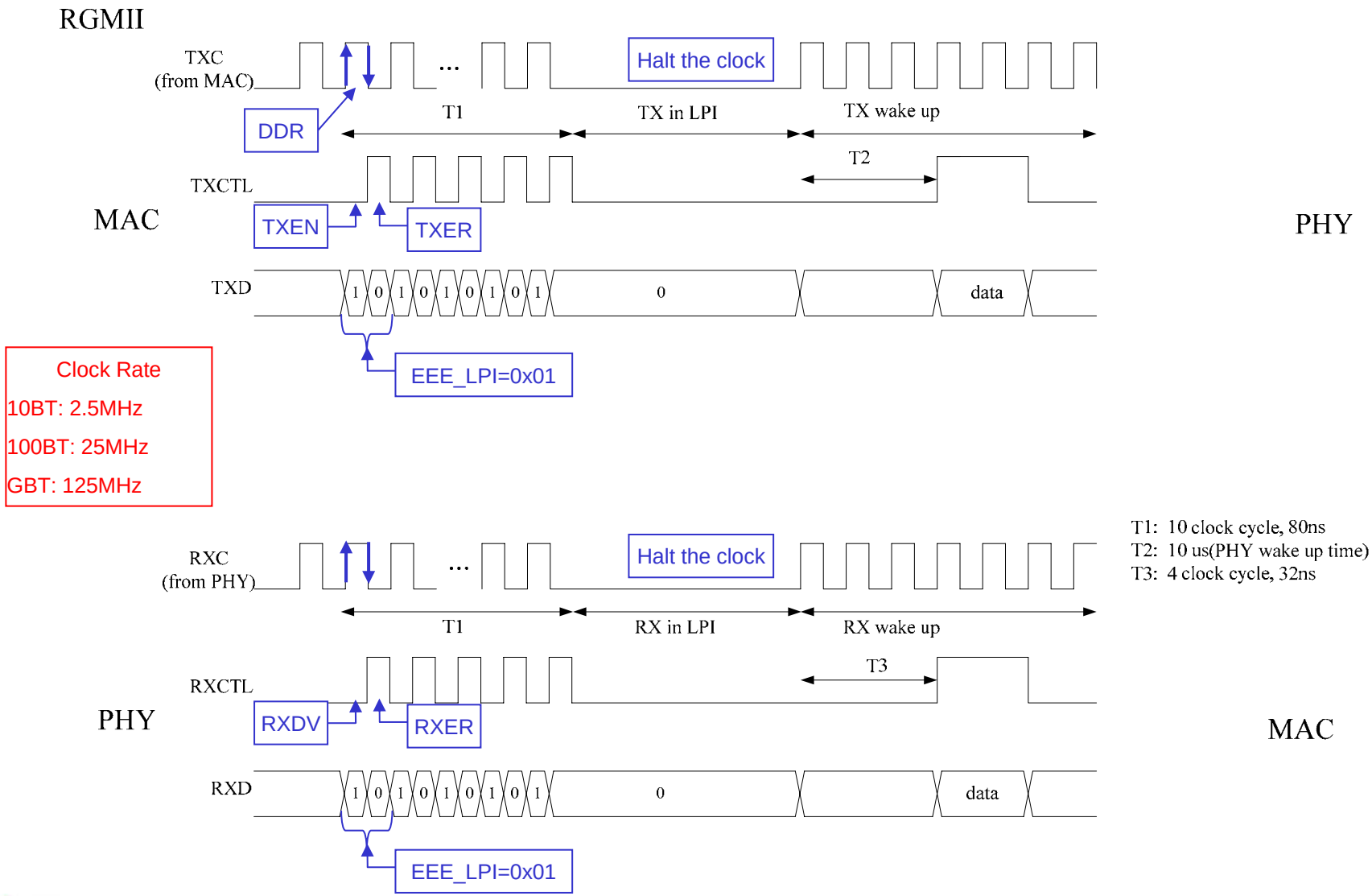
YES:

NO:

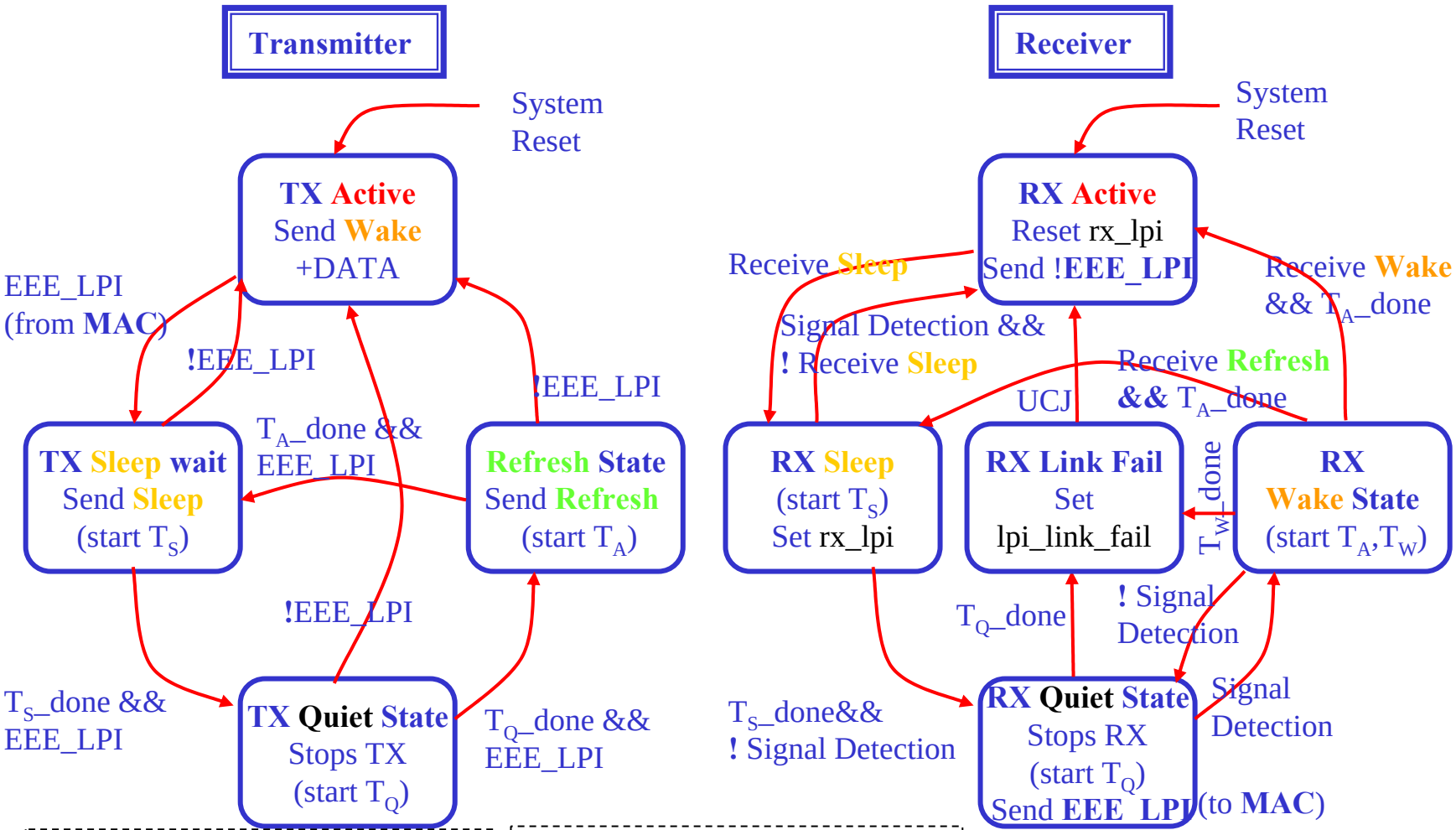
ABSTAIN:

Backup

RGMII Interface



100BT LPI Line State Diagrams (PHY)

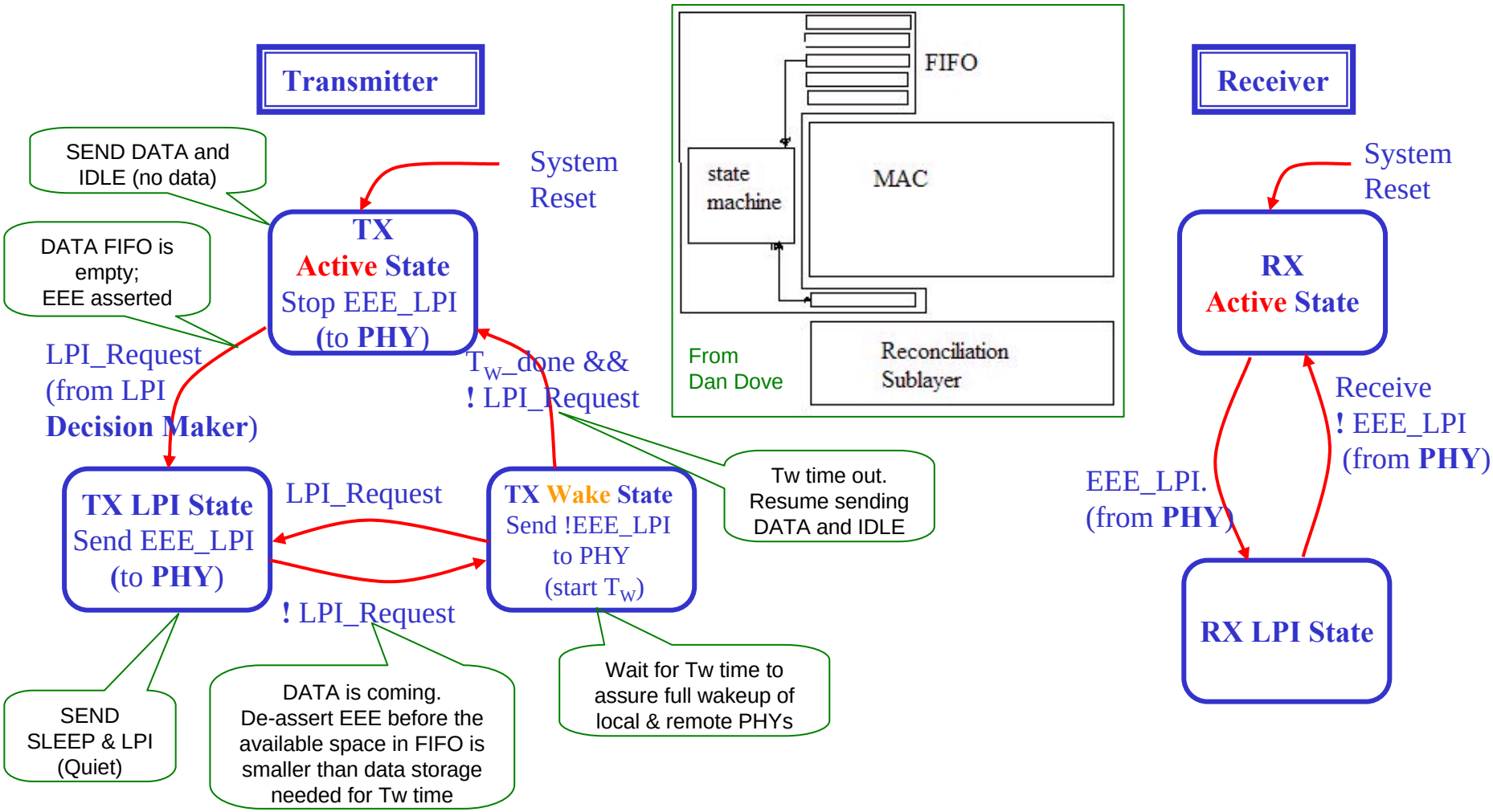


Note: Addition to Figure 24-8 Transmitter state diagram

Note: RX_LPI, LPI_Link_fail, new signals for Figure 24-15 Link_monitor State Diagram

Note: Addition to Figure 24-11 Receiver state diagram

100BT LPI Operating State Diagrams (above PHY)



Note: New EEE state diagrams