

EEE Compatible MII/GMII Interface (revised)

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Supporters

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- ❑ Mandeep Chadha (Vitesse)
- ❑ Dan Dove (ProCurve Networking by HP)
- ❑ Paul Gyugyi (Nvidia)
- ❑ Robert Hays (Intel)
- ❑ Adam Healey (LSI)
- ❑ Brian Murray (LSI)
- ❑ Mario Träber (Infineon)

Purposes

Revised version of chou_02_0508 :

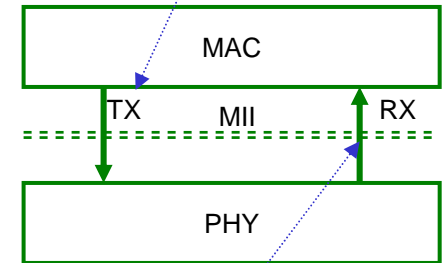
- ☐ Insert one cycle of clock before the end of LPI operating state
- ☐ Add MII registers to control the option to turn on and off interface clocks

Signals between MAC and PHY (MII)

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	EEE Low Power IDLE
0	1	0010 through 1111	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

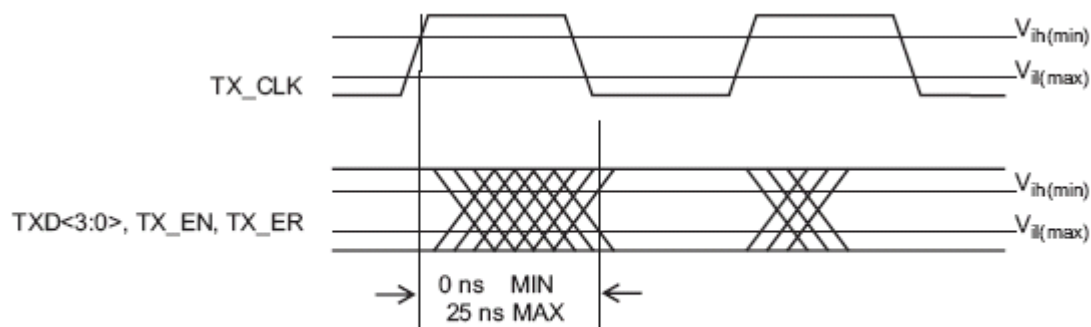
EEE_LPI
Opcode from
MAC to PHY



EEE_LPI
Opcode from
PHY to MAC

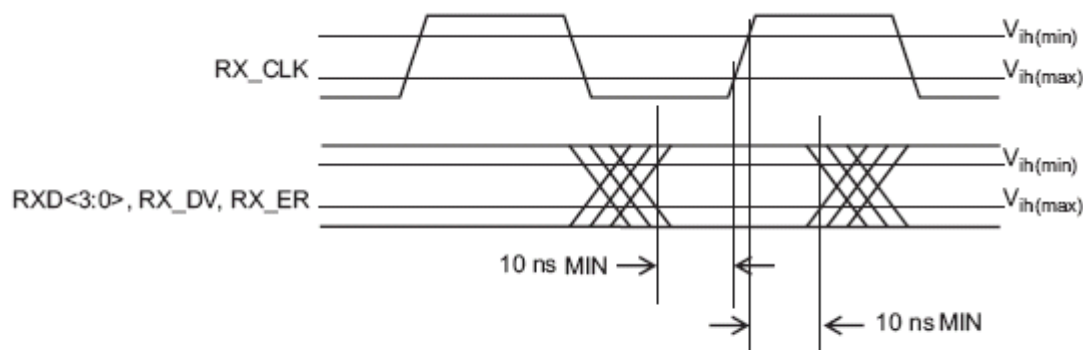
Note: From 802.3az Task Force Dove_01_0108.pdf **Clause 22**

Signal timing relationships at the MII



TX_CLK is not halted during LPI state

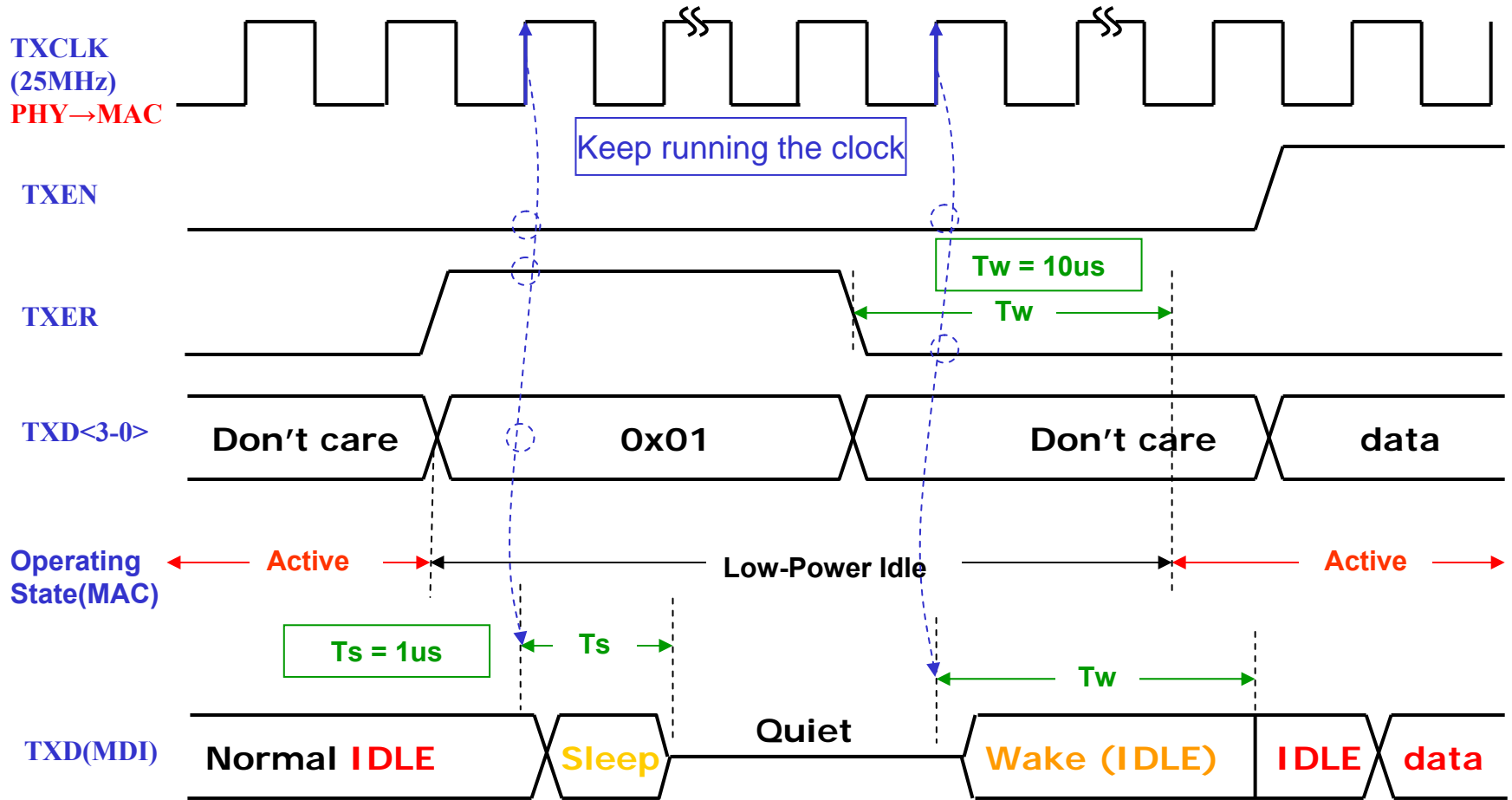
Figure 22-14—Transmit signal timing relationships at the MII



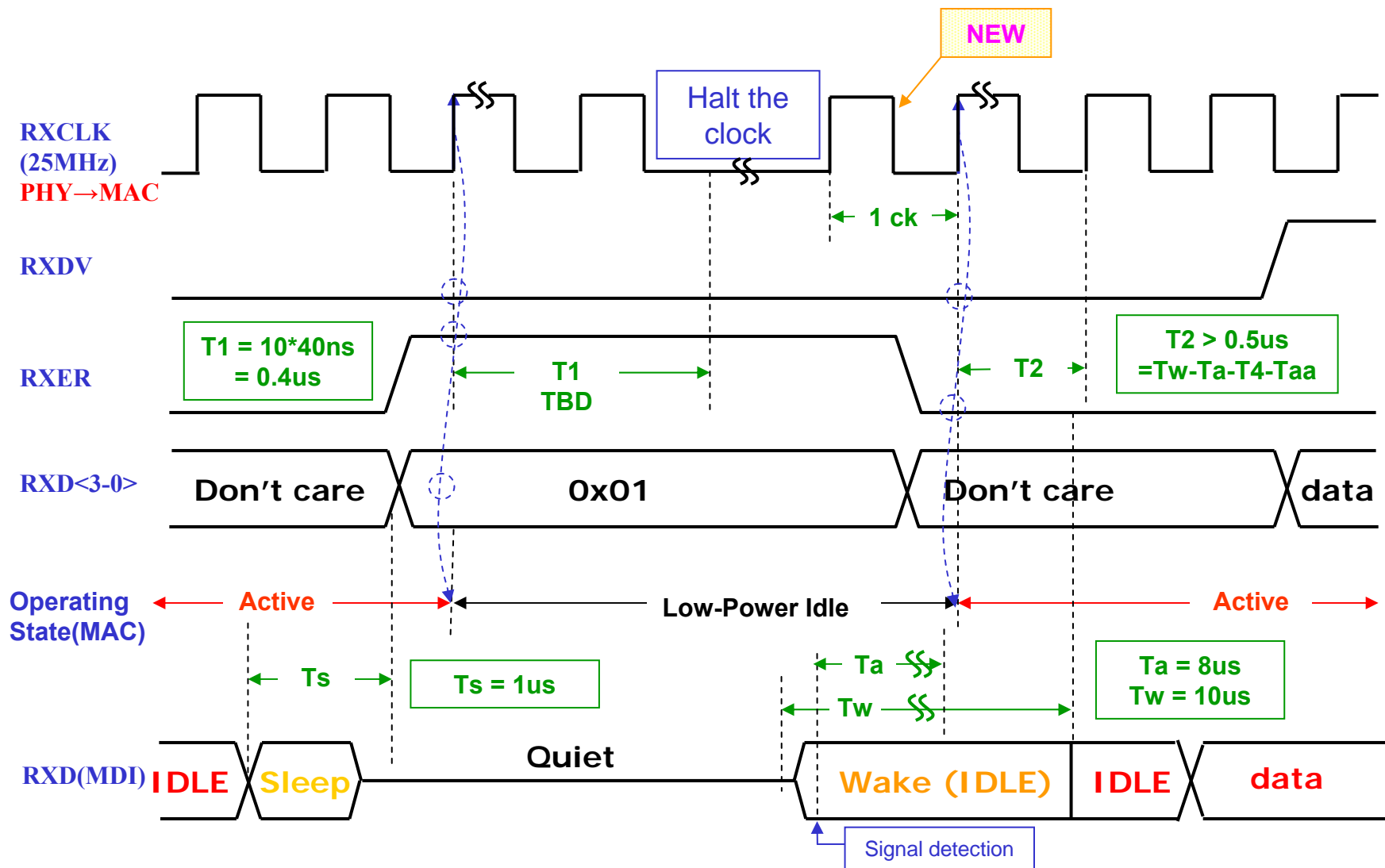
Only setup time and hold time defined w.r.t. the rising edge of RX_CLK

Figure 22-15—Receive signal timing relationships at the MII

MII Interface – Transmitter Path



MII Interface – Receiver Path

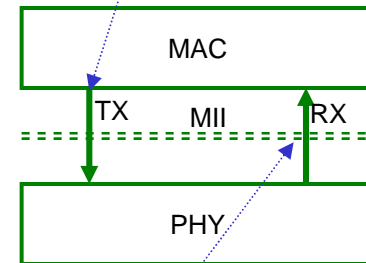


Signals between MAC and PHY (GMII)

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Low Power IDLE	EEE Low Power IDLE
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01	Low Power IDLE	EEE Low Power IDLE
0	1	02 through 0D	Reserved	—

EEE_LPI
Opcode from
MAC to
PHY



EEE_LPI
Opcode from
PHY to MAC

Note: From 802.3az Task Force Dove_01_0108.pdf

Clause 35

Signal timing relationships at the GMII

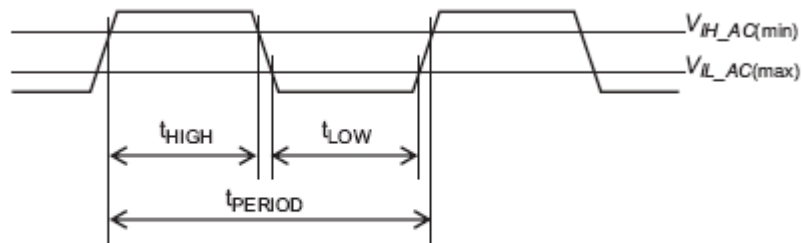
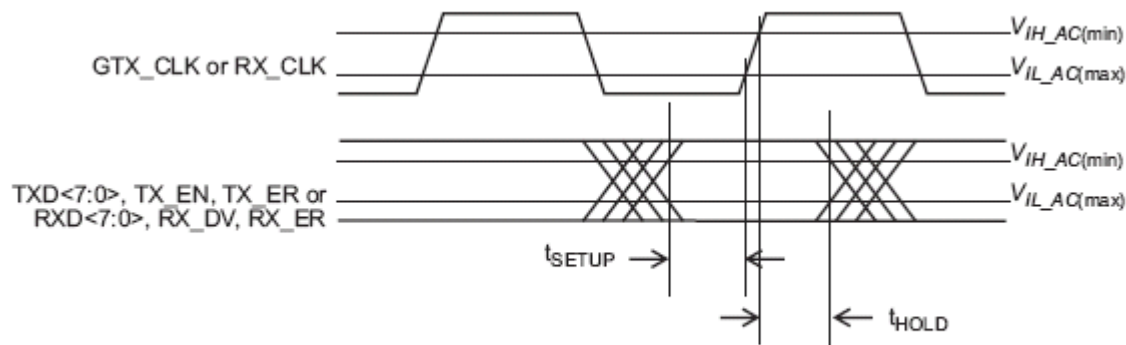


Figure 35-17—GTX_CLK and RX_CLK timing parameters at receiver input

f_{FREQ}	GTX_CLK Frequency	—	125 – 100 ppm	125 + 100 ppm	MHz
t_{PERIOD}	GTX_CLK Period	—	7.50	8.50	ns
t_{PERIOD}	RX_CLK Period	—	7.50	—	ns
t_{HIGH}	GTX_CLK, RX_CLK Time High	—	2.50	—	ns
t_{LOW}	GTX_CLK, RX_CLK Time Low	—	2.50	—	ns

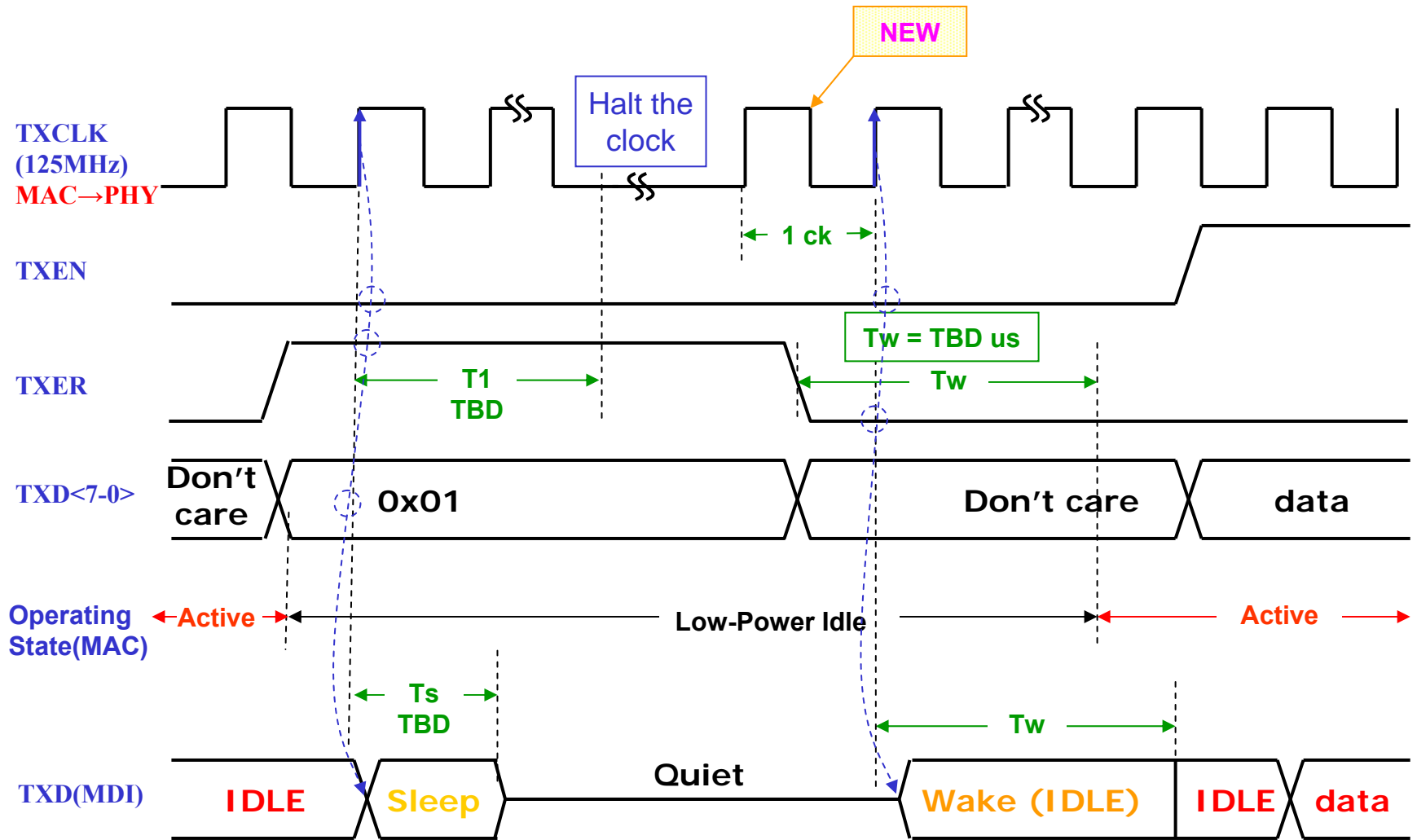
Needs to
modify



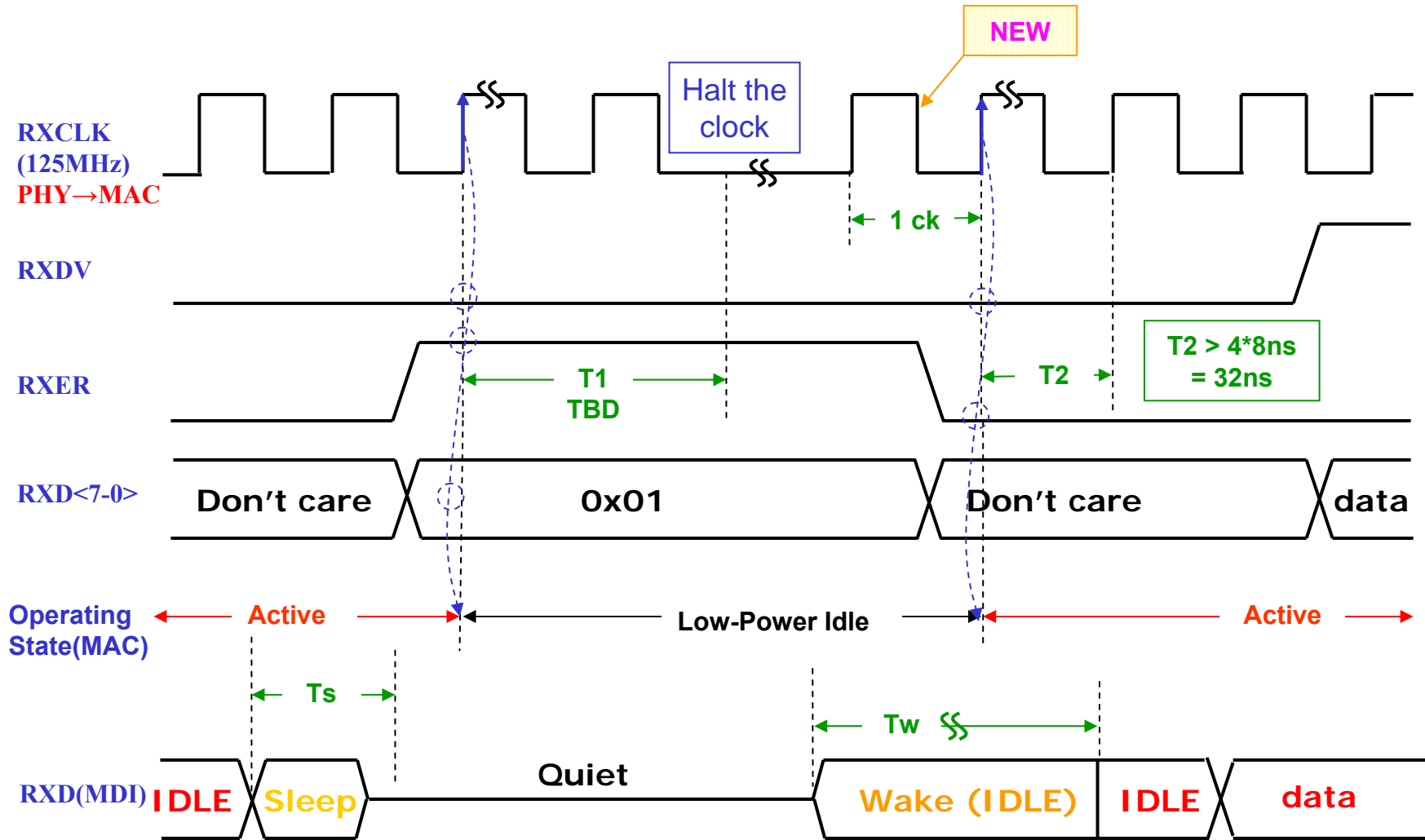
Only setup time
and hold time are
defined w.r.t. the
rising edge of
GTX_CLK and
RX_CLK

Figure 35-19—GMII signal timing at receiver input

GMII Interface – Transmitter Path



GMII Interface – Receiver Path



Estimated Power Saving and Option

Power consumption: Each clock pin consumes as much as 6mW to 25mW at 3.3V I/O power supply depending on the loading.

❑ For MII interface

- Only RXCLK can be turned off
➔ saves 6~25mW

❑ For GMII interface

- Both RXCLK and TXCLK can be turned off
➔ saves 12~50mW

Propose

- ❑ Optionally halt the following clocks during Low Power Idle state:

- RXCLK (from PHY to MAC) for MII interface
- TXCLK (from MAC to PHY) for GMII interface
- RXCLK (from PHY to MAC) for GMII interface

NEW

- ❑ Define new MII registers to enable or disable the on/off capability of MII/GMII clocks

- One control register (R/O) for TXCLK (for GMII)
- One control register (R/W) for RXCLK (for MII, GMII)

Thank you

Questions?

Backup

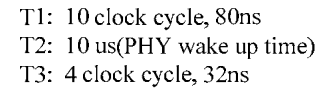
Straw Poll

- ☐ Do you oppose halting clocks of MII and GMII interfaces during Low Power Idle operating state to save more power? (5/13/2008, 5 pm, Munich)

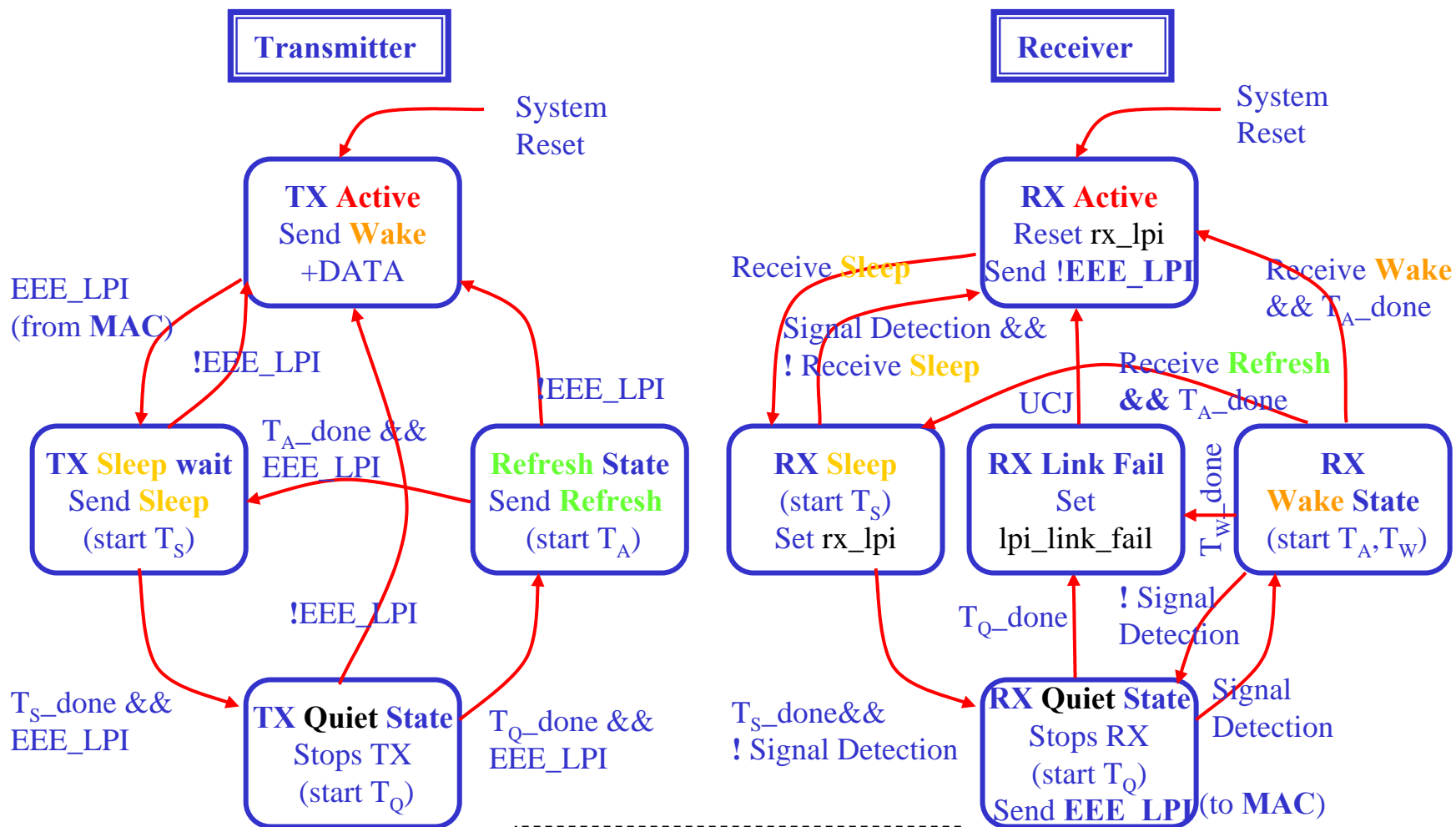
YES: 1

NO: 16

ABSTAIN: 3



100BT LPI Line State Diagrams (PHY)



Note: Addition to Figure 24-8 Transmitter state diagram

Note: RX_LPI, LPI_Link_fail, new signals for Figure 24-15 Link_monitor State Diagram

Note: Addition to Figure 24-11 Receiver state diagram

100BT LPI Operating State Diagrams (above PHY)

