Making EEE GPHY more robust on corner cases

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IEEE 802.3az Task Force

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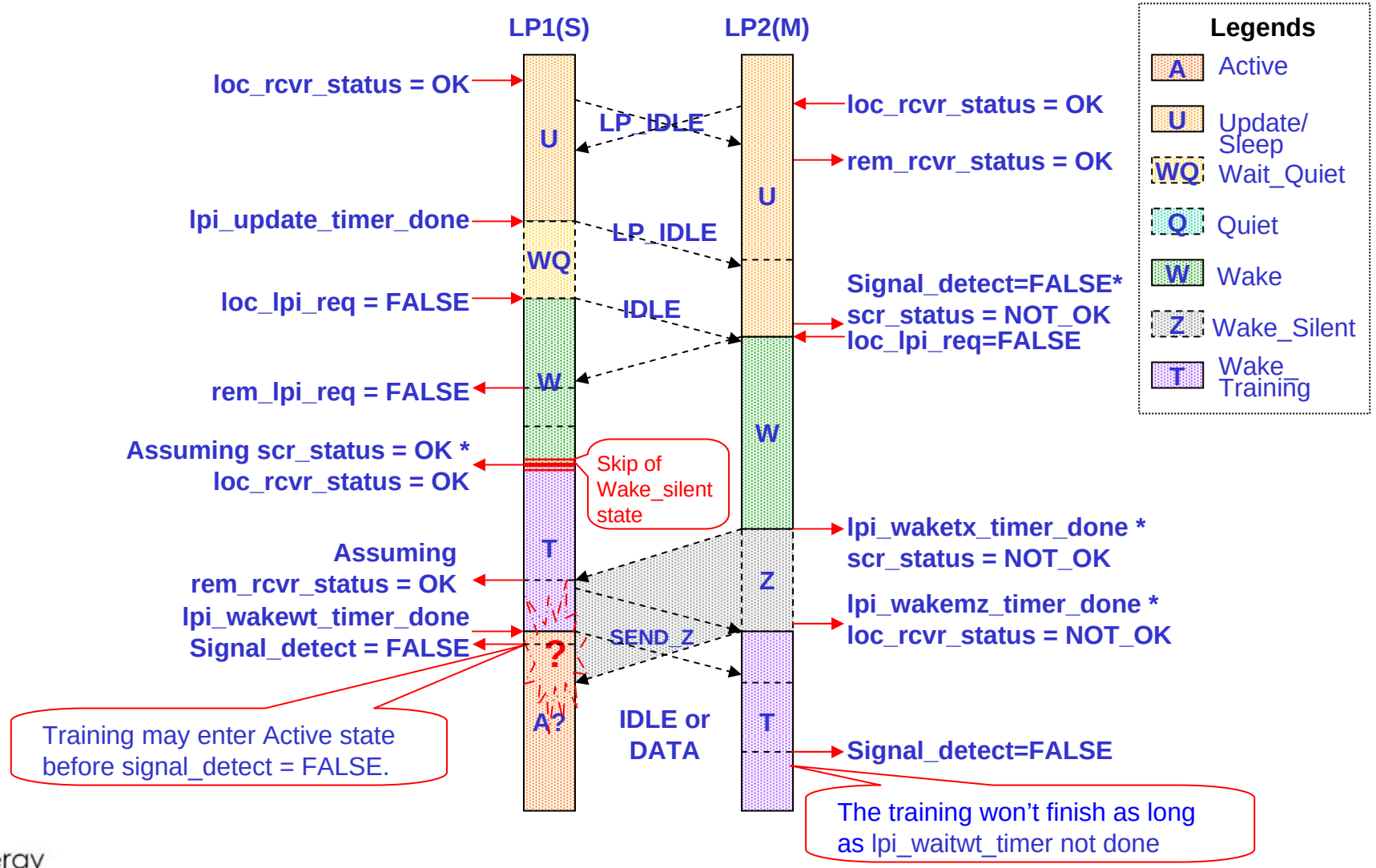
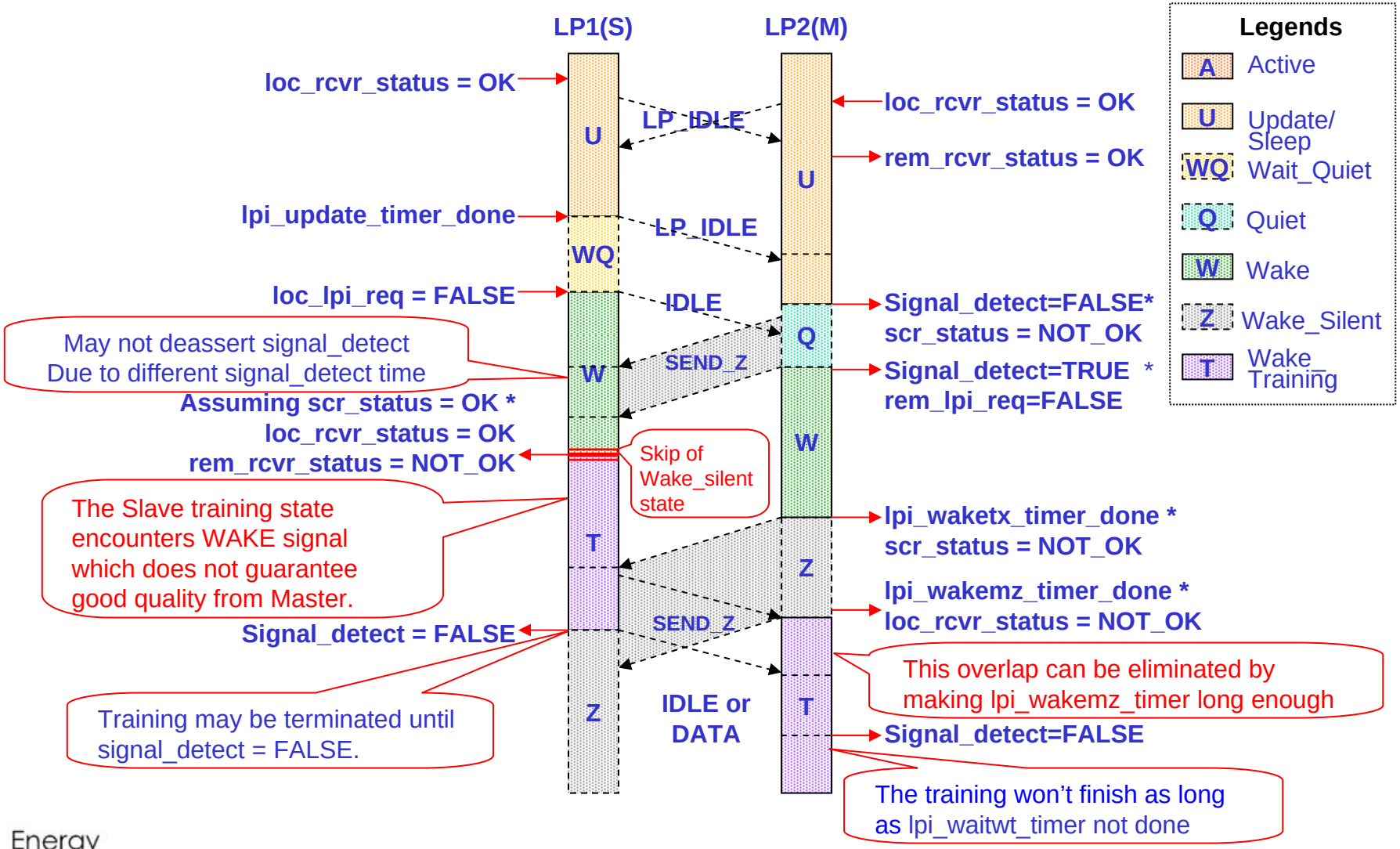
Motivations: LPI states out of sync

- The spirit of EEE GPHY state transitions is to mimic the cold start of GPHY link with shorter timer value so that the local and remote sites, either Master or Slave, can maintain synchronization of training states to complete the appropriate CDR loop.
- However, either party of an EEE link segment can exit any intermediate state and accelerate the transition of rest of states resulting in possible loss of state synchronization due to the round trip delay of signal exchanged and implementation dependent logic delay of generating a local signal or processing a remote signal .
- During the acceleration of state transition, the skip of WAKE_SILENT state (which is similar to Slave_Silent state in non-EEE standard) and improper setting of timer value may cause the Slave device to move to Active state prematurely.
- Furthermore, in another case, the Slave device may enter Training state while it is still receiving Master WAKE signal which may not have good quality.

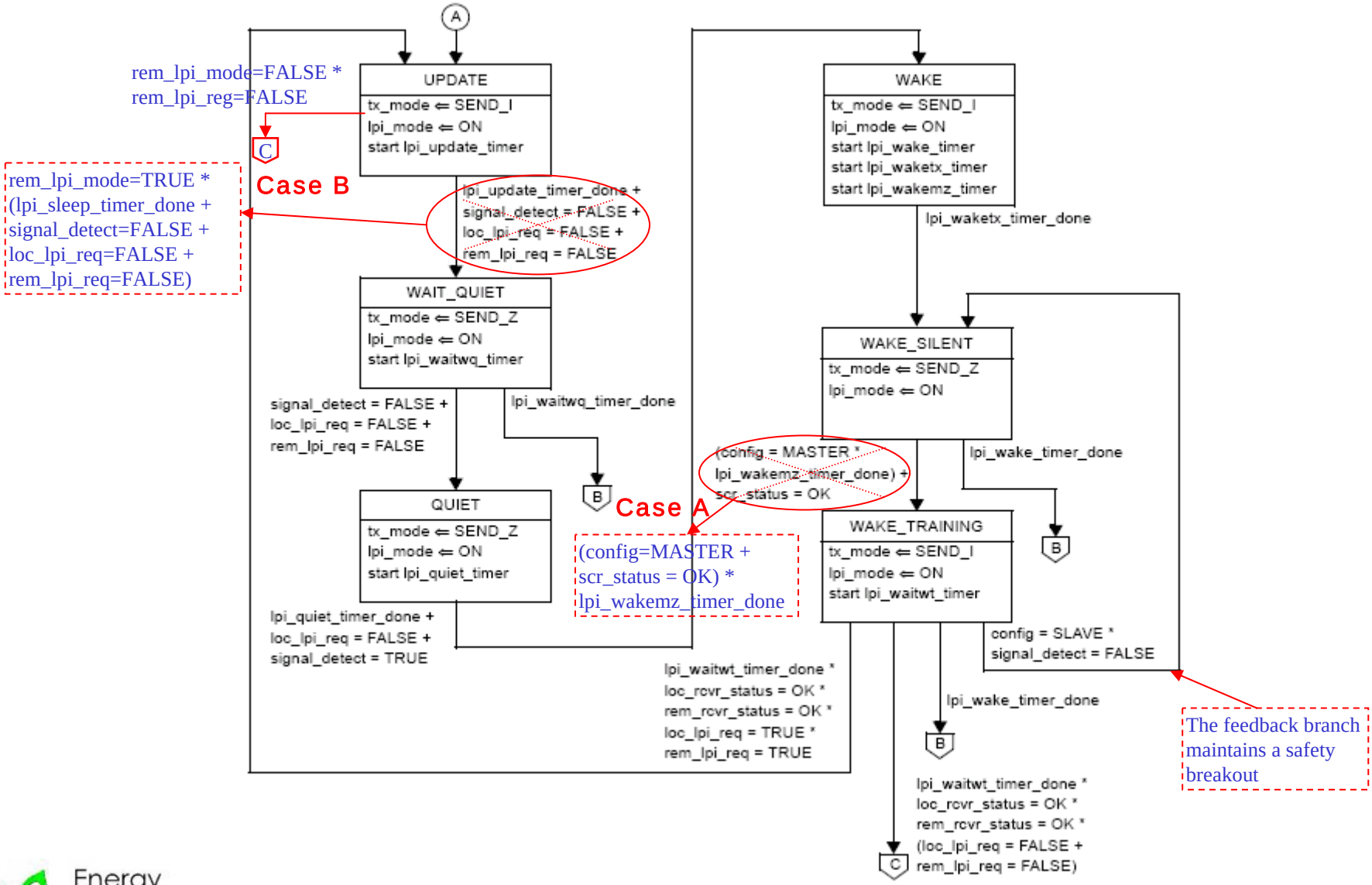
Case 1 : Slave enters Active state prematurely



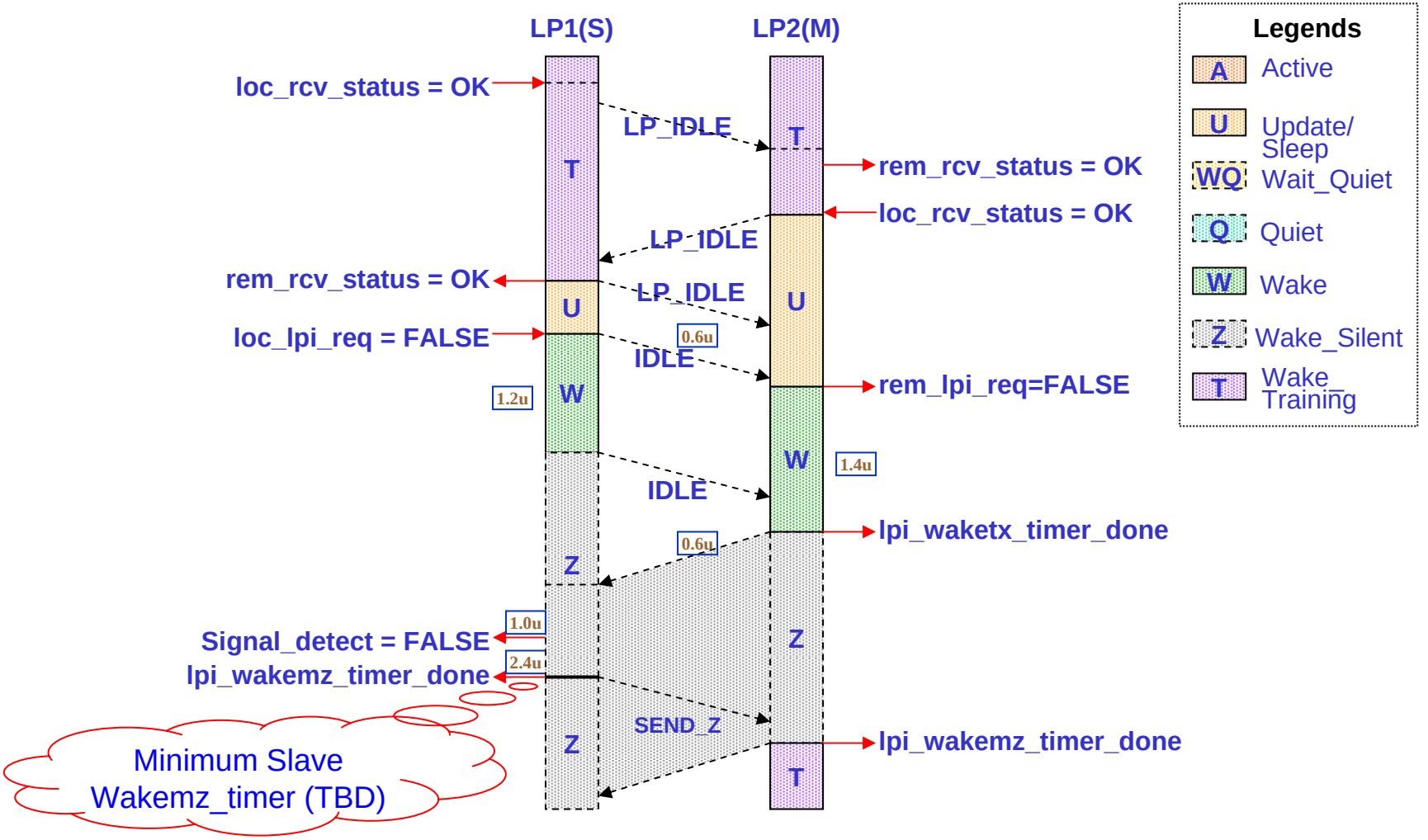
Case 2 : Slave training encounters unstable WAKE signal (from Xiaotong Lin)



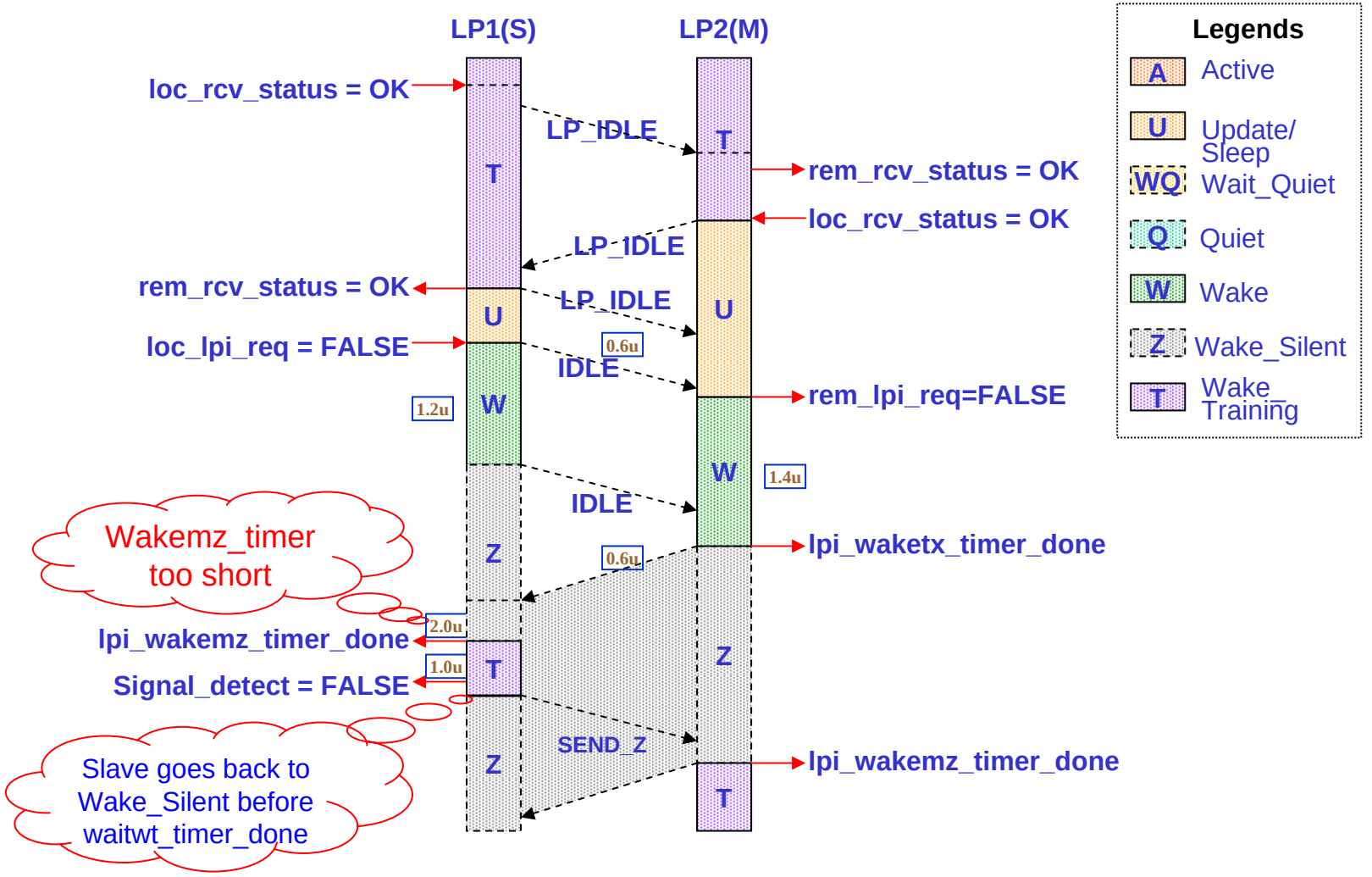
Suggested modifications of Fig 40-15b



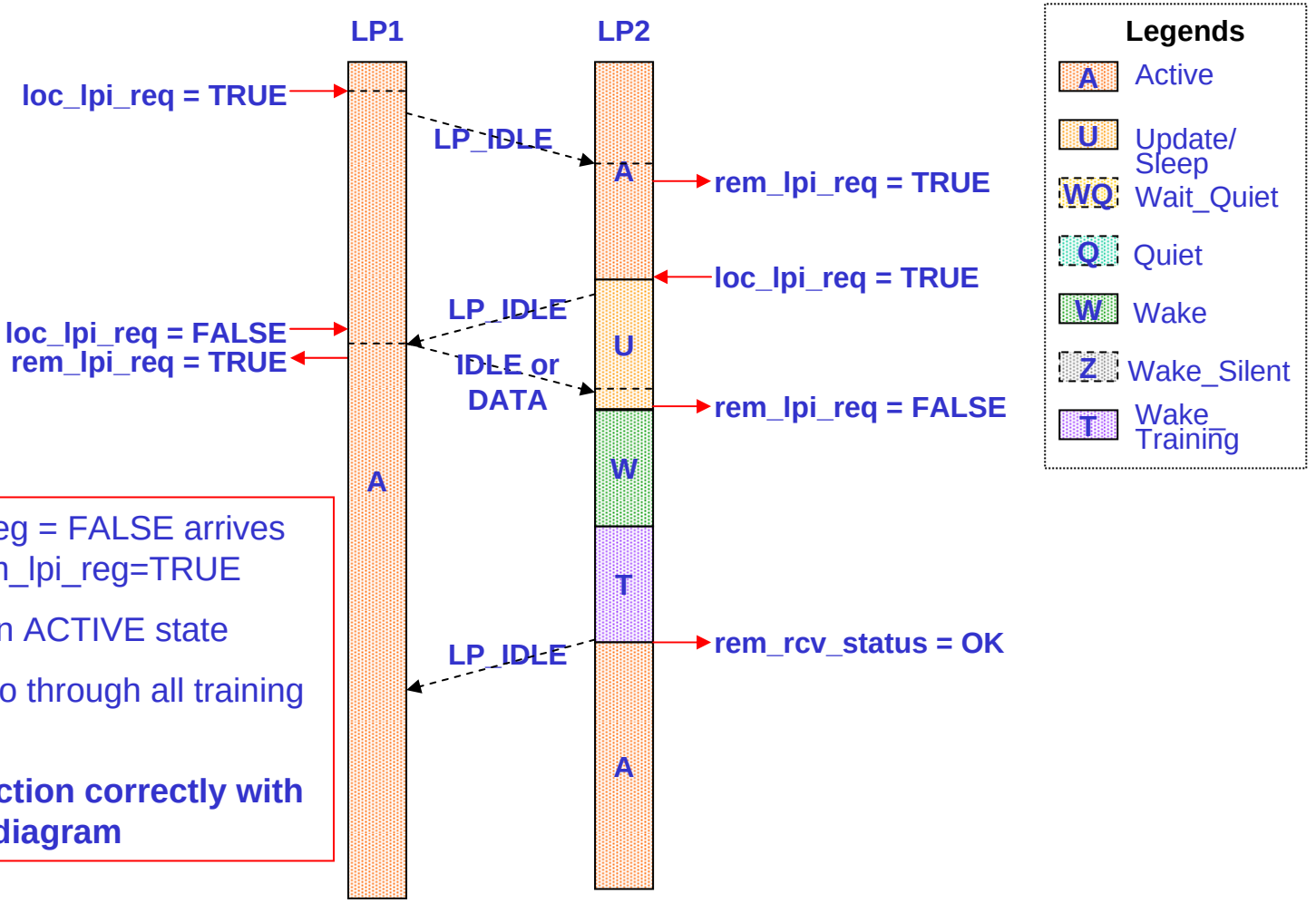
Example with state diagram modification – Case A



Example with state diagram modifications – Case A (cont)



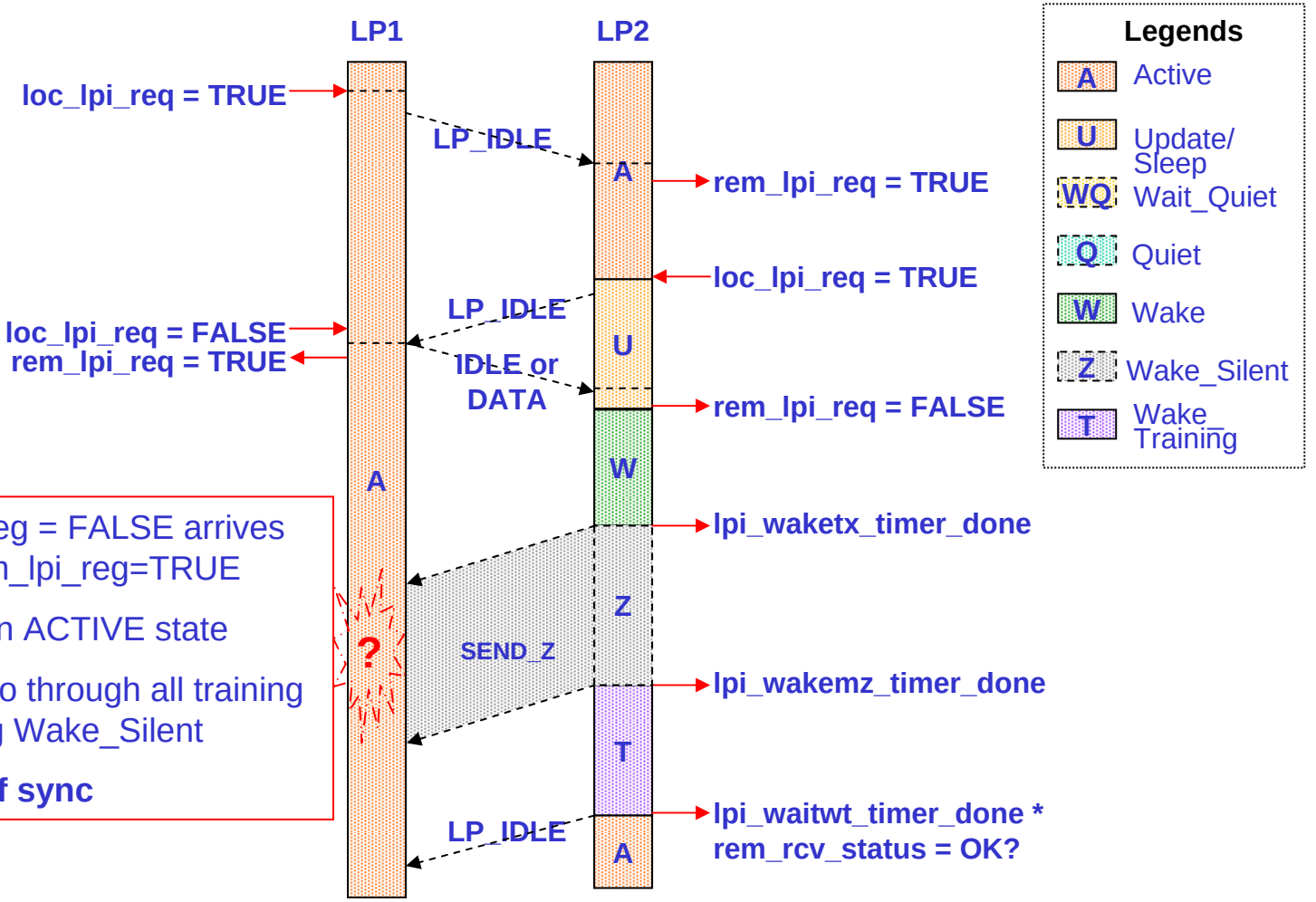
Example before state diagram modification – Case B



1. LP1's loc_lpi_reg = FALSE arrives right before rem_lpi_reg=TRUE
2. LP1 is always in ACTIVE state
3. LP2 needs to go through all training states

➔ **LP1 and LP2 function correctly with original state diagram**

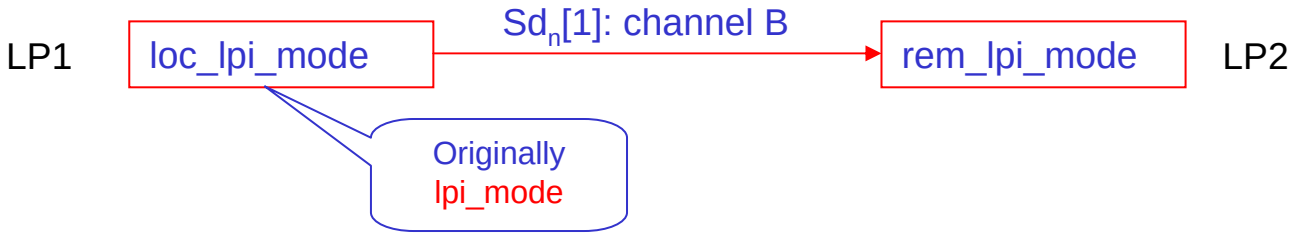
Example of Case B: Revisit with Case A modification only



1. LP1's loc_lpi_reg = FALSE arrives right before rem_lpi_reg=TRUE
2. LP1 is always in ACTIVE state
3. LP2 needs to go through all training states including Wake_Silent

➔ **LP1 will be out of sync**

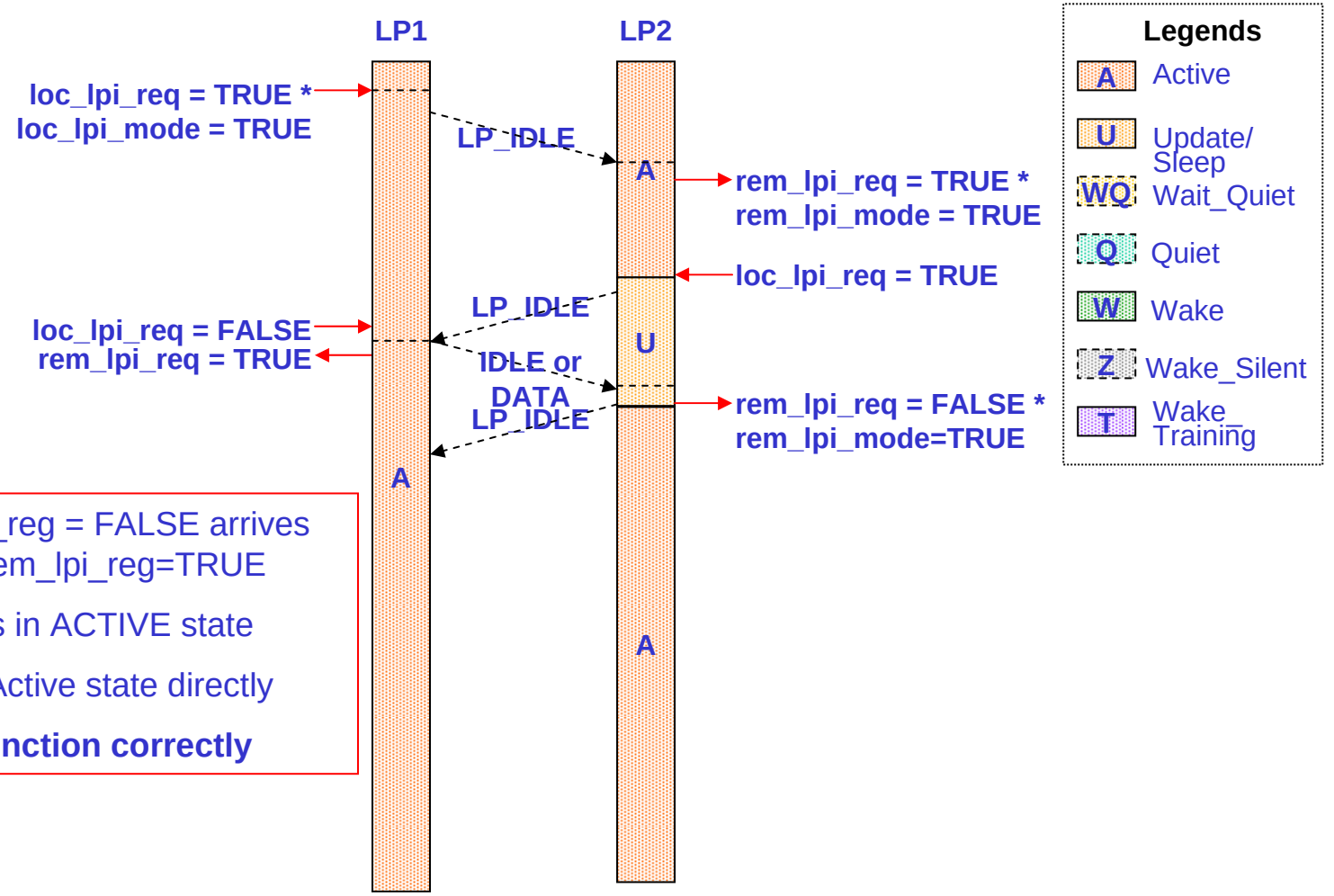
The need to encode LPI_mode signal in transmitted symbols



$Sd_n[1]$ = { $Sc_n[1]$ ^$TXD_n[1]$, if(tx_enable_{n-2}=1)
{ $Sc_n[1]$^ $cext\_err_n$,else if

$cext\_err_n$ = { tx_error_n if(tx_enable_n=0 *$TXD_n[7:0]$)≠0x0F *$TXD_n[7:0]$)≠0x01)
{ 1 , if(loc_lpi_mode=TRUE *tx_mode ≠SEND_Z)
{ 0, else

Example of Case B: Revisit with both Case A & Case B modifications



1. LP1's loc_lpi_reg = FALSE arrives right before rem_lpi_reg=TRUE
2. LP1 is always in ACTIVE state
3. LP2 exits to Active state directly

➔ **LP1 and LP2 function correctly**

Summary

- The corner cases of EEE GPHY which are caused by round trip signal delay and undefined logic delay of implementation are getting harder to identify.
- The enforcement of WAKE_SILENT state and proper setting of timer values can prevent those corner cases.
  ➔ Case A of Slide 4
- The rem_lpi_mode signal conveyed in data stream can avoid the SEND_Z to an Active state and also shorten the delay of state transition when one party is in Active state while the other wants to exit from Update state. setting of timer values can prevent those corner cases.
  ➔ Case B of Slide 4
- The proposed modifications are minimal yet making the state diagram more robust.

Thank You