

IEEE P802.3az/D1.0 Clause 40 Ipi_mode Encoding

Presented by: Mike Grimwood, Broadcom

Contributors: Xiaotong Lin, Peiqing Wang

IEEE P802.3az Task Force

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Contributors and Supporters

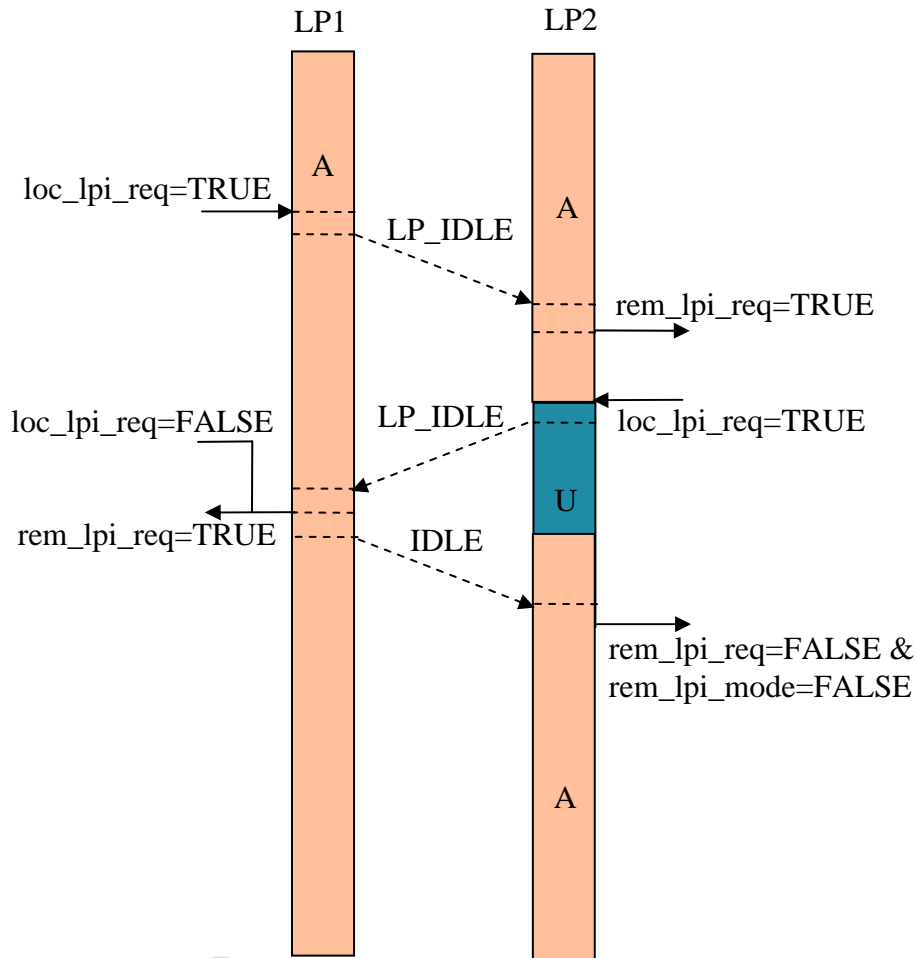
- Joseph Chou, Realtek
- Xiaotong Lin, Broadcom
- Peiqing Wang, Broadcom



Overview

- The presentation, `chou_01_1108.pdf`, proposes two changes to the state diagram:
 - “CASE A”: Enforcement of WAKE_SILENT during the Wake-up process.
 - “CASE B”: Use of *rem_lpi_mode* and associated state transitions to avoid sending zeros to an active link partner.
- This presentation proposes a mechanism for encoding *loc_lpi_mode* (related to CASE B).

Exception Case Requiring Special Handling - Ipi_mode Encoding



- Enforcement of WAKE_SILENT results in a corner case in which zeros may be sent to an active link partner.
- To avoid this case, if `rem_lpi_mode = FALSE` and `rem_lpi_mode = FALSE`, then a transition is made from Update directly to Active.
- Requires a mechanism for encoding `rem_lpi_mode`.

Summary of Proposed PCS Encoding

Pairs ($Sd_n[k]$)	802.3-2005 Encoding	802.3az D1.0 Encoding	Proposed EEE Encoding	
A & B ($Sd_n[0]$ and $Sd_n[1]$)	$cext_n$, $cext_err_n$	$cext_n$, $cext_err_n$	$cext_n$, $cext_err_n$, <i>loc_lpi_req</i>	} MAC- based control
C ($Sd_n[2]$)	loc_rcvr_status	loc_rcvr_status	loc_rcvr_status	
D ($Sd_n[3]$)	----	<i>loc_lpi_req</i>	<i>lpi_mode</i>	} PHY- based control



802.3-2005 PCS Encoding of $cext_n$ and $cext_err_n$ into $Sd_n[1]$ and $Sd_n[0]$

$$cext_n = \begin{cases} tx_error_n & \text{if } ((tx_enable_n = 0) \text{ and } (TXD_n[7:0] = 0x0F)) \\ 0 & \text{else} \end{cases}$$

$$cext_err_n = \begin{cases} tx_error_n & \text{if } ((tx_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0x0F)) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[1] \wedge cext_err_n & \text{else} \end{cases}$$

$$Sd_n[0] = \begin{cases} Sc_n[0] \wedge TXD_n[0] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[0] \wedge cext_n & \text{else} \end{cases}$$

	$cext_n$	$cext_err_n$
$tx_enable_n = 0$ * $tx_error_n = 1$ * $TXD_n[7:0] = 0x0F$	1	0
$tx_enable_n = 0$ * $tx_error_n = 1$ * $TXD_n[7:0] \neq 0x0F$	0	1
$tx_enable_n = 1$ + $(tx_enable_n = 0$ * $tx_error_n = 0$ * $TXD_n[7:0] = 0x00 \sim 0xFF)$	0	0



Proposed PCS Encoding of $cext_n$, $cext_err_n$, and loc_lpi_req using $Sd_n[1]$ and $Sd_n[0]$

$$cext_n = \begin{cases} tx_error_n & \text{if } (((tx_enable_n = 0) \text{ and } ((TXD_n[7:0] = 0x0F) \text{ or } ((TXD_n[7:0] = 0x01) \text{ and } (tx_mode \neq SEND_Z)))) \\ 0 & \text{else} \end{cases}$$

$$cext_err_n = \begin{cases} tx_error_n & \text{if } (((tx_enable_n = 0) \text{ and } (((TXD_n[7:0] \neq 0x0F) \text{ and } (TXD_n[7:0] \neq 0x01)) \text{ or } ((TXD_n[7:0] = 0x01) \text{ and } (tx_mode \neq SEND_Z)))) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[1] \wedge cext_err_n & \text{else} \end{cases}$$

$$Sd_n[0] = \begin{cases} Sc_n[0] \wedge TXD_n[0] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[0] \wedge cext_n & \text{else} \end{cases}$$

	$cext_n$	$cext_err_n$
$tx_enable_n=0 * tx_error_n=1$ $* TXD_n[7:0]=0x0F$	1	0
$tx_enable_n=0 * tx_error_n=1$ $* TXD_n[7:0] \neq 0x0F *$ $TXD_n[7:0] \neq 0x01$	0	1
$tx_enable_n=0 * tx_error_n=1$ $* TXD_n[7:0]=0x01 *$ $tx_mode \neq SEND_Z$	1	1
$tx_enable_n=1 +$ $(tx_enable_n=0 *$ $tx_error_n=0 *$ $TXD_n[7:0]=0x00 \sim 0xFF)$	0	0



Proposed Encoding of *loc_lpi_mode* using $Sd_n[3]$

$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if } (tx_enable_{n-2} = 1) \\ Sc_n[3] \wedge 1 & \text{elseif } (loc_lpi_mode = ON) \\ Sc_n[3] & \text{else} \end{cases}$$

- *loc_lpi_mode* is a PHY-generated control signal, similar to *loc_rcvr_status* (which uses $Sd_n[2]$)

Summary

- Enforcing WAKE_SILENT during the wake process improves robustness and interoperability.
- A consequence of this enforcement is that a corner case is introduced in which one link partner may send zeros (WAKE_SILENT) to an active link partner.
- By encoding *loc_lpi_mode*, this consequential corner case is avoided.
- This presentation proposes a mechanism for encoding *loc_lpi_mode*.
 - This mechanism involves first encoding *loc_lpi_req* with *cext_n* and *cext_err_n* on Pairs A and B.
 - This frees up Pair D for encoding *loc_lpi_mode*.
- Pair C continues to be used for encoding *loc_rcvr_status*.



Thank you



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Back-up



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GMI Permissible Encodings

(IEEE Draft P802.3az/D1.0, Table 35-1)

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.Request Parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert low power idle	—
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD<7:0> column are hexadecimal.

