10GBASE-T EEE Specifications

Alert

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Alert: Definition, Usage and Desirable Features

➢ Indicates a transition to full speed data mode

➢ Define in the existing framework of 10GBASE-T to avoid:
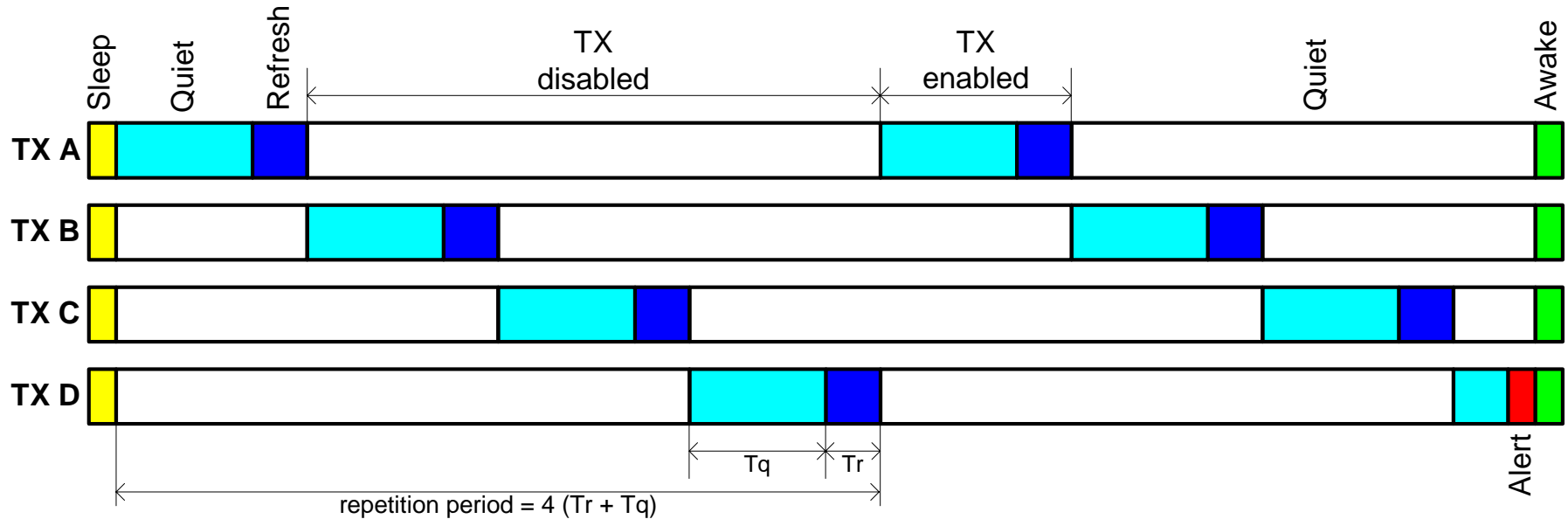
- new signal specification
- new test definition

➢ Specifications should accommodate:

- simple detection with low-power detector implementation
- robust detection to avoid false positives and negatives
- fast detection for rapid return to normal mode

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Transmitter Specifications: Signal Path

➢ Based on Quiet/Refresh proposal in sedarat_02_0908

- Training path: LFSR + PAM2 + THP
- Training LFSR, free running, non-stop
- THP coefficients same as in normal mode
- Transmit power (PBO) and PSD (both magnitude and phase responses) identical to normal mode

➢ Direct sequence spread spectrum (DSSS) encoding of Alert indicator bit (d)

$$d = \begin{cases} 1: & Alert \\ 0: & otherwise \end{cases}$$

LFSR → ⊕ → PAM-2 → THP →

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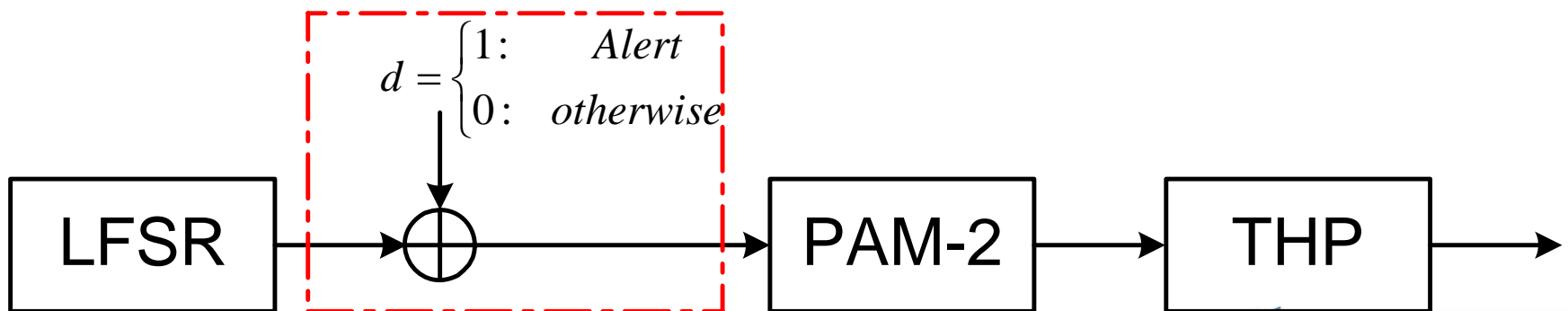
Transmit Specifications: Staggered Signaling

- ➢ Time unit: T = 1 LDPC frame = 256 PAM2 symbols = 320 ns
- ➢ Refresh duration: $T_r = M*T$
- ➢ Quiet duration: $T_q = N*T$
- ➢ Alert duration: $T_a = P*T$

Transmit Specifications: Staggered Signaling

➢ Only one transmitter channel is enabled at a time, alternating in a round-robin fashion

➢ A disabled transmitter is always quiet and may not transmit Alert

➢ Alert is allowed any time while the transmitter is enabled and lasts for P frames

- P < 5 (~1 us) to limit the return time to normal mode
- An Alert occurring at the end of an Enabled interval may be split over 2 channels

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Receiver Considerations

➢ Simplified receiver :
  - No FEXT canceller, 1 FFE
➢ Even simpler when both ends in LPI:
  - No echo canceller, 1 NEXT canceller

➢ Huge SNR margin (>30 dB): low probability of false-positive and false-negative for Alert detection
  - PAM-2 vs. DSQ128: +19 dB
  - 1 bit/frame (P=1): +24 dB
  - No LDPC: -9 dB
➢ Can sacrifice some margin to further simplify receiver even in asymmetric mode

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Summary

➢ DSSS (LFSR) + PAM2 + THP

- No new signal specification (and test definition) needed
- Minimal additional signal processing blocks in the transmit path

➢ Well-understood receive path

- No new hardware blocks
- No synchronization issues

➢ Larger SNR margin: robust, simple and rapid Alert detection

- opportunities to simplify implementation and lower power

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