# Extended Reach via FEC

John Petrilla, Piers Dawe
Avago Technologies
May 29, 2008

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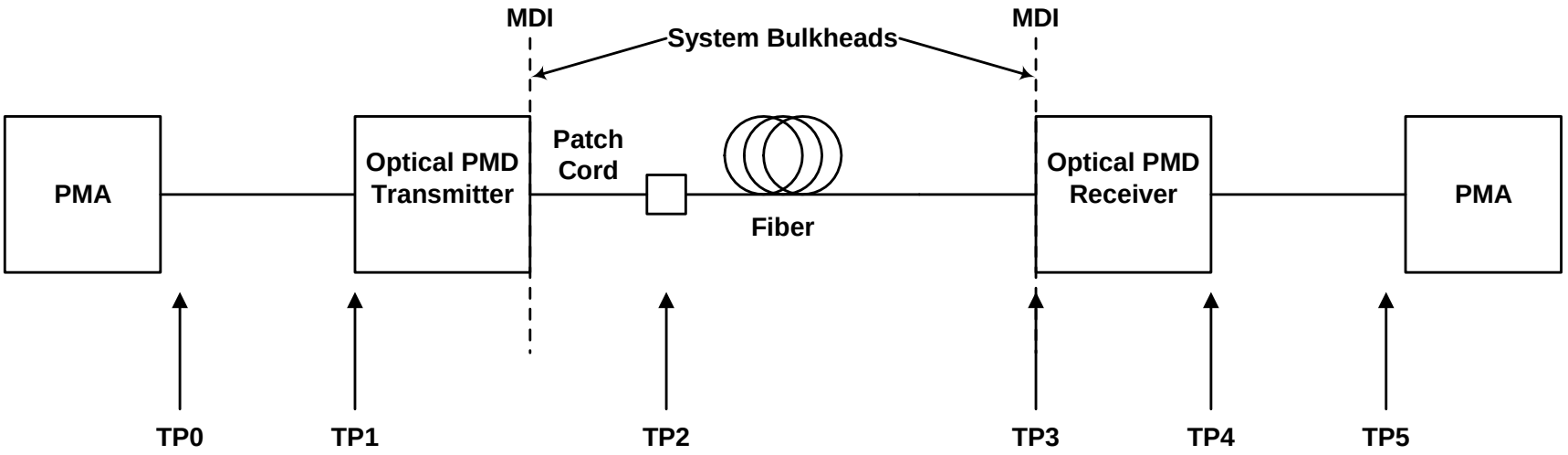
# Overview – Extended Reach

- IEEE 802.3ba has adopted pepeljugoski_01_0508 as the baseline proposal for the first drafts of 40GBASE-SR4 and 100GBASE-SR10 in support of its “at least 100m on OM3 MMF” objective. For applications that may not be adequately supported by an 100 m reach an ad hoc subcommittee was authorized to investigate extended reach options, including enhanced module specifications, addition of CDRs, linear optical receivers with EDC and use of FEC.
- This presentation addresses use of FEC. KR FEC included to support backplane variants, is considered. A comparison of benefits and costs follows. Benefits are shown for extended reach, the primary concern, and jitter allocation made available at TP1 and TP4.
- FEC effectively reopens noisy eyes, providing low BER from degraded SNR. The increase in power consumption for this enhancement can be offloaded from the modules to where it is more readily accommodated.
- KR FEC is expected to correct all single bit errors in the 32 x 64 bit code block (frame) and burst errors of up to 11 bits. Only the effect of single bit error correction is considered.
- Limiting non-retimed optical modules promise the lowest power consumption and lowest cost solution for the 100 m MM variant, sufficient for most data center applications. Extended reach enhancement must be carefully chosen such that the cost, density and power consumption of the base solution is not compromised.

# Overview - Test Points and Assumptions




Assumed FEC Parameters:

- Corrects all single bit errors in block
- Chip Area ~ 16k to 20k gates
- Power Consumption/Lane = 20 to 50 mW
- Latency = 1 frame + 3 bits (decoder) + 32 bits (encoder) = 218 ns without error marking
- Latency = 2 frames + 3 bits (decoder) + 32 bits (encoder) = 422 ns with error marking

# Overview - Jitter Allocation Targets

| | GbE | 8GFC | 10G SFP+ SFF-8431 | **40/100G Targets** |
|---|---|---|---|---|
| TP1 DJ, UI | 0.100 | 0.170 | 0.100* | **0.150** |
| TP1 TJ, UI | 0.240 | 0.310 | 0.280 | **0.300** |
| TP4 DJ, UI | 0.462 | 0.420 | 0.420 | **0.400** |
| TP4 TJ, UI | 0.749 | 0.710 | 0.700 | **0.700** |

* SFF-8431 specifies DDJ

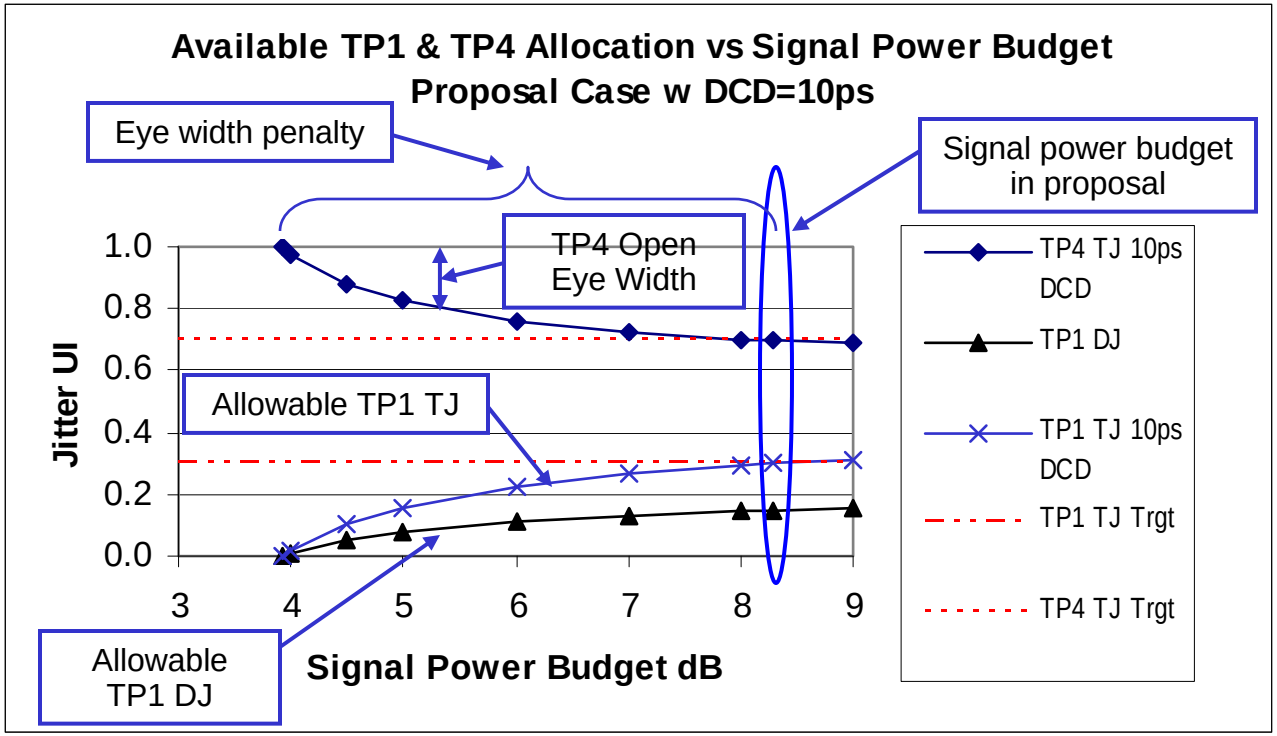
- Before evaluating the benefits of FEC or CDRs, jitter targets are shown for the baseline case. These baseline targets are shown in the above table and compared to requirements in selected specifications.
- The targets were chosen to provide a better design point than those from either 8GFC or 10GBASE-SR as implemented in SFF-8431.

# Link Model

- The 10GbE link model, 10GEPBud3_1_16a, available at http://www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/ was used for the analysis presented in the following pages.
- Jitter in the following pages follows dual-Dirac methodology and, where used, DJ is intended to be dual-Dirac DJ.
- Since the 10GbE link model is open, available to all and reasonably well-regarded, it is a useful tool for comparing various proposals and tradeoff among attributes.
- The 10GbE module was extended to include the effects of RJ at TP1 and Rx contributed DJ and convert noise penalties into the associated RJ, permitting determination of RJ, DJ and TJ at TP4.

# Link Model Results

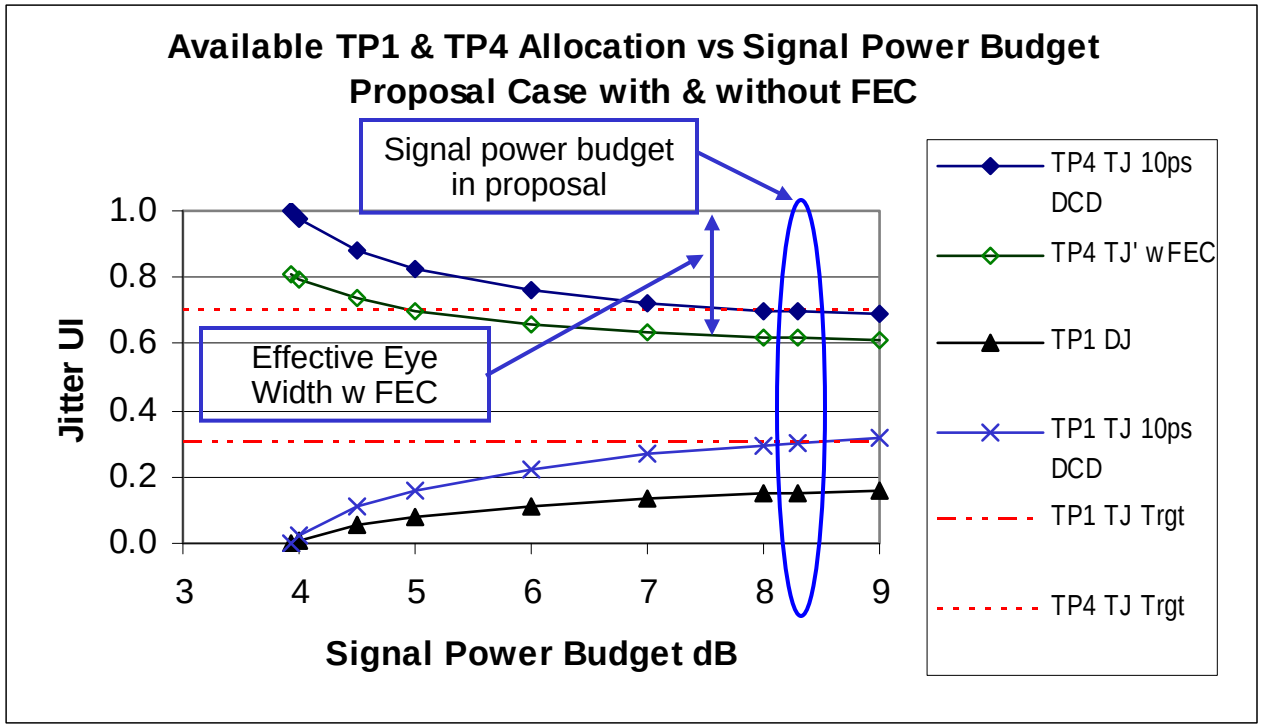
## Base Case TP1 & TP4 TJ Contours




- The figure shows the relationship between available jitter allocation and signal power budget.
- Target jitter allocations are set at TP1 TJ = 0.30 UI & TP4 TJ = 0.70 UI.
- The base case includes an 8.3 dB signal power budget and, as shown above, can support jitter allocations of TP1(DJ) = 0.15 UI, TP1(TJ) = 0.30 UI and TP4(TJ) = 0.70 UI.

# Link Model Results

## TP4 Contours with & without FEC




- Use of FEC provides TP4 TJ relief by effectively reducing its random and/or uncorrelated jitter components. For a fixed TP4 TJ allocation, this can be translated into reach extensions.

# Link Model Base Case
## Transmitter Attributes (Each Lane)

- Min OMA:  -3.0 dBm
- Min ER:  3.0 dB
- Min Center Wavelength:  840 nm
- Max RMS Spectral Width:  0.65 nm
- Max Transition Time (20%, 80%):  35 ps
- Max RIN12OMA:  -130 dB/Hz
- RIN Coefficient: 0.70
- Mode Partition Noise Coefficient:  0.30
- Min Optical Reflection Tolerance: -12 dB
- TP1 Jitter Allocation: TJ = 0.300 UI, DJ = 0.150 UI
- TP2 Jitter Allocation: TJ = 0.488 UI, DJ = 0.284 UI

# Link Model Base Case
## Receiver Attributes (Each Lane)

- Max Sensitivity:  -11.3 dBm
- Min Bandwidth:  7500 MHz
- RMS Base Line Wander:  0.025
- Max Rx Reflection:  -12 dB
- TP3 Jitter Allocation:  DJ = 0.284 UI, DCD = 0.103 UI
- TP3 Jitter Allocation:  TJ = 0.511 UI
- TP4 Jitter Allocation:  TJ = 0.700 UI
- TP4 Jitter Allocation:  DJ = 0.367 UI

# Link Model Base Case
## Link Attributes (Each Lane)

- Signal Rate: 10.3125 GBd
- BER: < $10^{-12}$ (Q = 7.034)
- 100 m of OM3
- 1.5 dB connector loss allocation
- Signal Power Budget:  8.3 dB
- Attenuation = 0.36 dB
- Center Eye Penalties
  - Pisi = 1.40 dB
  - Pdj = 0.22 dB
  - Pmn = 0.30 dB
  - Pmpn = 0.02 dB
  - Prin = 0.15 dB
  - Pcross = 0.14 dB
- 0.30 UI Eye Width Penalty = 4.11 dB (see figure on page 7)

# Summary

## Potential Extended Reach or Jitter Allocation Relief

### Comparison: Link reach for constant TP1 & TP4

| | Base (Targets) | KR FEC |
|---|---|---|
| OM3 Reach, m | 100 | 183 |
| OM4 Reach, m | 126 | 223 |

### Comparison: TP1 & TP4 for constant 100 m link reach

| | Base (Targets) | KR FEC |
|---|---|---|
| TP1 DJ, UI | 0.150 | 0.150 |
| TP1 TJ, UI | 0.300 | 0.300 |
| TP4 DJ, UI | 0.367 | 0.367 |
| TP4 TJ, UI | 0.700 | 0.620* |

* TP4 TJ at correctable single bit error rate

# Summary
## KR FEC Costs, Benefits & Limitations

- **Costs**
  - Latency: if FEC is done per lane, 218 ns without error marking, 422 ns with error marking (Note 422 ns is the time of flight for ~84 m of fiber.)
  - Chip Area: 16k to 20k gates (per lane)
  - Power Dissipation: 20 to 50 mW (per lane)
- **Benefits**
  - Doesn't look like another PMD. TP1 and Tx specs remain the same. TP4 and Rx specs are stated at a higher BER which can be included in the SRS test without significant impact.
  - Free - likely already available for backplanes and copper cable assemblies support
  - Forward looking - Likely needed for all variants at 25 GBd and higher signal rates and doesn't require redesign for shift from 10 GBd/lane to 25GBd/lane
  - Lower imposition of dynamic range and/or distortion limits on optics modules and host ICs
  - Keeps solution within host IC
  - Turn on when needed to correct errors due to longer fiber lengths or PCB traces
  - Corrects raw 4.4E-8 BER into 1E-12 BER.
  - Enables continuous error monitoring without requiring traffic
  - No increase in overhead – no sacrifice of data rate
- **Limitations**
  - Mitigates noise but not systematic impairments, e.g. ISI
  - Useful only if both ends of the link have FEC

# Conclusions/Recommendations (1)

- KR FEC can be used to provide more generous TP1 and TP4 jitter allocations or increase the fiber reach, with no increase in power consumption or tighter specifications for the pluggable modules or increase in payload overhead or change in signal rate.
- FEC is a solution well-matched for the impairments expected from crosstalk in multilane implementations and degradation in SNR for longer fiber reaches.
- FEC doesn’t impose dynamic range or distortion limits on the optics modules.
- FEC can be used with all variants

# Conclusions/Recommendations (2)

## FEC Promotion

- It's time to embrace FEC
- FEC (forward error correction) turns a mediocre to bad BER into a good BER. It mitigates noisy eyes. Many versions exist with different gains and costs.
- Ethernet uses FEC in:
  - 1000BASE-PX (EPON)
  - 10GBASE-KR
  - 10GEPON
  - 10GBASE-T
  - DSL
- High end long haul telecoms use many FEC schemes.
- P802.3ba links have limited power budgets and SNR, for e.g. eye safety reasons. We also can benefit from FEC.

# References


- 10GBASE-KR FEC Tutorial
  http://ieee802.org/802_tutorials/july06/10GBASE-KR_FEC_Tutorial_1407.pdf
  See IEEE Std 802.3, 74
- 802.3ah EFM
  Reed-Solomon code (255, 239) operating on 8-bit symbols.
  See IEEE Std 802.3, 65.2 and e.g.
  http://ieee802.org/3/efm/public/sep01/rennie_1_0901.pdf
  http://ieee802.org/3/efm/public/jul02/p2mp/khermosh_general_1_0702.pdf
  http://ieee802.org/3/efm/public/sep02/p2mp/rennie_p2mp_1_0902.pdf
- 802.3av
  RS(255, 223) See P802.3av 92.3 and e.g.
  http://ieee802.org/3/av/public/2007_07/3av_0707_daido_1.pdf
  http://ieee802.org/3/av/public/2007_01/3av_0701_effenberger_1.pdf
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  http://ieee802.org/3/av/public/2007_05/3av_0705_effenberger_4.pdf
- petrilla_HSE_01_0208
  http://www.ethernetalliance.org/apps/org/workgroup/hse/download.php/573/petrilla_HSE_01_0208.pdf
- petrilla_01_0308
  http://www.ieee802.org/3/ba/public/mar08/petrilla_01_0308.pdf
- QSFP MSA
  http://www.qsfpmsa.net/index.html
  ftp://ftp.seagate.com/sff/INF-8438.PDF