



**CEI-25 / CEI-28 Projects
Ad Hoc:**

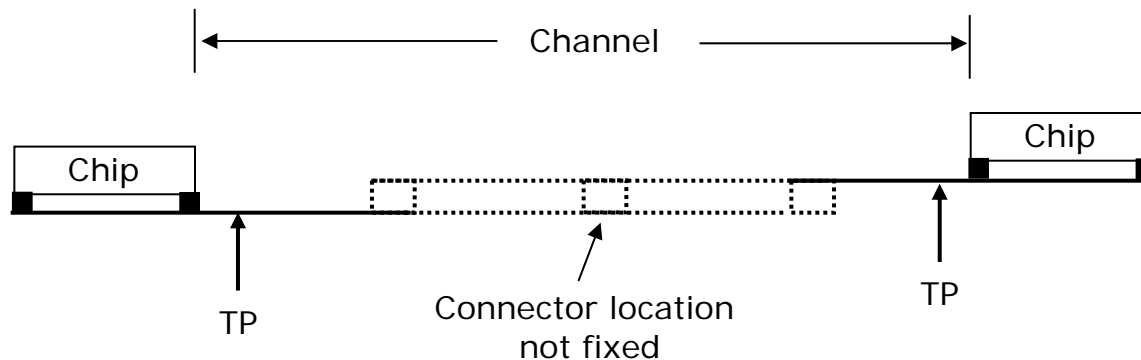
Some Initial Thoughts for Discussion

Gary Nicholl, Cisco
18 November, 2009

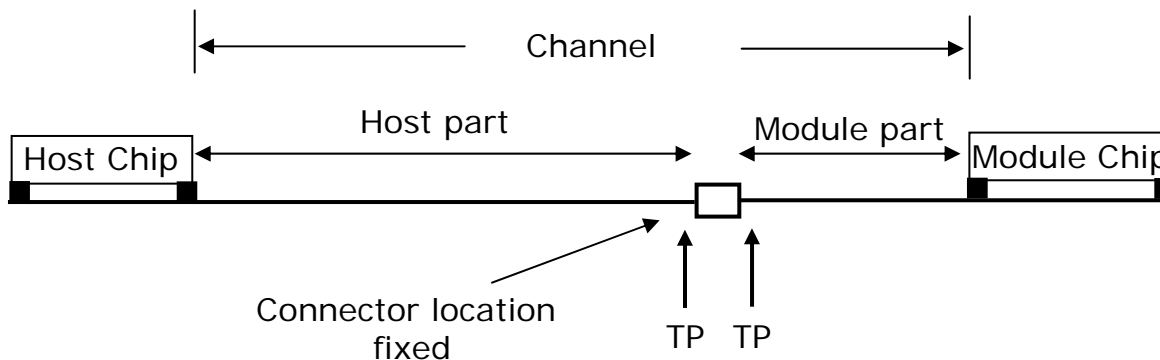
Chip to Chip versus Chip to Module ?

- Need to have a clear understanding of terminology ..
- (Hidden) assumption is that we would (ideally) like to use same serdes technology (same elec specs) for both applications ?

Chip to chip



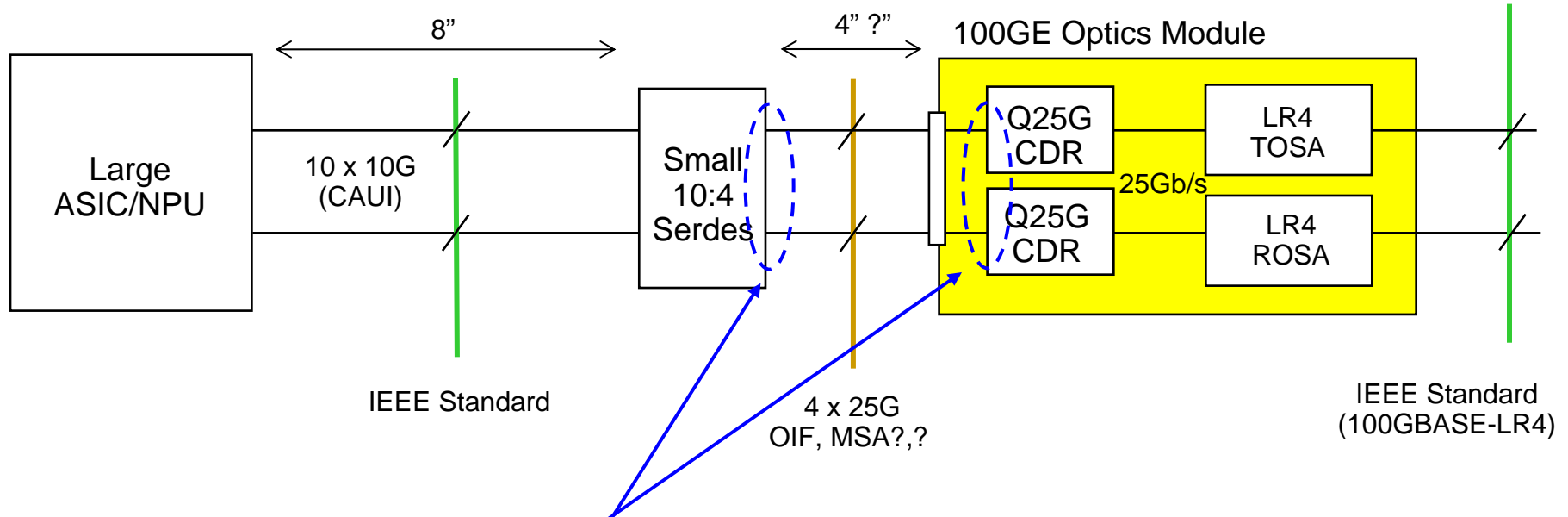
Chip to Module



- Connector location fixed
- Test points moved to connector
- Likely a different chip on either end of link (so could support asymmetric electrical specs)

Symmetrical versus Asymmetrical ?

- another term that problem needs clear explanation

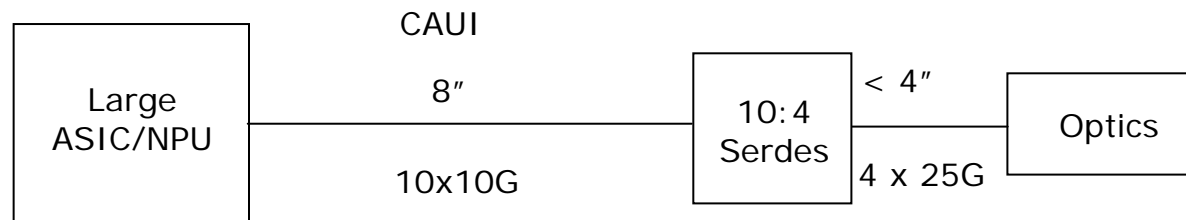


- Host and module chip electrical specs could be identical (symmetrical) or could be different (asymmetrical)
- BUT .. power in the module is at a premium (and is not as critical on host)
- An asymmetrical solution might be preferred, even if the total power dissipation is higher than a symmetrical solution

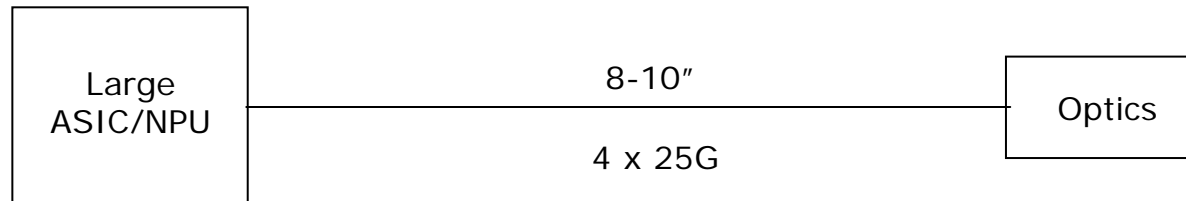
Chip to Module Applications

- there are likely two primary applications, with different distance (and timeframe ?) requirements ...

Initial Application



Future Application (circa 2015?)



- Initial application: NPU/ASIC will have 10G I/O. Always be a 10:4 serdes in front of each module. 25G distances are short (< 4" ?).
- Future application: NPU/ASIC migrate to integrated 25G I/O. May want to drive optics directly and eliminate need for (host) serdes. 25G distances are longer (8-10")
- Do we want one 'superset' 25G spec which addresses both, or two specs .. one optimized for each application ?

Summary

- Ran out of time ...