PBL Solution for HSE

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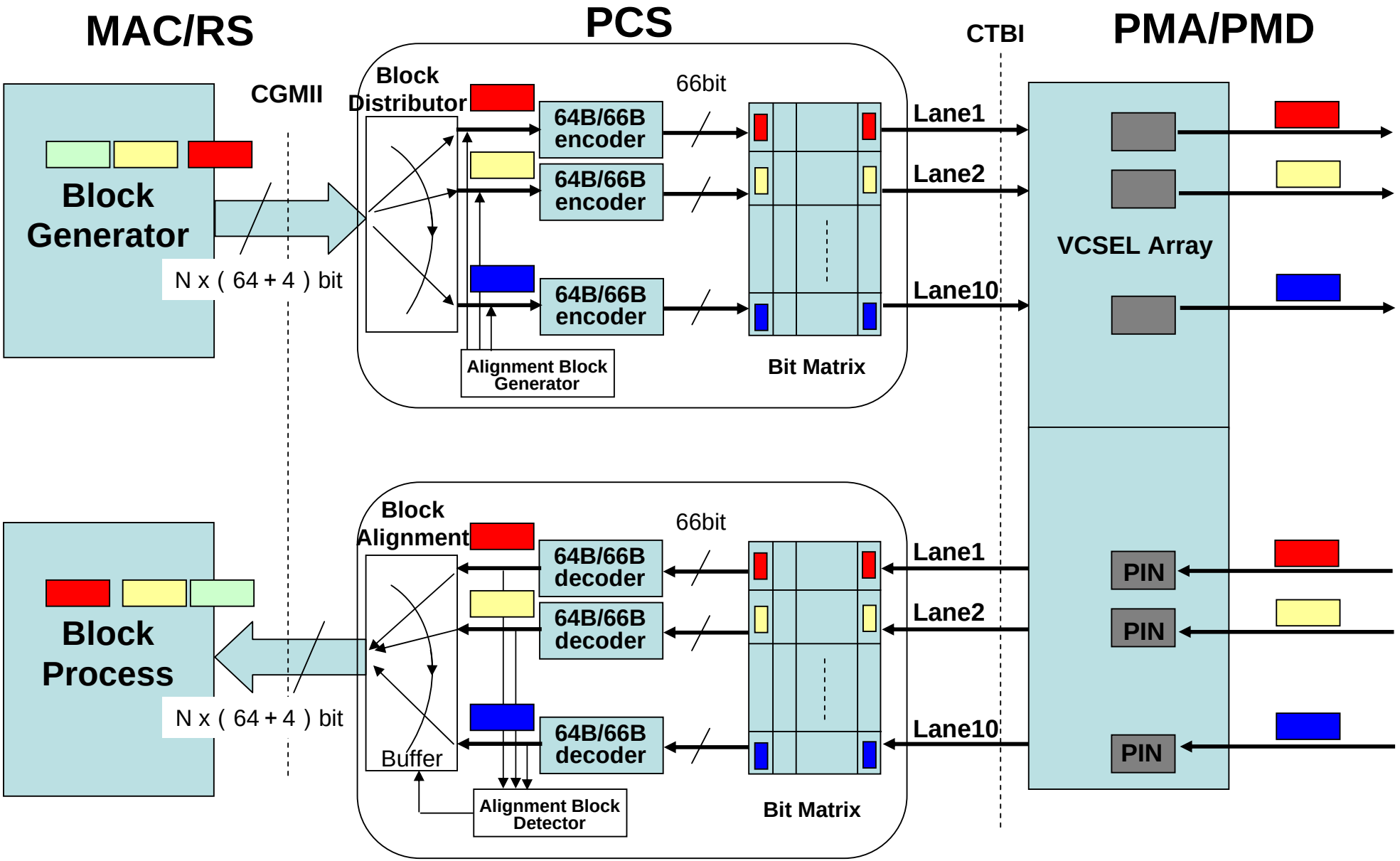
PBL Model

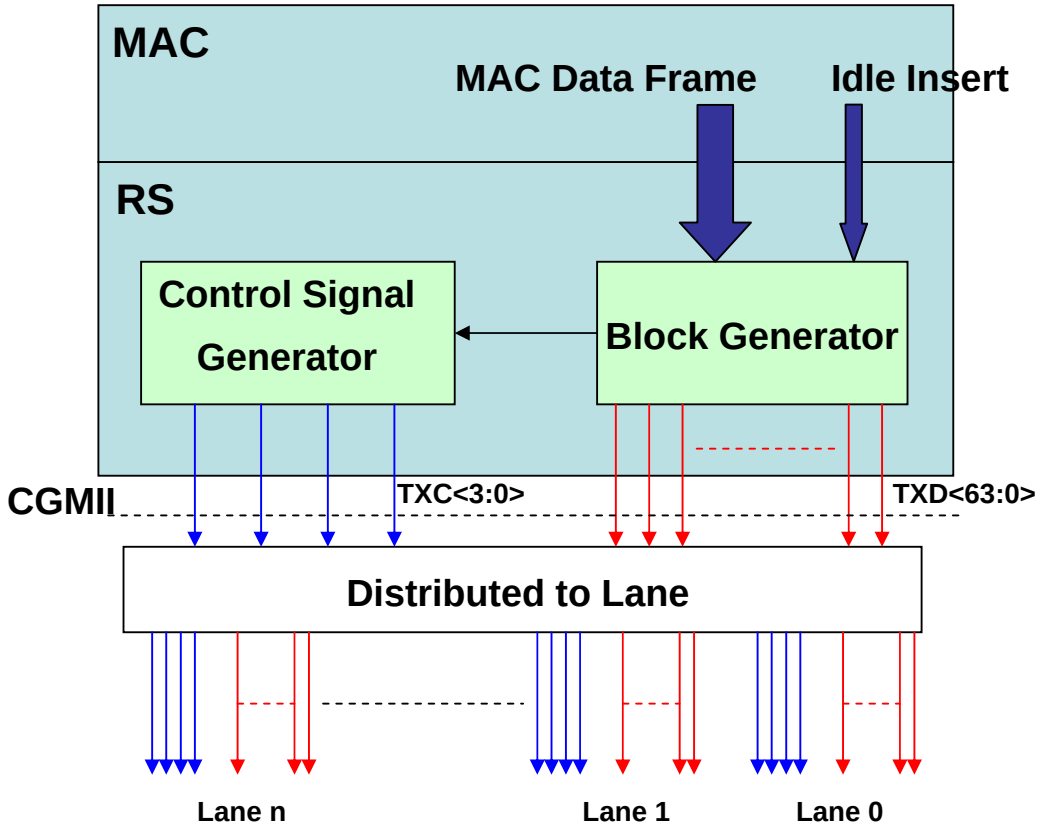

MAC/RS
PCS
CTBI
PMA/PMD
CGMII
Block Generator
N x (64 + 4) bit
Block Distributor
66bit
64B/66B encoder
64B/66B encoder
64B/66B encoder
Alignment Block Generator
Bit Matrix
Lane1
Lane2
Lane10
VCSEL Array
Block Process
N x (64 + 4) bit
Block Alignment
66bit
64B/66B decoder
64B/66B decoder
64B/66B decoder
Buffer
Alignment Block Detector
Bit Matrix
Lane1
Lane2
Lane10
PIN
PIN
PIN

PBL Model

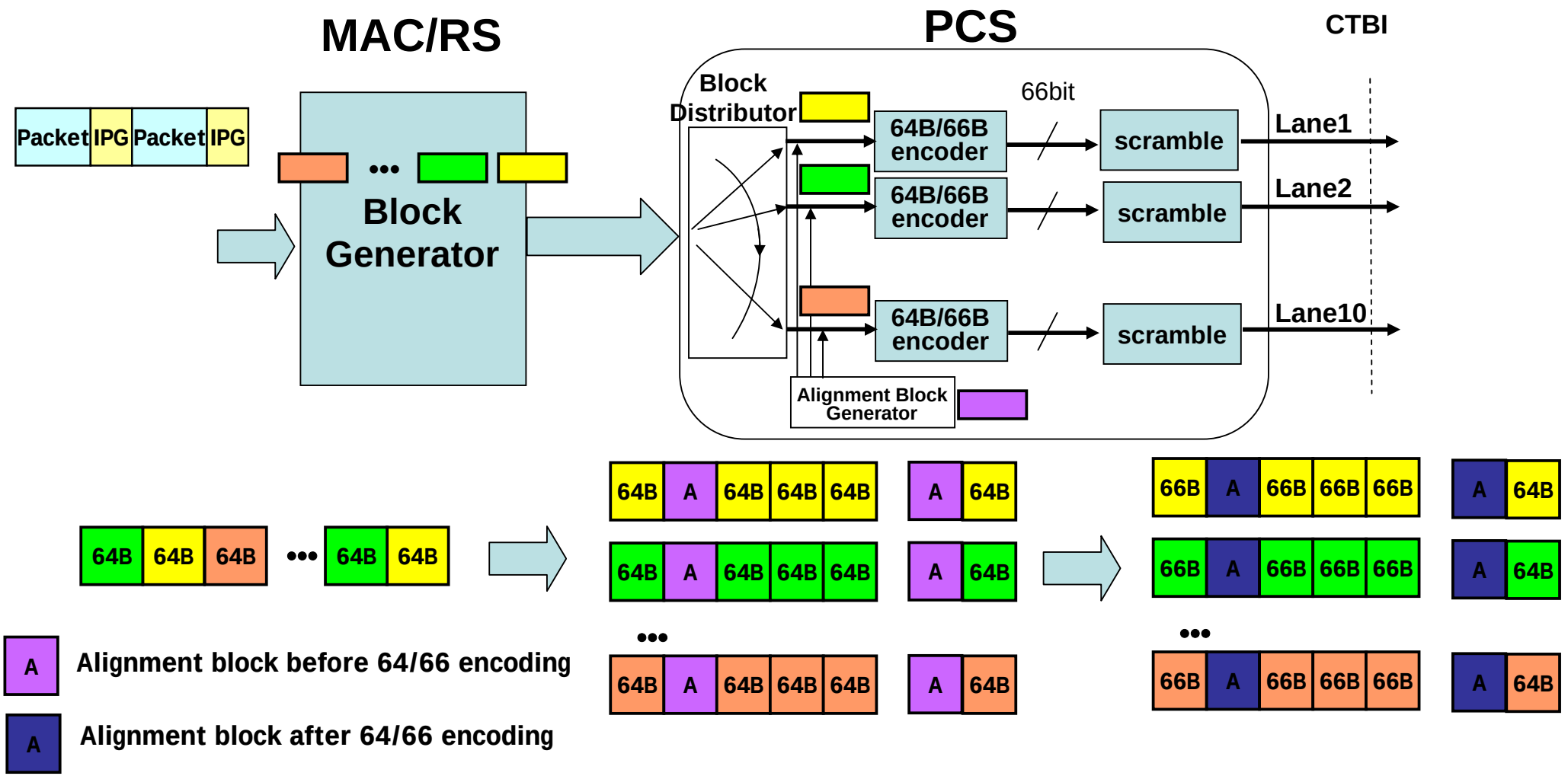
- Receives data from MAC layer, generates 64-bit blocks
- Transmits blocks through the CGMII bus
- Blocks distributed to N lanes, alignment words will be inserted in each lane following the distributor.
- Encode the blocks in each lane (64B/66B encoding & scrambler)
- Bit matrix will adapt N-lane structure to standard CTBI for all PMDs
- Preserves block format in the physical Lanes (Block interleave in physical lanes)

Block Generator and CGMII Interface

- MAC data frame will generate the 64-bit blocks using the existing 64B/66B rule.
- Based on the type of the Block, RS generates the 4-bit control code signal.
- (64+4)bit is the unit of the CGMII for each lane
- PBL distributes the blocks to each lane



Block Distribution and Alignment Insertion



- Alignment blocks will be added into the stream by increasing lane rate

Insert alignment block by increasing lane rate

- **Alignment block is defined using a 64B/66B block format.**

- **Increase the lane rate to insert the alignment blocks.**
  - **If we send an alignment block once every 1375 blocks, the lane rate will be 10.32GHz (0.073% increase)**
  - **If we send an alignment block once every 16k blocks, the lane rate will be 10.313GHz (0.00625% increase)**
  - **Alignment block rate will affect**
    - **the maximum skew that can be compensated**
    - **adaptation to OTN**
    - **receive RAM size for de-skew**
    - **clock rate generator complexity in the encoding modules**

What should the alignment block look like

- **Alignment block:**

  64-bit data + 4-bit ctrl

1101	5a	SEQ	ID	x	x	x	x	x

- **Alignment block after 64/66 coding:**

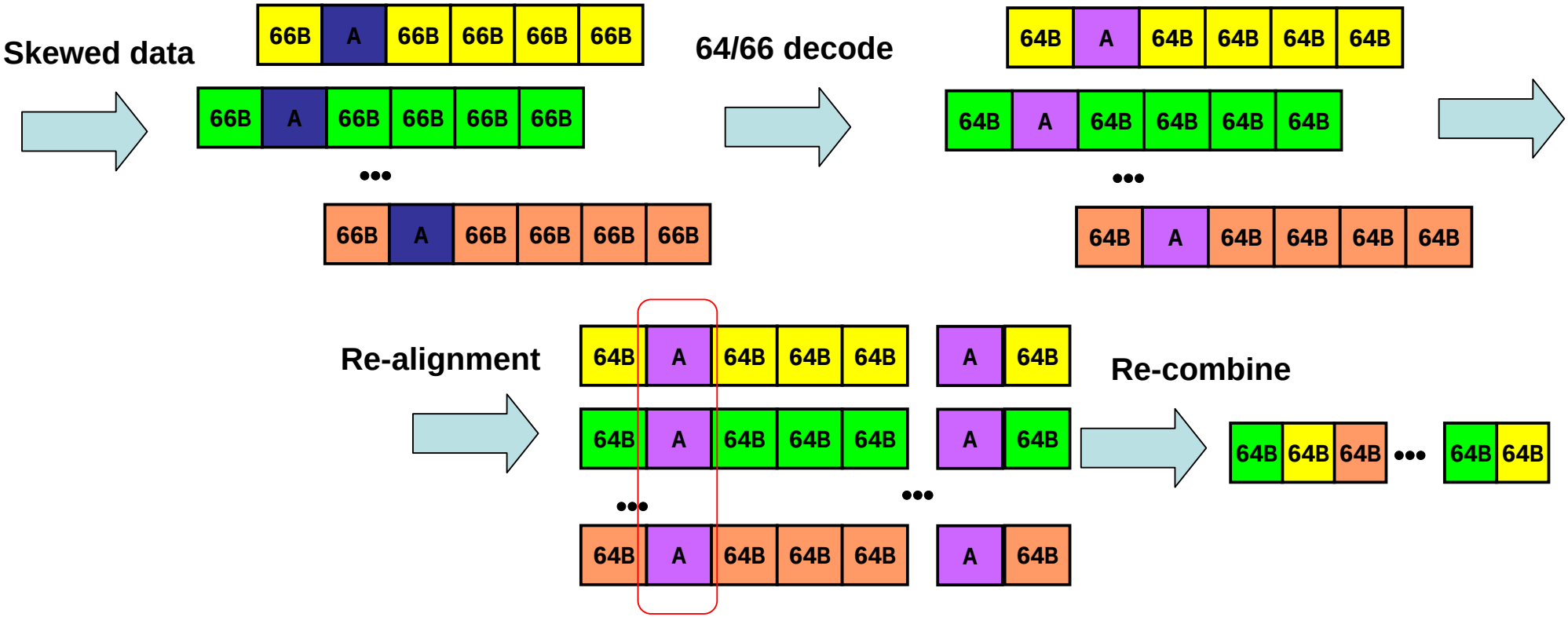
10	5a	SEQ	ID	x	x	x	x	x

  –SEQ is alignment block sequence number

  –ID indicates the lane number

TXD/RXD								TXC/RXC	Description
D	D	D	D	D	D	D	D	0000	Data
S	D	D	D	D	D	D	D	1001	Start
C	C	C	C	S	D	D	D	1010	Start
T	C	C	C	C	C	C	C	1000	Terminate
D	T	C	C	C	C	C	C	0111	Terminate
D	D	T	C	C	C	C	C	0110	Terminate
D	D	D	T	C	C	C	C	0101	Terminate
D	D	D	D	T	C	C	C	0100	Terminate
D	D	D	D	D	T	C	C	0011	Terminate
D	D	D	D	D	D	T	C	0010	Terminate
D	D	D	D	D	D	D	T	0001	Terminate
C	C	C	C	C	C	C	C	1111	Control
A	A	A	A	A	A	A	A	1101	Alignment
O	O	O	O	O	O	O	O	New	OAM
N	N	N	N	N	N	N	N	New	Null
X	X	X	X	X	X	X	X	New	Reserve

Insert alignment block by increasing lane rate



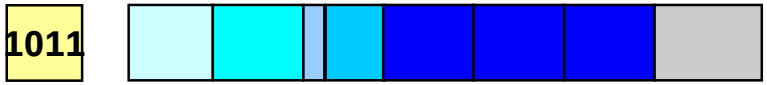
- The received data is unaligned because of the skew introduced across physical lanes
- Decode and detect the alignment block
- Realign using alignment block with the same SEQ
- Reassemble data steam in order by lane ID.

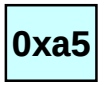
PHY OAM Process

- **PHY OAM process can be used to monitor lane failures.**
  - LLF/RLF
  - Others, i.e. Auto negotiate
- **PHY OAM code is defined as a new block type.**
- **Insert PHY OAM by stealing from IPG**

What should the OAM block look like

- OAM block: 64-bit data + 4-bit ctrl





Block type:8bits

OAM type: 8bits
- x01H:LLF
- x02H:RLF
- x03H:status advertisement
- x04H:BER Monitor
- Others: reserved

Broadcast OAM / lane OAM : 2bits

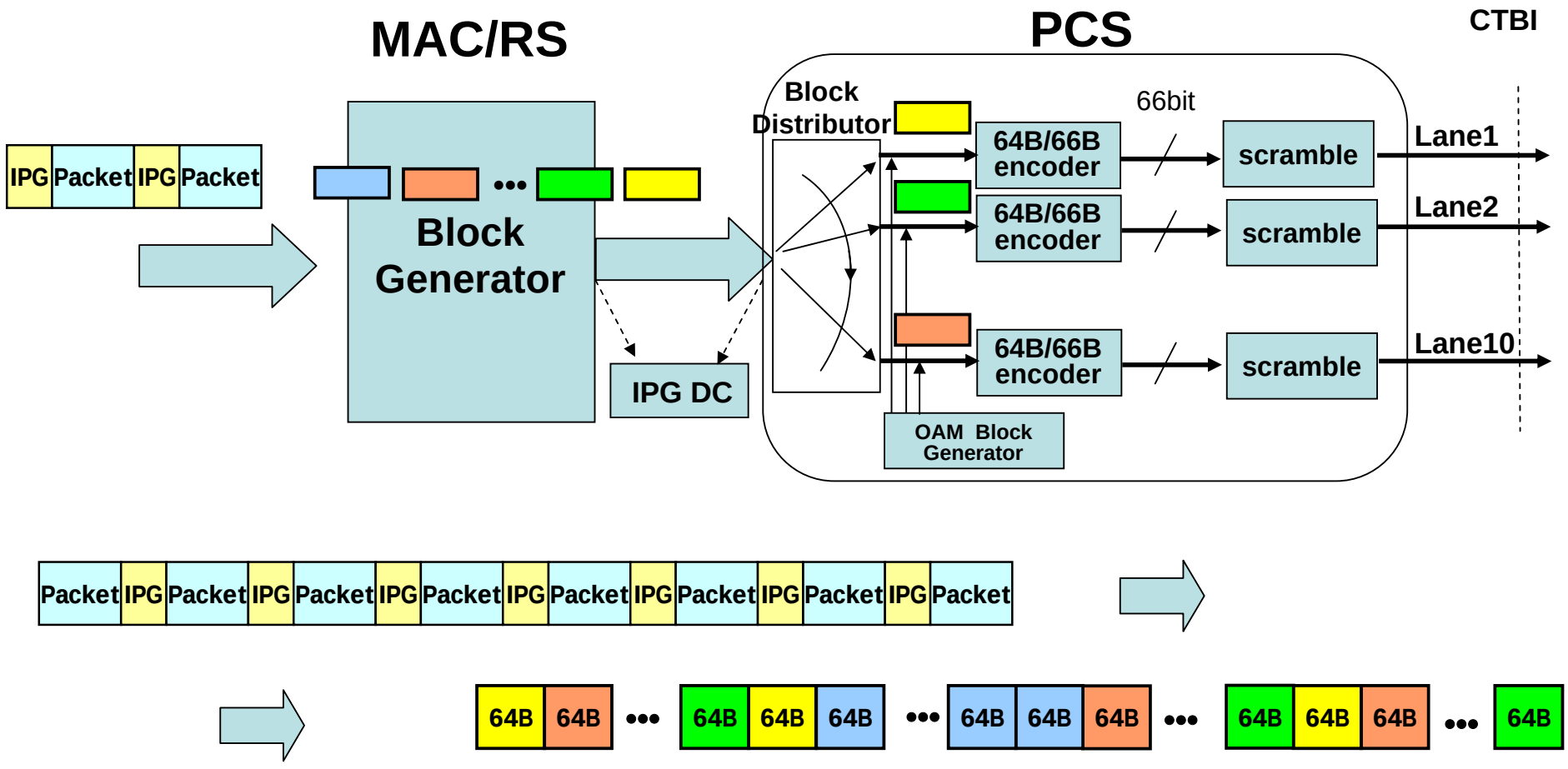
lane ID : 6bits

OAM value : 24bits

reserved

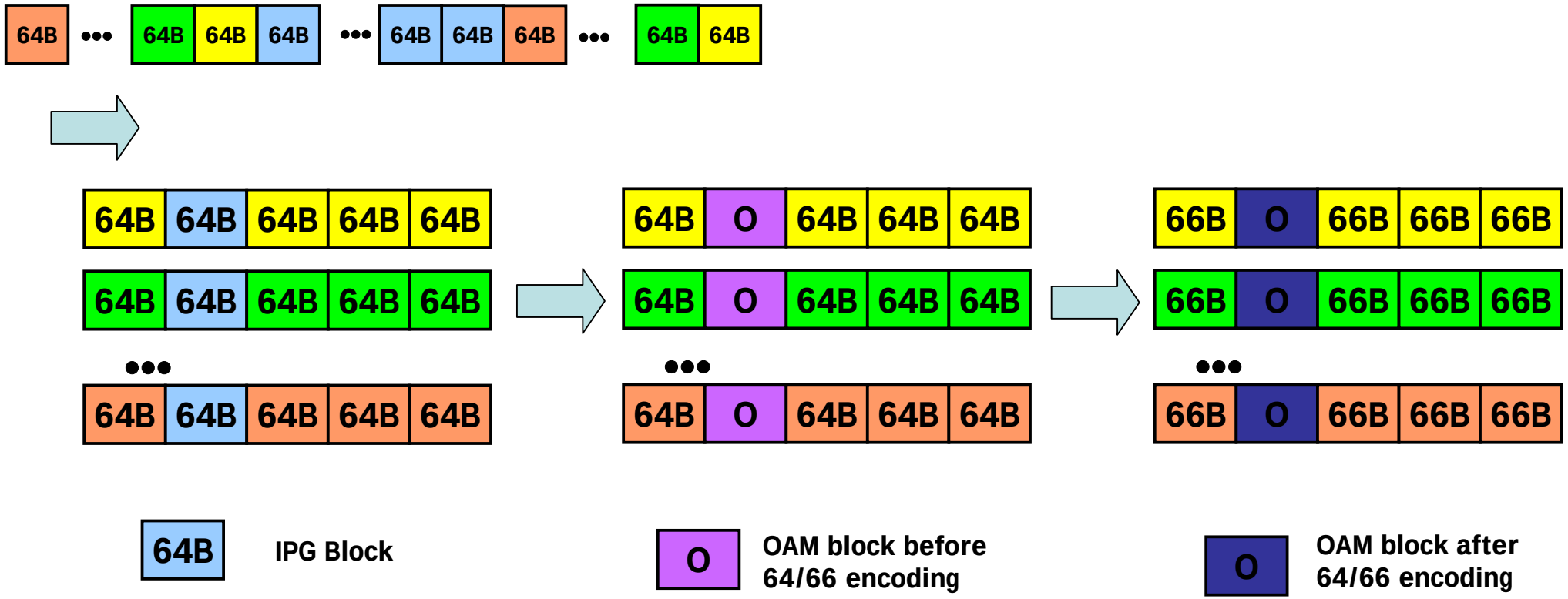
TXD/RXD								TXC/RXC	Description
D	D	D	D	D	D	D	D	0000	Data
S	D	D	D	D	D	D	D	1001	Start
C	C	C	C	S	D	D	D	1010	Start
T	C	C	C	C	C	C	C	1000	Terminate
D	T	C	C	C	C	C	C	0111	Terminate
D	D	T	C	C	C	C	C	0110	Terminate
D	D	D	T	C	C	C	C	0101	Terminate
D	D	D	D	T	C	C	C	0100	Terminate
D	D	D	D	D	T	C	C	0011	Terminate
D	D	D	D	D	D	T	C	0010	Terminate
D	D	D	D	D	D	D	T	0001	Terminate
C	C	C	C	C	C	C	C	1111	Control
A	A	A	A	A	A	A	A	1101	Alignment
O	O	O	O	O	O	O	O	1011	OAM
N	N	N	N	N	N	N	N	New	Null
X	X	X	X	X	X	X	X	New	Reserve

Insert OAM block by stealing from IPG



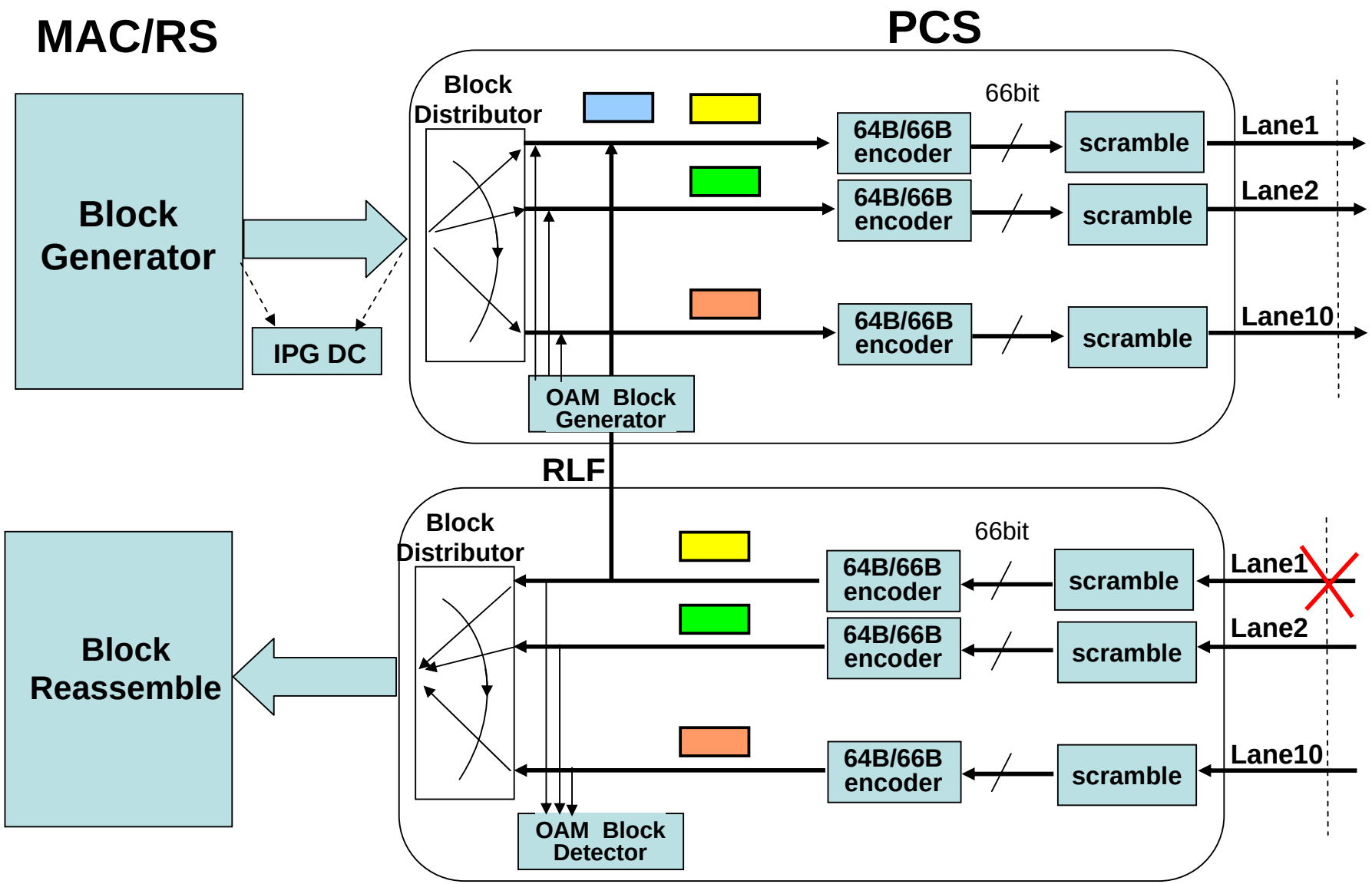
- IPG adjustment gains gains enough bandwidth for inserted OAM
- Introduce Deficit Counter mechanism to collect extra IPG
- OAM blocks cover the extra IPG (generator)

Insert OAM block by stealing from IPG



- Block generator adjusts IPG to get IPG blocks in each lane
- Distributor sends IPG blocks to each lane
- PHY OAM replaces the IPG block

Fault Indication by PHY OAM Block



Receiver gets lane failure information, returns a Remote Link Fail status to Transmitter for OAM block generation

Block Encoding

- **Receive distributed blocks in each lane**
- **64/66 encoding format is compatible to 10GE**
- **Independently encode and scramble in each lane**
- **The scrambler polynomial**
  - $G(X)=1+X^{39}+X^{58}$

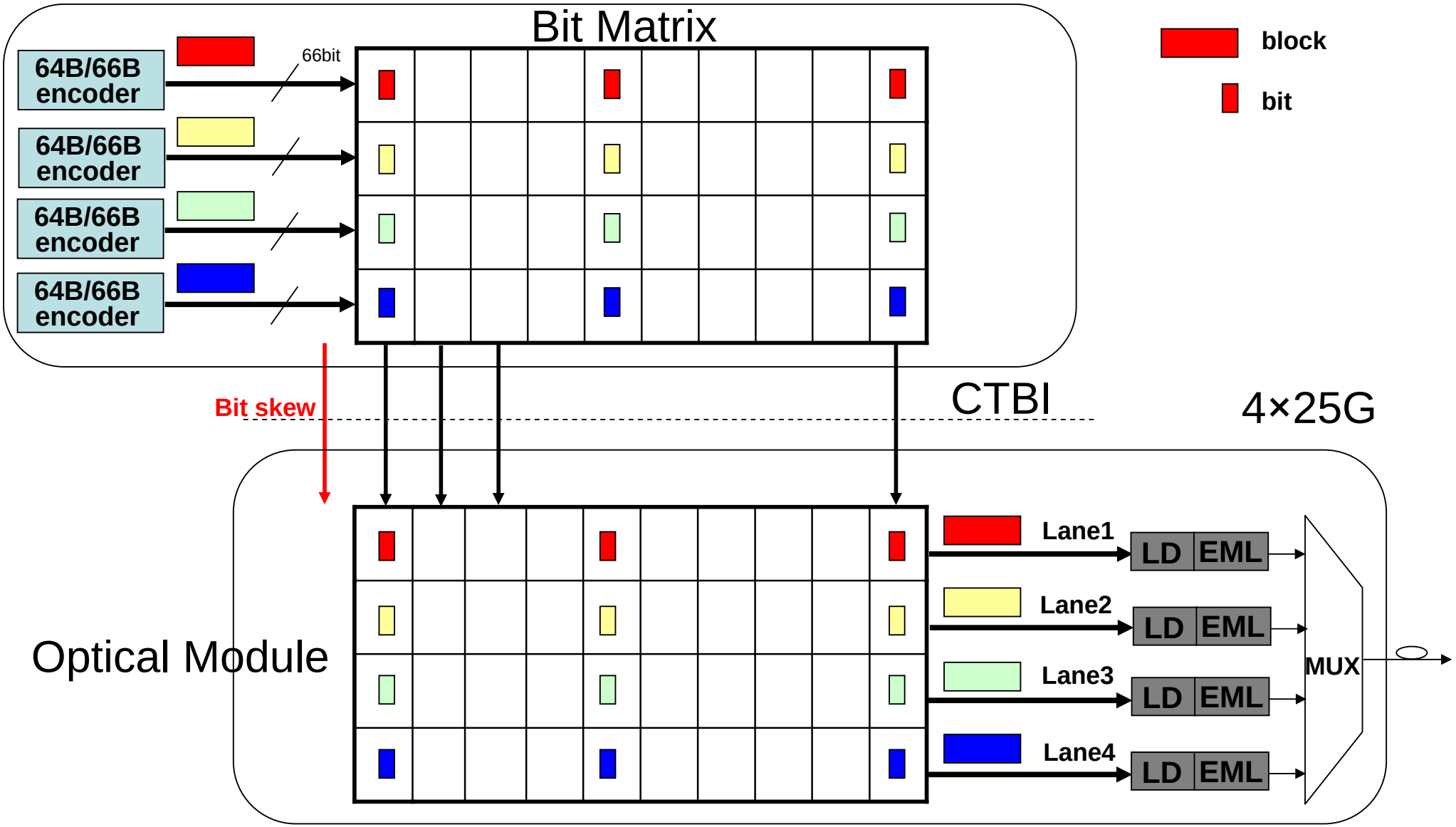
64B/66B Block Formats

	Original Data (64bit+4bit)										Output Data (66Bit)								
Description	TXC/RXC	TXD/RXD								SYNC	Block Payload								
Data	0000	D	D	D	D	D	D	D	D	01	D	D	D	D	D	D	D	D	
Control Block Formats											Block Type								
Start	1001	S	D	D	D	D	D	D	D	10	0x78	D	D	D	D	D	D	D	
Start	1010	C	C	C	C	S	D	D	D	10	0x33	C’	C’	C’	C’		D	D	D
Terminate	1000	T	C	C	C	C	C	C	C	10	0x87		C’	C’	C’	C’	C’	C’	C’
Terminate	0111	D	T	C	C	C	C	C	C	10	0x99	D		C’	C’	C’	C’	C’	C’
Terminate	0110	D	D	T	C	C	C	C	C	10	0xaa	D	D		C’	C’	C’	C’	C’
Terminate	0101	D	D	D	T	C	C	C	C	10	0xb4	D	D	D		C’	C’	C’	C’
Terminate	0100	D	D	D	D	T	C	C	C	10	0xcc	D	D	D	D		C’	C’	C’
Terminate	0011	D	D	D	D	D	T	C	C	10	0xd2	D	D	D	D	D		C’	C’
Terminate	0010	D	D	D	D	D	D	T	C	10	0xe1	D	D	D	D	D	D		C’
Terminate	0001	D	D	D	D	D	D	D	T	10	0xff	D	D	D	D	D	D	D	
Control	1111	C	C	C	C	C	C	C	C	10	0x1e	C’	C’	C’	C’	C’	C’	C’	C’
Alignment	1101	A	A	A	A	A	A	A	A	10	0x5a	SEQ	ID	x	x	x	x	x	
OAM	1011	O	O	O	O	O	O	O	O	10	0xa5	OAM TYPE	OAM Value						
Null	New	N	N	N	N	N	N	N	N	10	0x00	0x00							
Reserve	New	X	X	X	X	X	X	X	X	10									

Bit Matrix

- **Adaptation between N PBL lanes to CTBI**
- **Adapts to any N-lane physical transport by bit transpose**
- **Bit Matrix is (n x m) memory**
  - n is number of distributed lanes (physical lanes)
  - m is number of electrical lanes in CTBI signal (10)

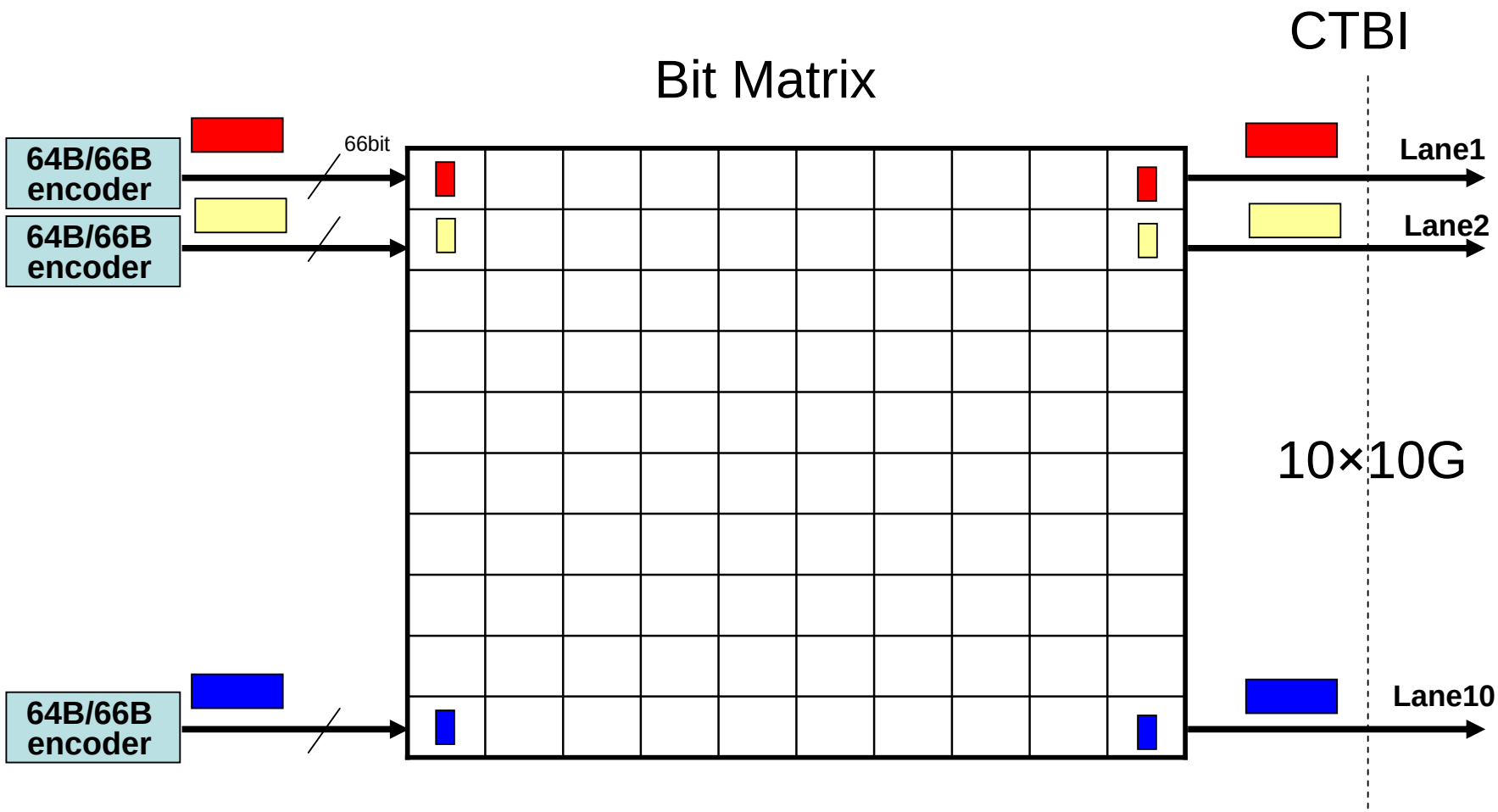
Bit Transpose (10:4)



Bit Matrix

- **The block from the independent lane is written into the row of matrix bit by bit**
- **Bits will be read from column of the matrix**
- **A de-skew lane will help re-align the bits across the CTBI**
  - The mechanism is the same as the SFI-5 definition.
- **A bit matrix is used in the 4x25G module.**

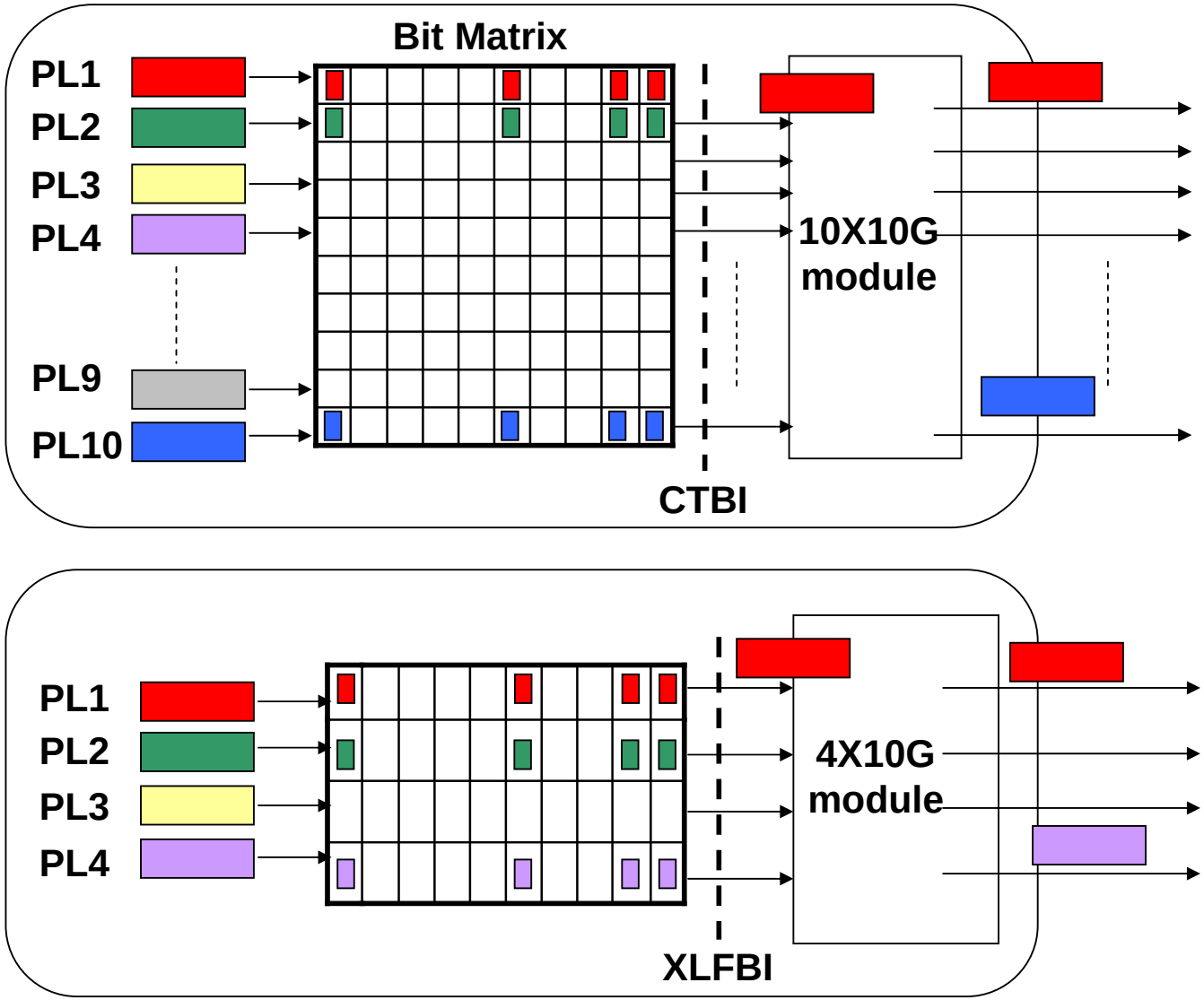
Bit Pass Through



Special mode for 10x10G module, the pass through mode can keep the blocks running in the lanes

What do the PMD Modules look like?

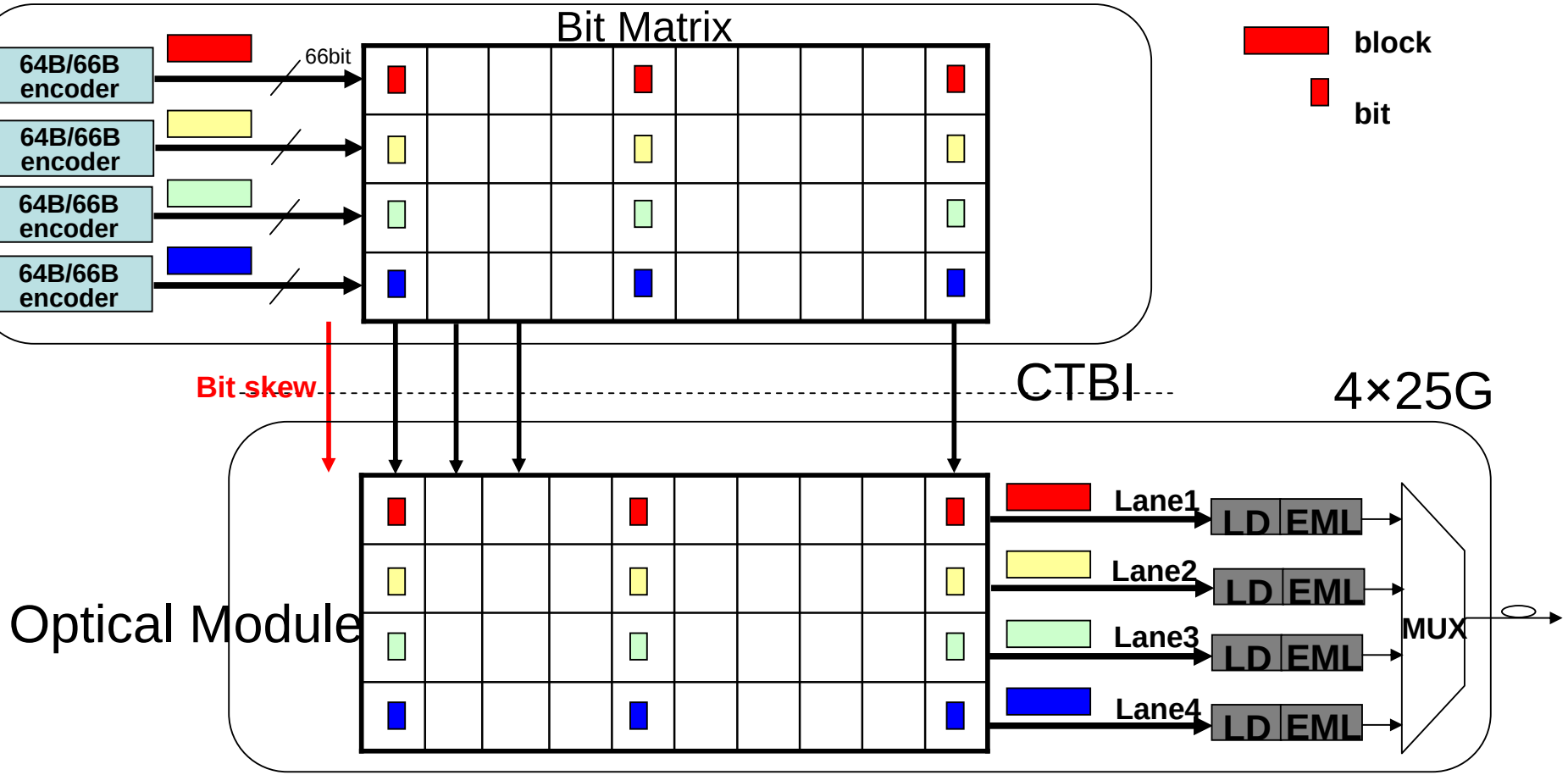
- Nx10G PMDs



When the number of nTBI lanes = the number of module physical lanes, then the module is very simple and 64/66 blocks are preserved at the final output.

What do the PMD Modules look like?

•4x25G PMD



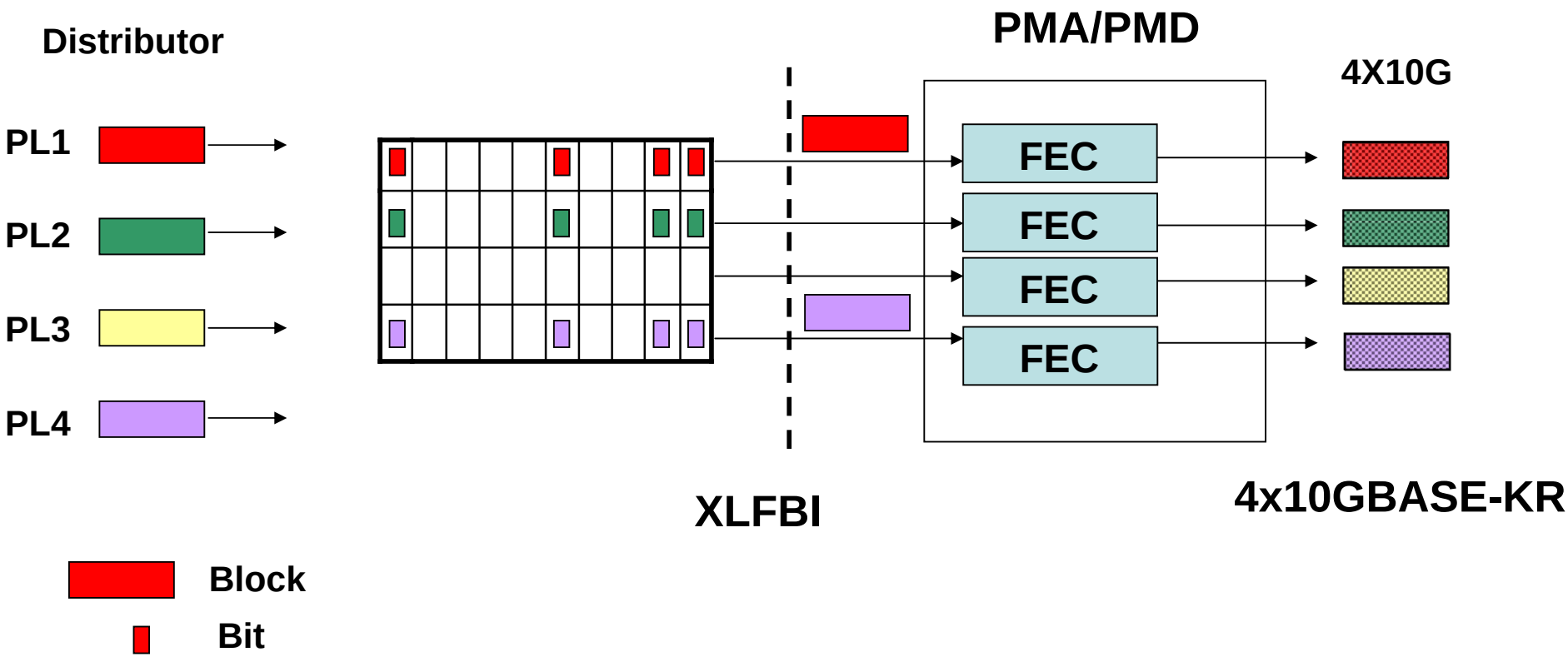
For the 4x25G PMD module, the bit matrix is required to go from 10-lane CTBI back to 4-lane physical; but this module is better able to tolerate the extra cost.

Applications with PBL Model

- **Backplane Transmission**
- **Mapping to OTN**

Backplane Application

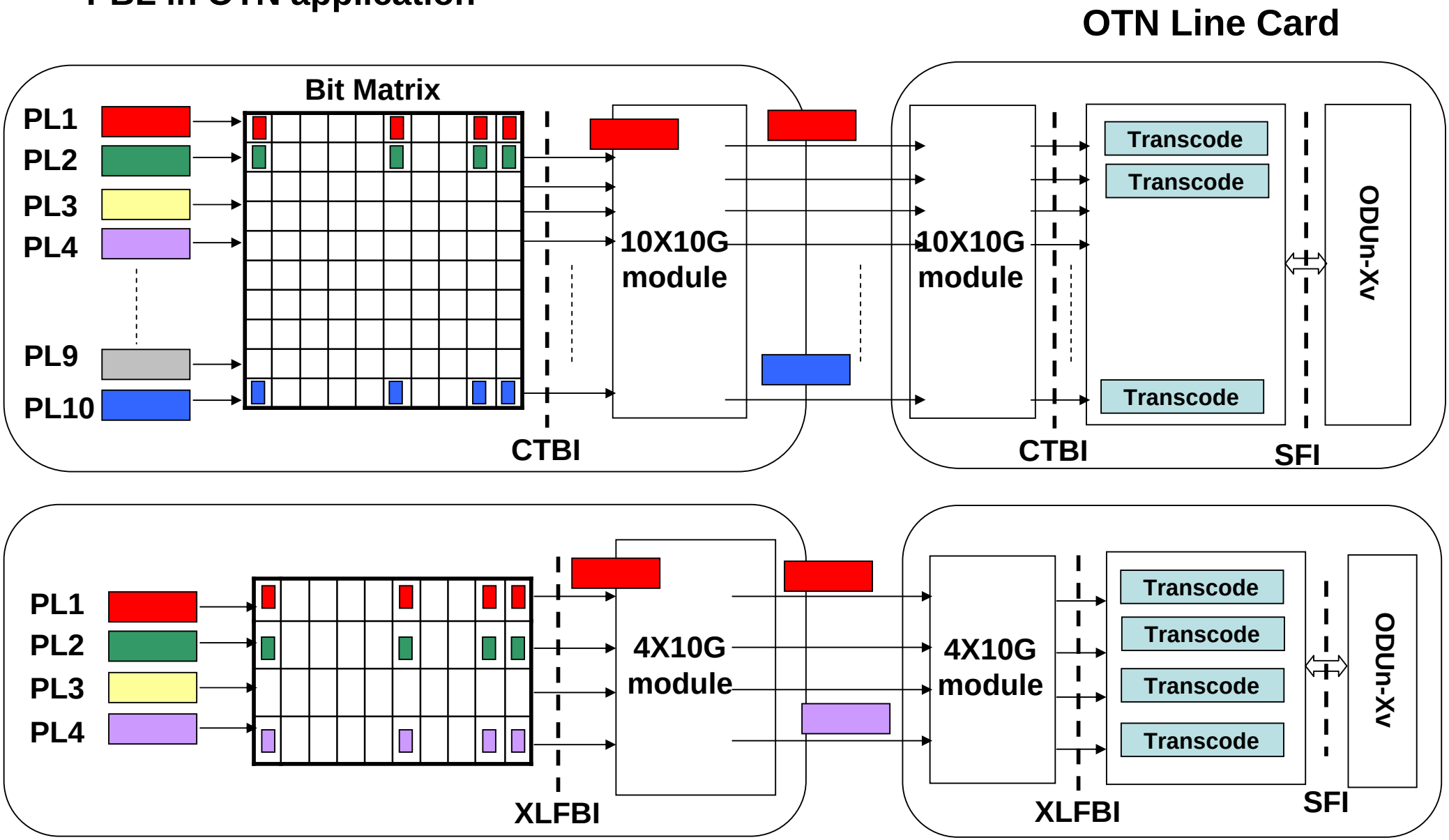
•Backplane transmission



FEC function is implemented in each lane; re-use existing KR
Current FEC requires preservation of 64/66 block boundaries

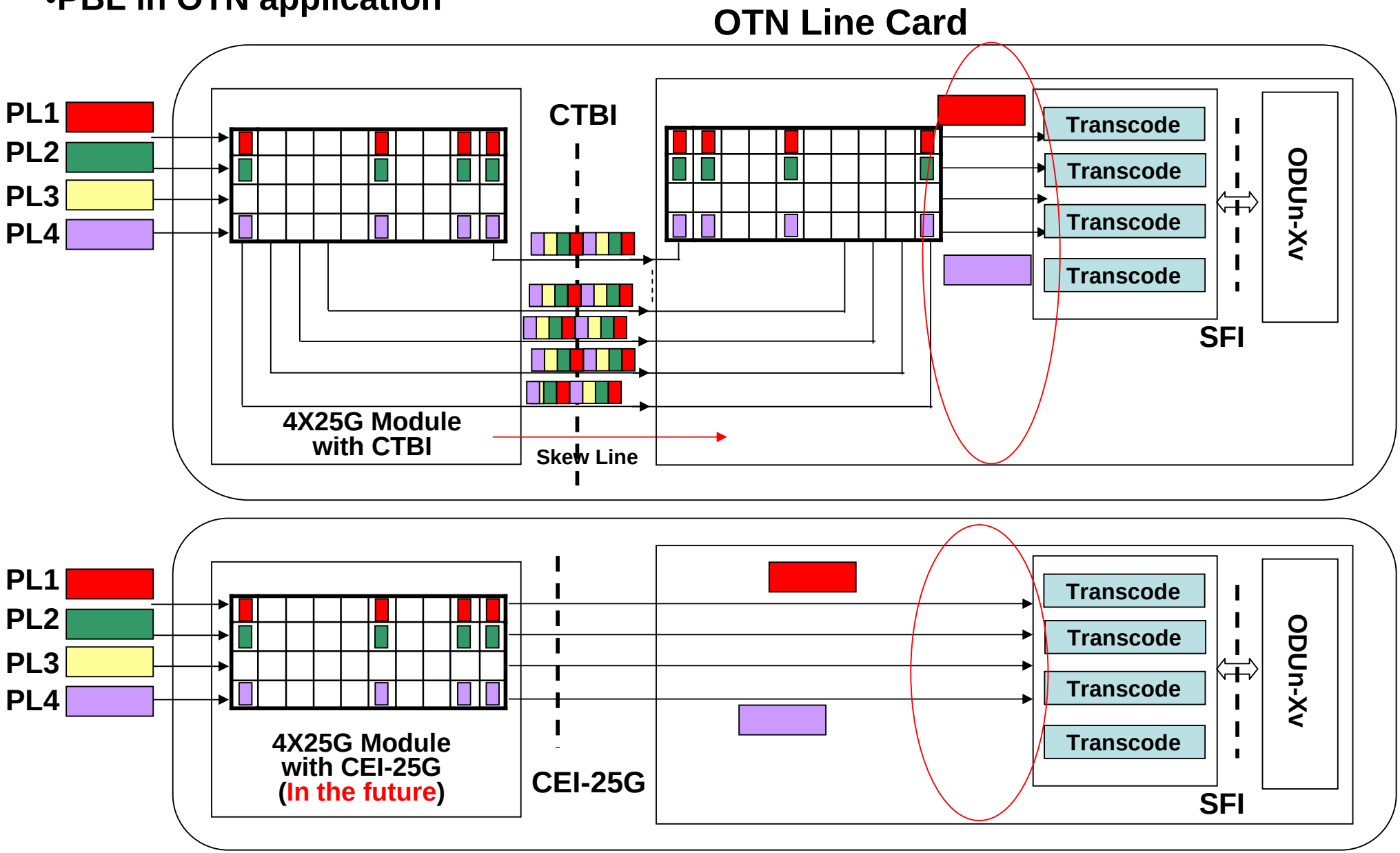
OTN application

- PBL in OTN application



OTN application

- PBL in OTN application



Conclusion

- **Blocks running in Physical lanes (rather than bit interleave)**
  - **Benefit to OTN mapping and Backplane applications by using existing technology.**
  - **Enables fault detection and maintenance per physical lane**
  - **Physical Bundling Layer can be easily extended to higher-rate Ethernet in the future (1Tbps…)**
  - **Block integrity in each physical lane is an important feature**
- **Alignment blocks will be needed in multi-lane formats**
  - **Define the alignment block by extending 10GE block formats**
  - **Insert alignment blocks into the data steam**
- **PHY OAM provides the monitor of physical lane**
  - **Lane failure will be indicated (LLF/RLF)**
  - **More functions can be considered using PHY OAM (Auto Negotiate, BER monitor)**

Thank You

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