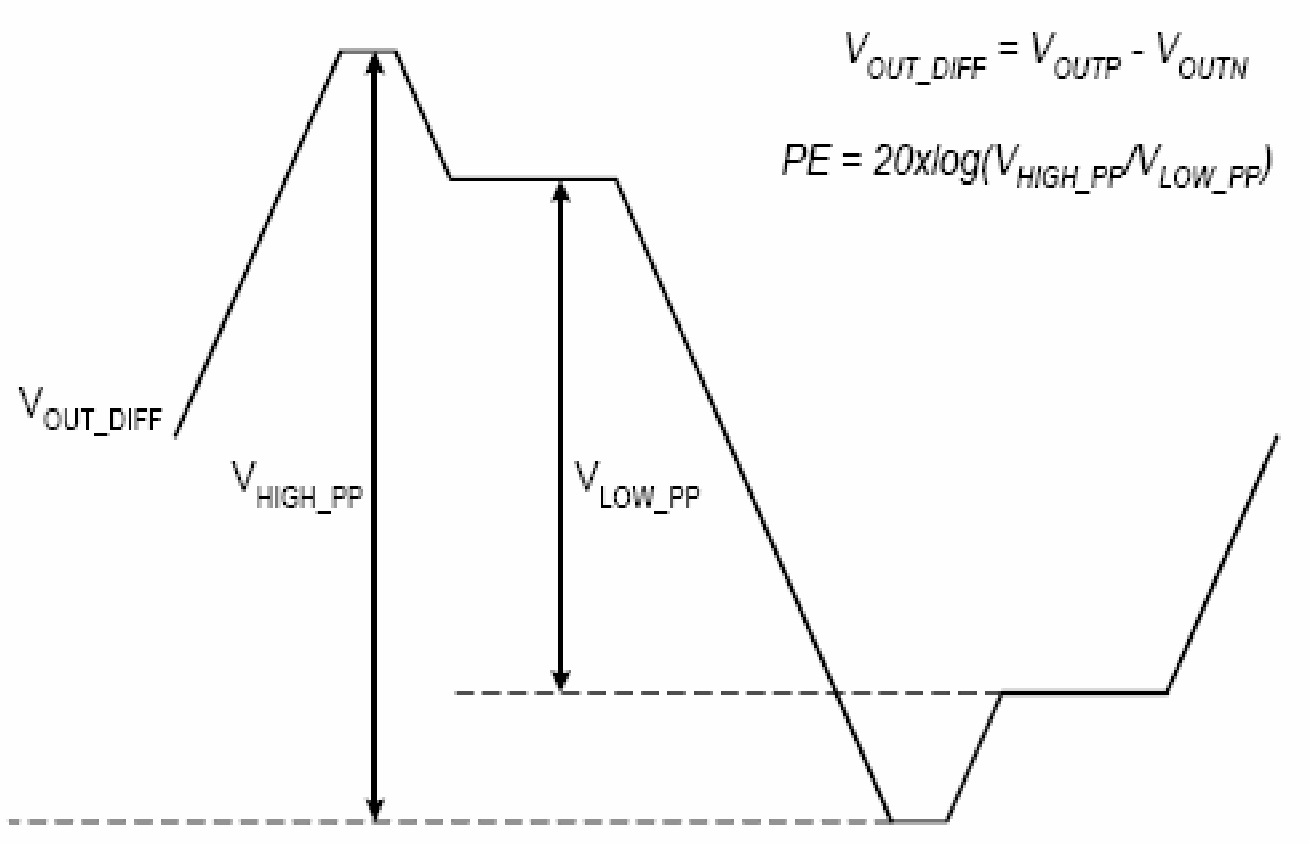
Define Pre-emphasis Values for SR4/SR10 and 40G-LR4 at TP1

- This slide is in support of Comment#329, to add pre-emphasis level into PPI specs for SR4/SR10 or 40G-LR4 at TP1.
  - The pre-emphasis is introduced because PPI TP1 could be critical non-retimed interface between module and host ASIC for SR4/10, and/or 40G-LR4 which has tight jitter budget.
  - Generally assume retimed interface like XL/CAUI, CDR inside module will reset jitter budget.
- Current SFP+ implementation takes advantage of hosted-based transmit pre-emphasis and receive equalization to overcome lossy connector(s) and PCB trace impairments.
  - So its implementation is well-understood and trivial.
- Current suggestion is to insert a row as follows into Table 86-6

  Pre-emphasis level (min)……6dB (or TBD)

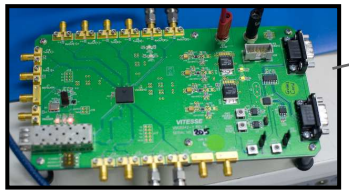
Define Pre-emphasis Values for SR4/SR10 and 40G-LR4 at TP1

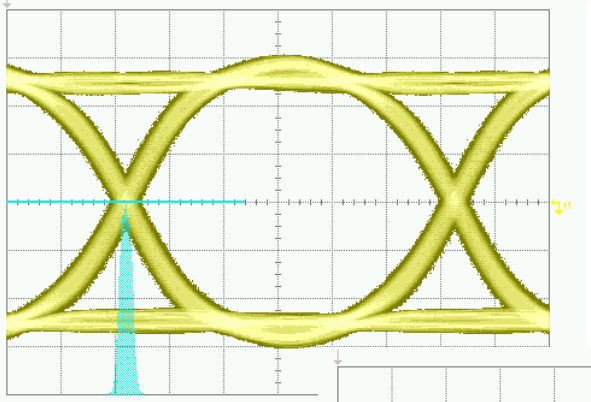
- Transmit Pre-emphasis level definition
  - **PE=20xLOG(V_{High_PP}/V_{Low_PP})**

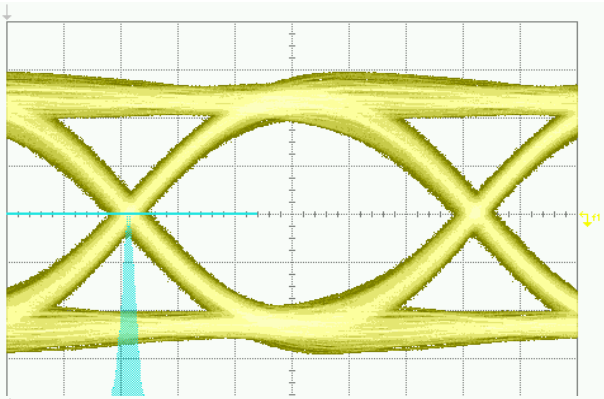


CDR TX Waveforms at Adjusted PE Settings After FR4 Traces up to 8”

Dual/Quad EDC/CDR TX Output: 0” →

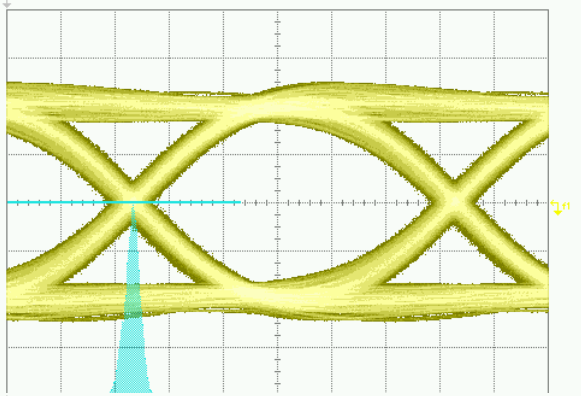


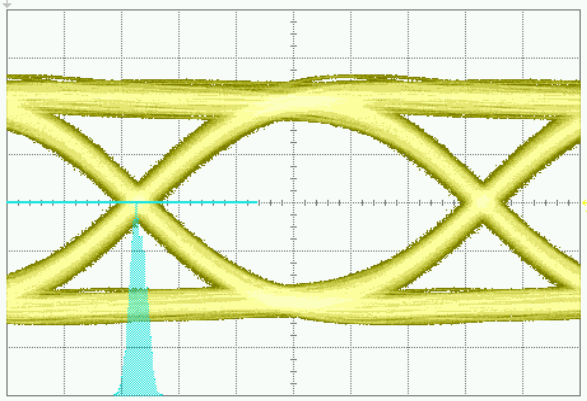




← 2”

4” →





← 6”

8” →