Supporting material for clause 85 Draft 1.1 comments

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Objective

- Technical completion of Clause 85
- Resolve TBDs and Editors notes
- Comments, 302,308,303,296,305,307,306,297, 309 and 663 (Tom Palkert comment).

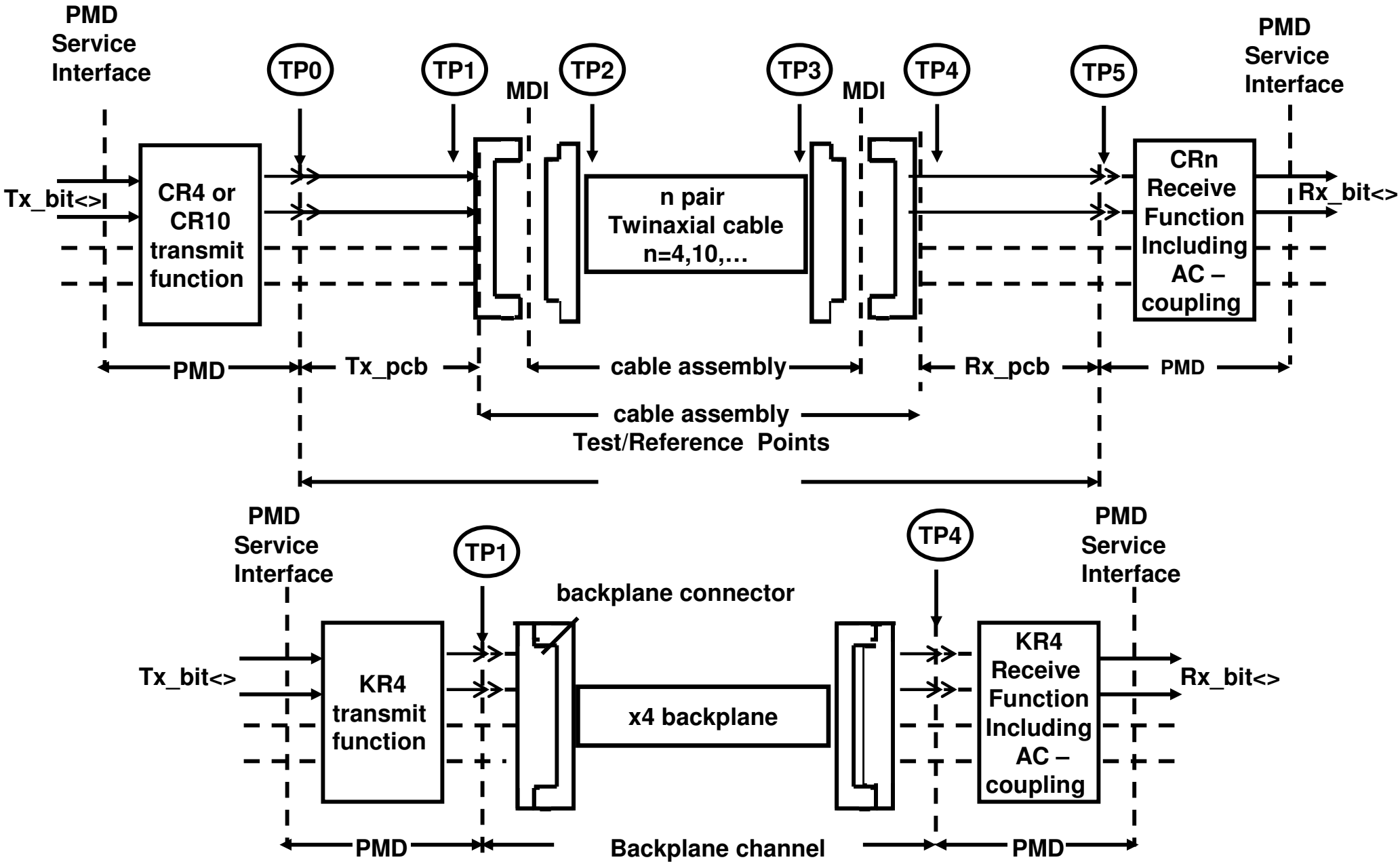
802.3ba CR4 and CR10 Transmitter Specifications and Test Points

Proposal

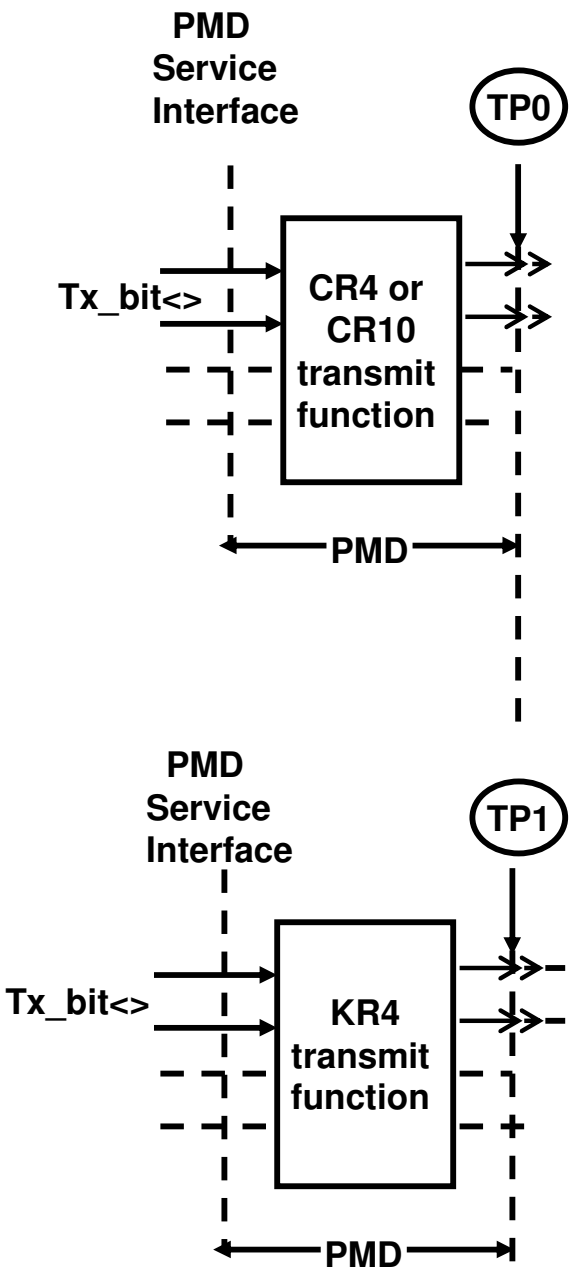
- Table 85-4 Transmitter characteristics to be met at TP0.
  - Draft 1.1. Table 85-4 transmitter characteristics don't change.
  - Common reference point for the transmitter specifications and test fixture definitions for both KR and CR.

- Adjust applicable Table-85-4 transmitter specifications at TP0 to specify TP2.

802.3ba / 802.3ap compare



CR4/CR10 - Transmitter characteristics @ TP0



- CR4 and CR10 transmitter characteristics specified at TP0.
- Remove Table 85-4 TBDs

Table 85–4—Transmitter characteristics' summary

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	85.8.3.3	10.3125 ± 100 ppm	GBd
Unit interval nominal	85.8.3.3	96.969697	ps
Differential peak-to-peak output voltage (max.) with TX disabled	72.6.5 or 85.8.3.x	30(TBD)	mV
Common-mode voltage limits	72.7.1.4 or 85.8.3.x	0–1.9(TBD)	V
Differential output return loss (min.)	72.7.1.5 or 85.8.3.x	[See Equation (72–4) and Equation (72–5)] (TBD)	dB
Common-mode output return loss (min.)	72.7.1.6 or 85.8.3.x	[See Equation (72–6) and Equation (72–7)] (TBD)	dB
Transition time (20%–80%)	72.7.1.7 or 85.8.3.x	24–47 (TBD)	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.8 or 85.8.3.x	 0.15(TBD) 0.15(TBD) 0.035(TBD) 0.28(TBD)	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

CR4/CR10 – Transmitter test fixture @ TP0

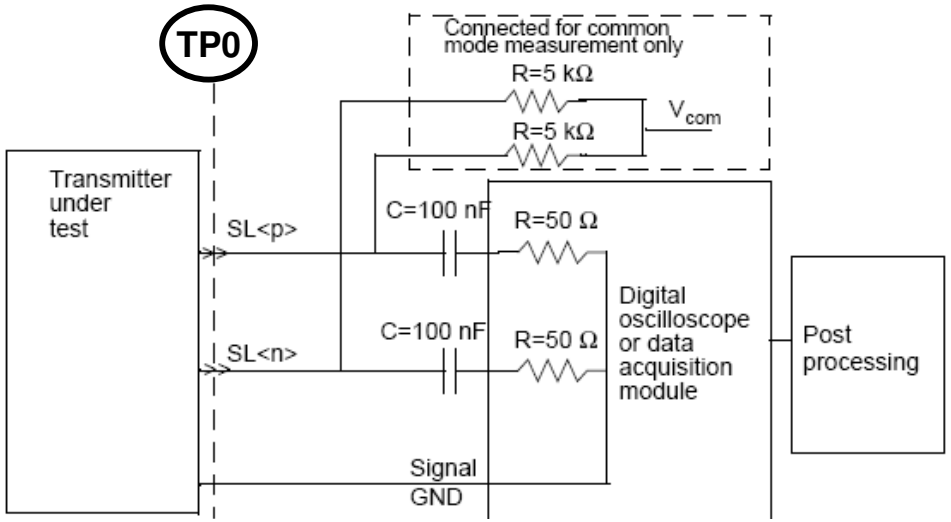


Figure 85–X—Transmit test fixture at TP0

- Replace 85.8.3.1 Test fixtures with Figure 85–X—Transmit test fixture at TP0.

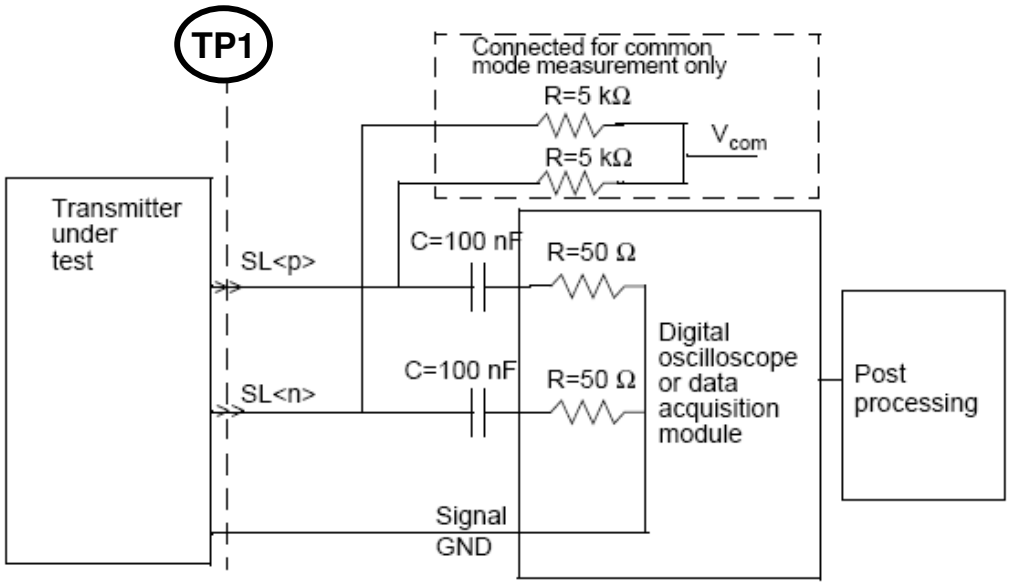


Figure 72–7—Transmit test fixture for 10GBASE-KR

CR4/CR10 - Transmitter characteristics @ TP2

- **CR4 and CR10 transmitter characteristics specified at TP2.**
  - **-Do we need to specify at TP2 in addition to TP0?**
  - **-What to specify?**
  - **-What are the values?**
  - **-Test fixture?**

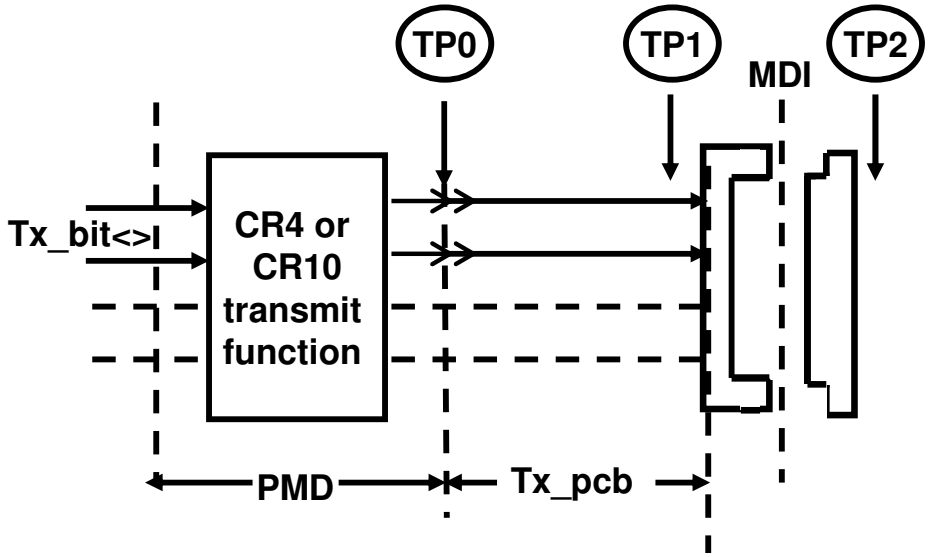


Table-85-X

Parameter	Values
Differential peak-to-peak output voltage (max.) with TX disabled (max.) with TX disabled	NA
Common-mode voltage limits	NA
Differential output return loss (min.)	NA
Common-mode output return loss (min.)	NA
Transition time (20%–80%)	NA
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion Total jitter	

- **Proposal to be provided prior to the meeting.**
- **Adjust applicable Table-85-4 transmitter specifications at TP0 to specify TP2.**

802.3ba CR4 and CR10 Return Loss Comment#663

Contributors

- Chris DiMinico, MC Communications
- Tom Palkert, Luxtera

RL 802.3ba return loss proposal

- **Draft 1.1**

$$Return\ Loss(f) \geq 10 \text{ dB TBD} \qquad (85\text{–}18)$$

for 100 MHz $\leq f <$ 4000 (TBD) MHz.

$$ReturnLoss(f) \geq 10 - 10 \times \log_{10}\left(\frac{f}{4000(TBD)}\right) \text{ dB TBD} \qquad (85\text{–}19)$$

for 4000(TBD) MHz $\leq f \leq$ 10000 MHz.

- **Draft 1.1- comment**

$$\text{Re}\,turnLoss\,(f) \geq 10 \qquad \text{Re}\,turnLoss(f) \geq 10 - 7 \times \log\left(\frac{f}{1250}\right)$$

$$100\ MHz \leq f < 1250\ MHz \qquad 1250\ MHz \leq f \leq 10000\ MHz$$

RL limit comparisons

E.4 SFP+ Passive Direct Attach cable Assembly Specifications

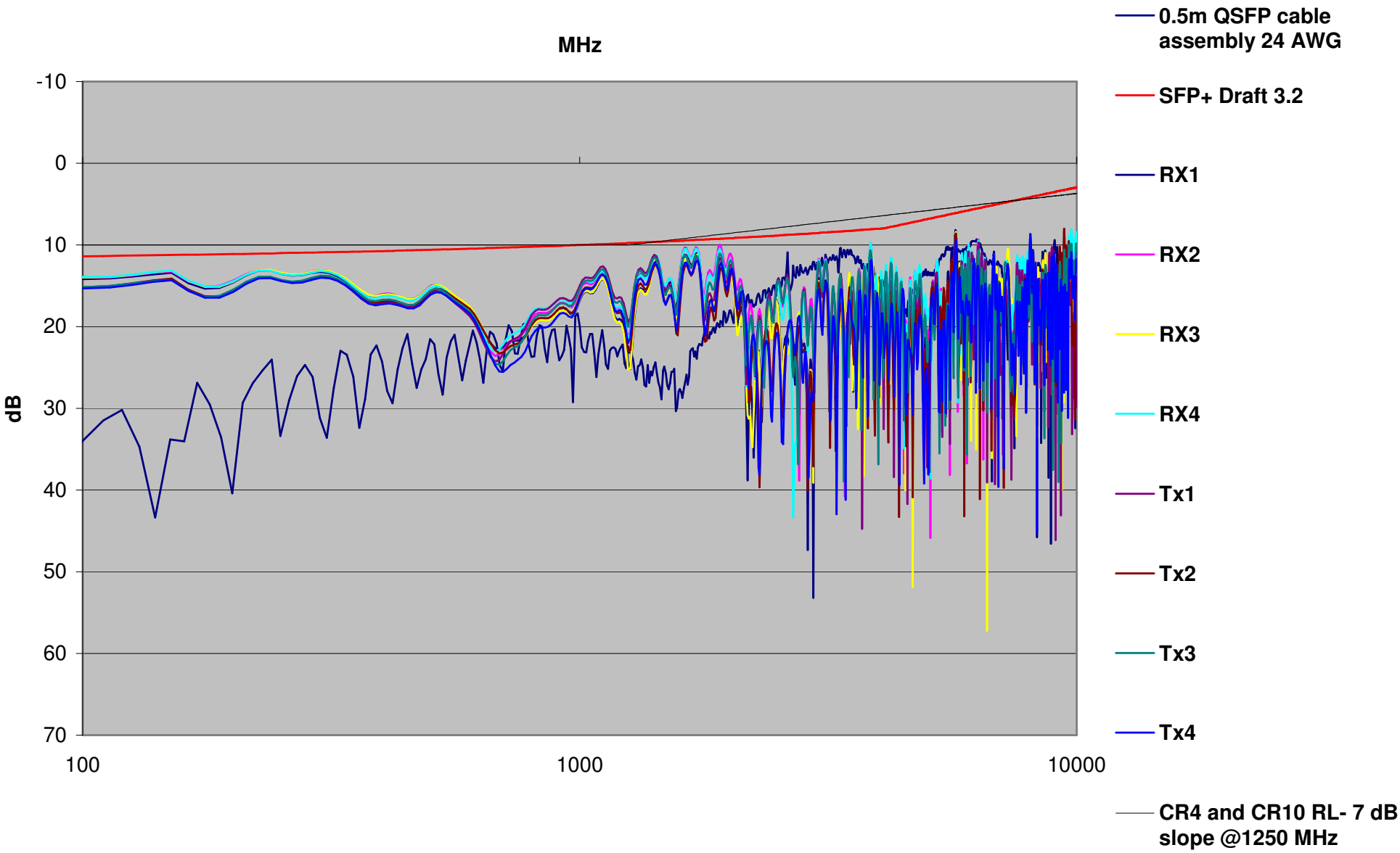
Passive direct attach cables are tested with a pair of module Compliance Boards at compliance point B′ and C′. SFP+ passive cable assemblies need to meet specification in Table 37.

Table 37 10GSFP+Cu Cable Assembly Specifications at B′ and C′

Parameter - C′ (Cable Output)	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Single Ended Input and Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage	Vcm	See 1			13.5	mV (RMS)
Difference Waveform Distortion Penalty	dWDPc	See 2, 9,, E.4.1, E.4.2 and D.14.2			6.75	dBe
VMA Loss	L	See 3, 9, D.7, E.4.4			4.5	dBe
VMA Loss to Crosstalk Ratio	VCR	See 1 D.7, E.4.1, E.4.4	32.5			dB
Differential Output/Input Reflection Coefficient [4]	SDDxx	0.01-4.1 GHz			See 5	dB
		4.1-11.1 GHz			See 6	dB
Common Mode Output/Input Reflection Coefficient [7]	SCCxx	0.01-2.5 GHz			See 10	dB
		2.5-11.1 GHz			See 11	dB
Parameter - B″ (Input Test Conditions)	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Input AC Common Mode Voltage	Vcm	See 1, D.15.1		12		mV (RMS)
Signal Rise and fall time Time	Tr/tf	See D.6		34		ps
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	See D.6		34		ps
Crosstalk Source Amplitude Differential (p-p)				700		mV
WDP_i		See 8		2.4		dBe

1. When input common mode voltage is 12.0 mV RMS and when input rise and fall times are 34ps and the amplitude is the max amplitude allowed by Table 12.
2. Defined with reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps, see Appendix G.
3. VMA loss is the ratio of VMA measured at input and output, respectively.
4. Reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.
5. Reflection Coefficient given by equation SDDxx(dB)= = -12 + 2*SQRT(f), with f in GHz.
6. Reflection Coefficient given by equation SDDxx(dB)= = -6.3 + 13*log10(f/5.5), with f in GHz.
7. Common mode reference impedance is 25 Ω. The dB value listed here are the same as dBe
8. Adjust DDJ and/or DDPWS by adjusting pre-emphasis untill the target WDP_i is achieved.
9. With input test condition given by parameters B″ given in this table.
10. Reflection coefficient given by equation SCC22(dB) < -12 + 2.8*f, with f in GHz.
11. Reflection coefficient given by equation SCC22(dB) < -5.2 + 0.08*f, with f in GHz

802.3ba RL proposal and SFP+ 3.2



802.3ba channel ICR comment#301

Contributors

- Chris DiMinico, MC Communications
- Hiroshi Takatori, PhyCore Technology

Draft 1.0 comments #456 – ICR

Basis of 2.5 dB ICR allocation: IEEE Std 802.3ap™-2007 - 69B.4.6.4 Insertion loss to crosstalk ratio (ICR)

It is recommended that ICR_{fit} be greater than or equal to ICR_{min} as defined by Equation (69B–24).

$$ICR_{fit}(f) \geq ICR_{min}(f) = 23.3 - 18.7\log_{10}\left(\frac{f}{5\ \text{GHz}}\right) \qquad (69B–24)$$

for $f_a \leq f \leq f_b$. ICR_{fit} accounts for the worst-case differences in characteristcs (e.g., amplitude, transition times) between the victim and aggressor transmitters. It also assumes a 3 dB signal-to-noise ratio penalty related to insertion loss deviation.

Add equation: ICRfit(f)>/=ICRmin(f)=23.3-18.7*LOG((f*10^6)/(5*10^9))-2.5 (TBD) dB

Note: 2.5 dB of the 3 dB signal-to-noise ratio penalty related to insertion loss deviation embodied in 802.3ap ICRmin is applied as 2.5 dB ICRmin margin to account for reduction in ILD penalty for CR4 and CR10

Draft 1.0 Comment #457 – Cable assembly ILD

Comment # 457
Add cable assembly ILD specifications to limit cable assembly ILD. Add TBD to equation as contributions from IL and power sum crosstalk to ICR under consideration.

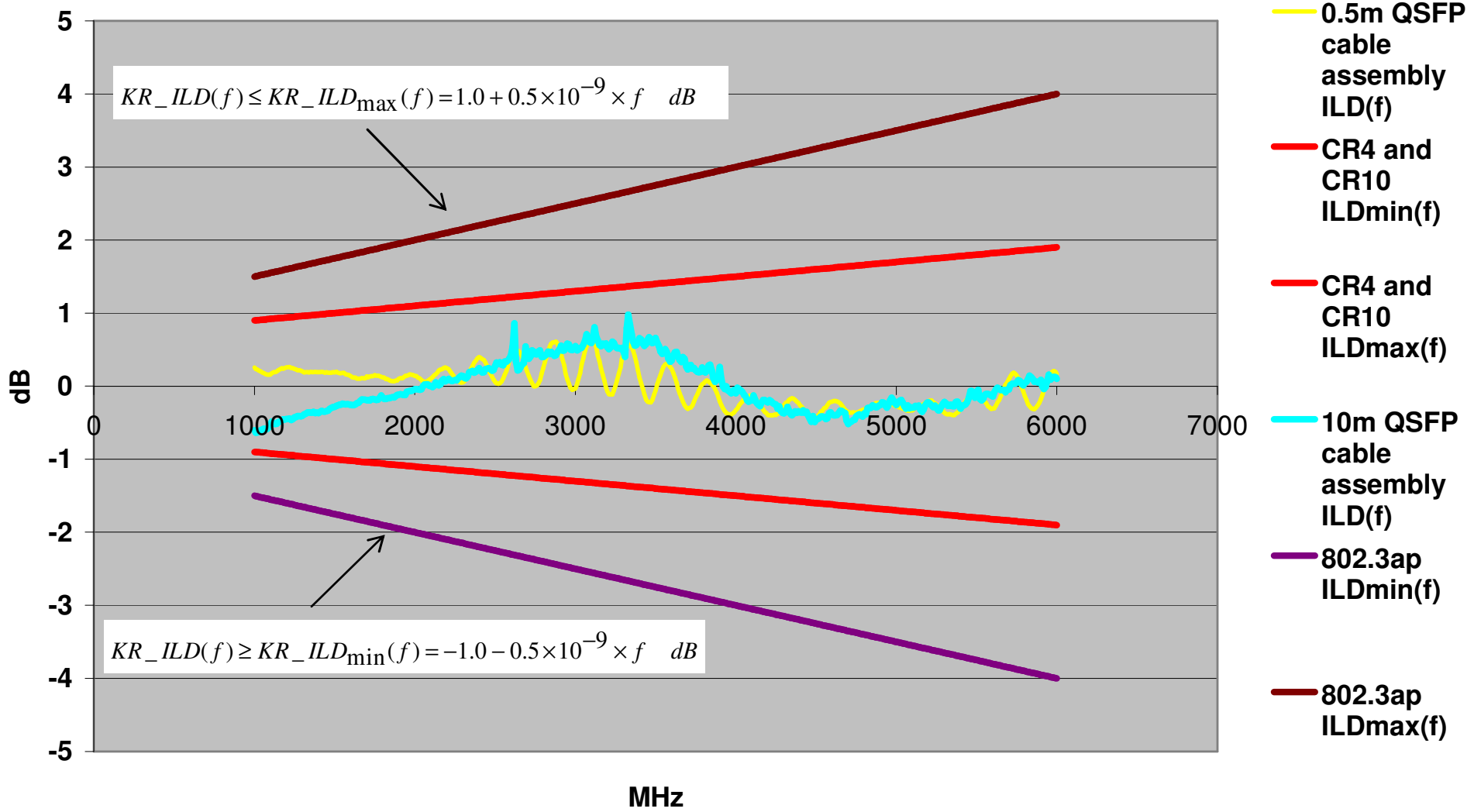
The cable assembly insertion loss deviation is the difference between the cable insertion loss and the fitted insertion loss determined using Equation (85-x).
ILD(f) = IL(f) – ILfitted(f) (85-x)

The ILD shall be within the region bounded by the following equations:

ILDmax= 0.7(TBD)+0.2(TBD)*10^-9*(f*10^6) TBD dB
ILDmin= -0.7(TBD)-0.2(TBD)*10^-9*(f*10^6) TBD dB
1000 MHz</=f</= 6000 MHz

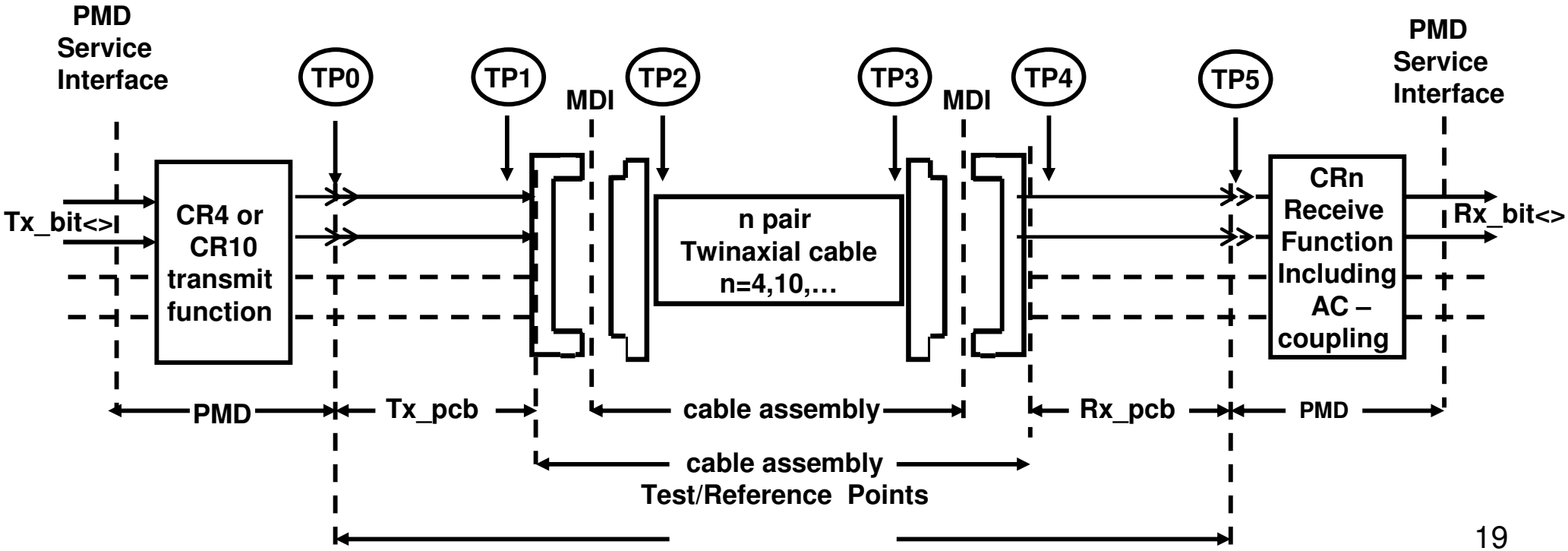
Draft 1.0 comments #457 – Cable assembly ILD

802.3ap ILD vs CR4 and CR10 ILD 0.5m and 10m cable assembly

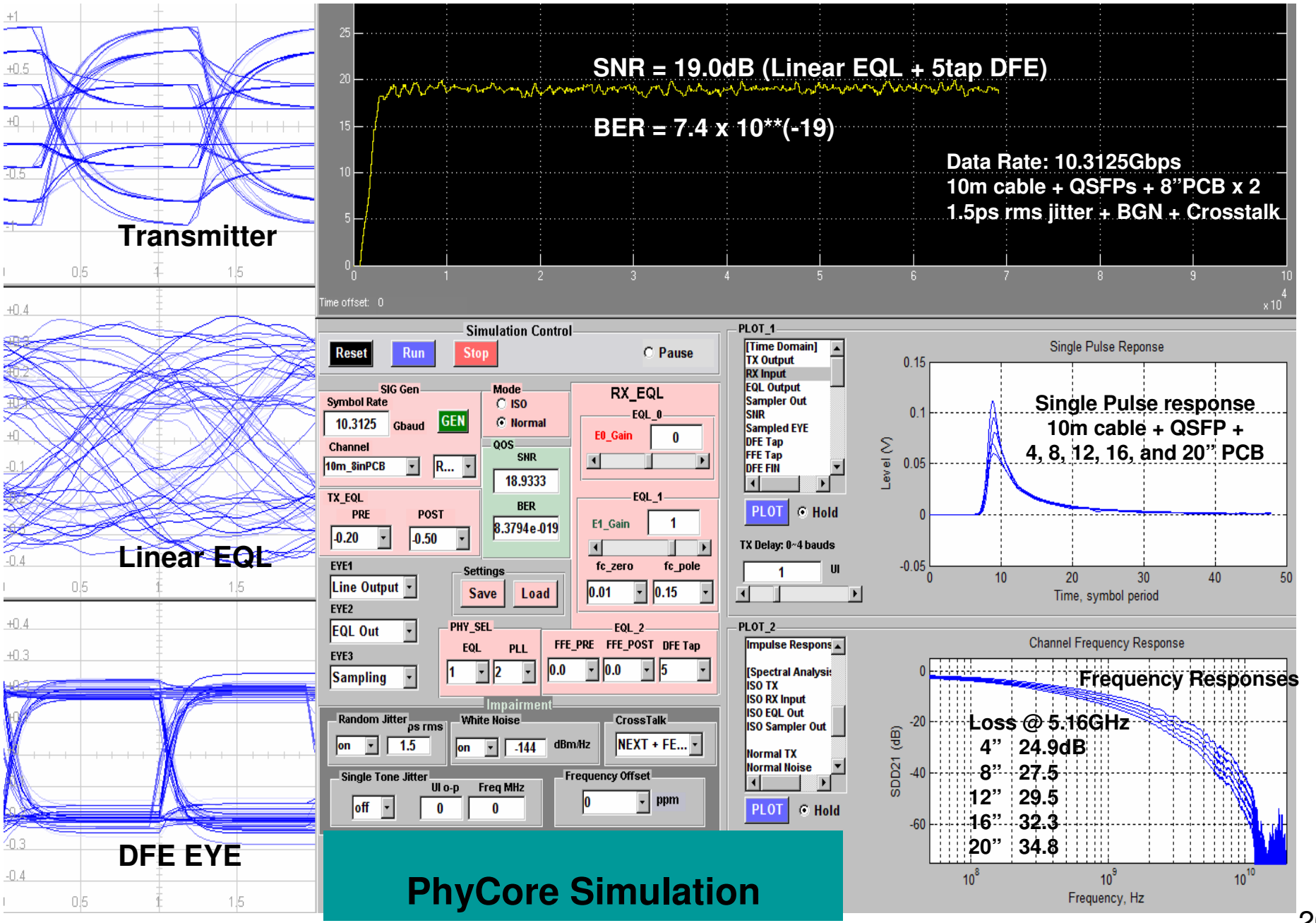


Supporting analysis

PCB per end	PCB total	TP0 -TP5 (dB)	SNR (dB)
2”	4”	24.9	21.2
4”	8”	27.5	20.7
6”	12”	29.5	19.7
8”	16”	32.3	19.0
10”	20”	34.8	18.0



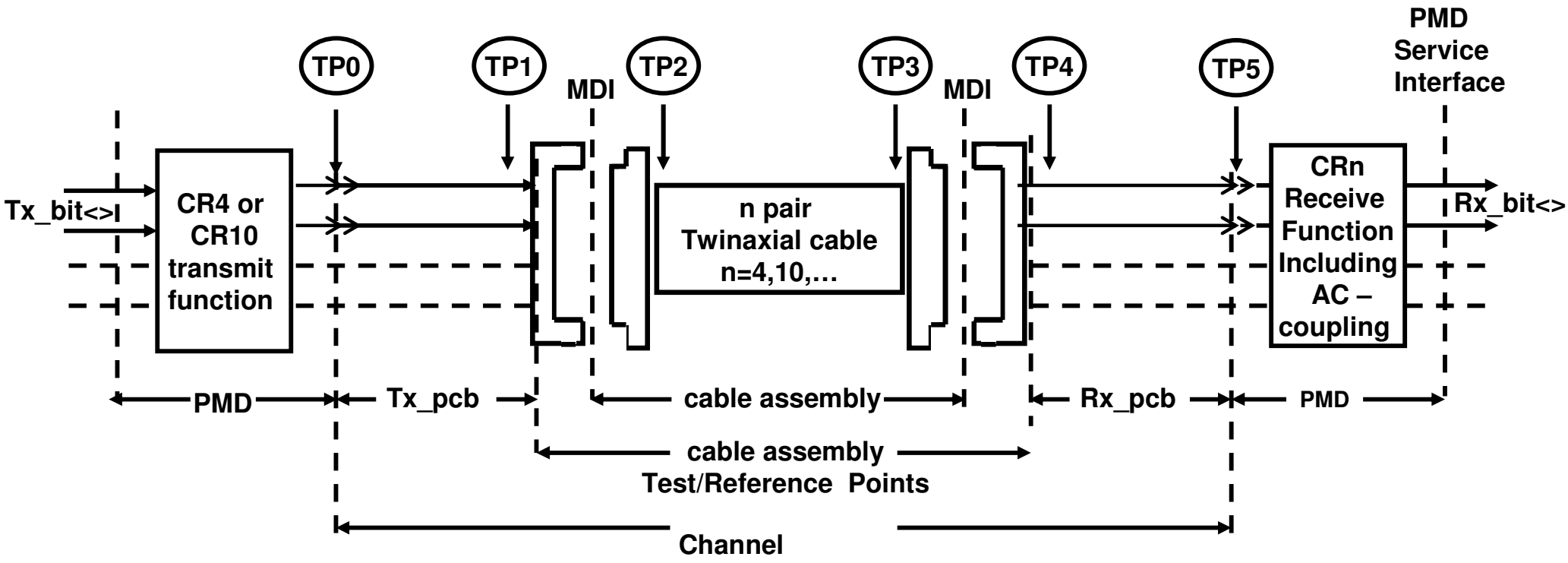
PhyCore simulations



PhyCore Simulation

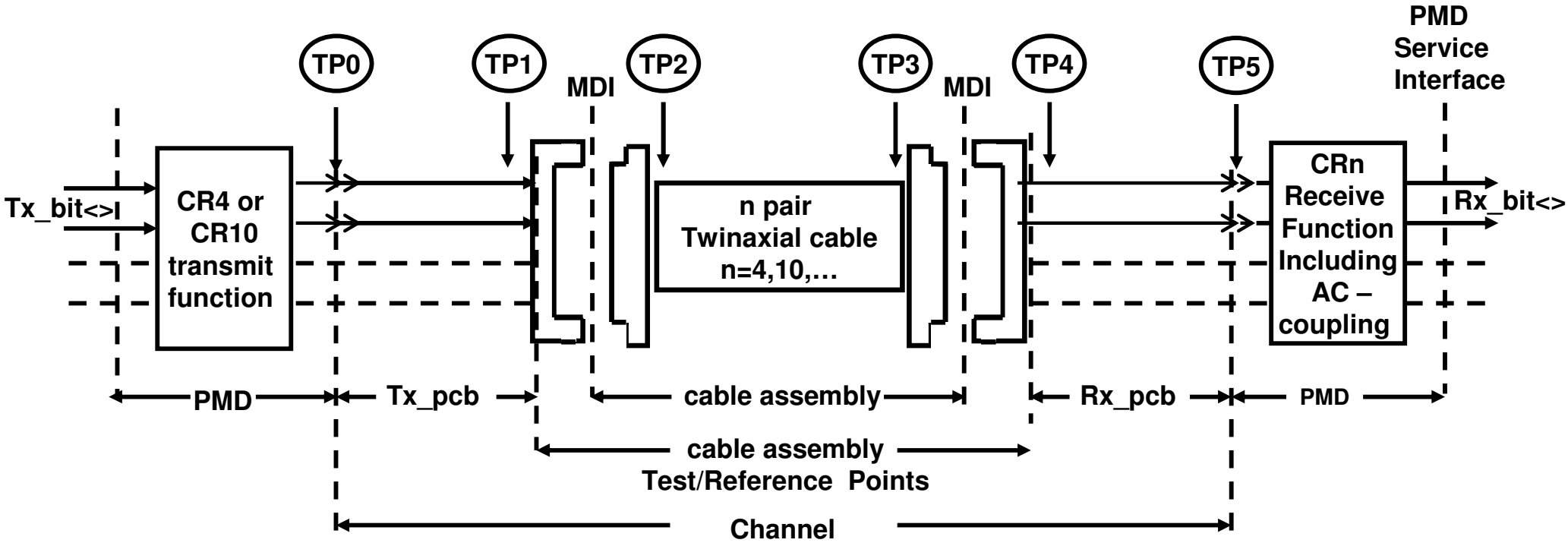
Backup material

802.3ba IL allocation



Description	dB
Maximum PCB insertion loss at 5.15625 GHz (4 in Amax) –TP0 to TP1	2.4
Maximum connector insertion loss at 5.15625 GHz – TP1 to TP2	
Maximum cable assembly insertion loss at 5.15625 GHz –TP1 to TP4	21.55
Maximum channel insertion loss at 5.15625 GHz – TP0 to TP5	26.30

802.3ba IL allocation



$$ILpcb\ (f) \le ILpcb\ (f) = Tx\_pcb + Rx\_pcb$$

$$ILpcb\ (f) \le ILpcb\ (f) = (0.2032) \times \left[20 \times Log_{10}(e) \times \left(b_1 \sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3 \right) \right]$$

$$ILchannel\ (f) \le ILchannel\ (f) = ILcable\_asssembly + Tx\_pcb + Rx\_pcb$$

$$ILcable\_assembly\ (f) \le 0.192749 \times \sqrt{f} + 0.001494 \times f$$

$$100\ MHz \le f \le 6000\ MHz$$