nAUI TBD Closure

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Agenda

1. BER Objective
2. Rise / Fall time
3. De-emphasis
4. Jitter Methodology
5. Channel Definition

BER Proposal

- Baseline BER 10^{-12} in Annex 83A
  - **83A.3.4.1 Bit error ratio:** The receiver shall operate with a BER of better than 10^{-12} in the presence of a reference input signal as defined in 83A.3.4.2
- Add informative section to Annex 83A on how to enable a BER of 10^{-15}
  - BER=10^-15 is achieved by using the same DJ and TJ number in UI for Tx and Rx.

83A.3.3.2 Rise / Fall Time

- Rise and fall times are measured from the 20% to the 80% levels of the differential voltage level. Note that, with de-emphasis, the voltage thresholds corresponding to 20% and 80% vary depending on the voltage level of the previous UI. Only those transitions crossing the zero threshold need to meet TR/TF limits defined in Table 83A-1. In Figure YYY, there are three distinct thresholds corresponding to deemphasized transitions from high to low, low to high, and full swing transitions in either direction. Rise / Fall Time must be validated for all four possible cases.

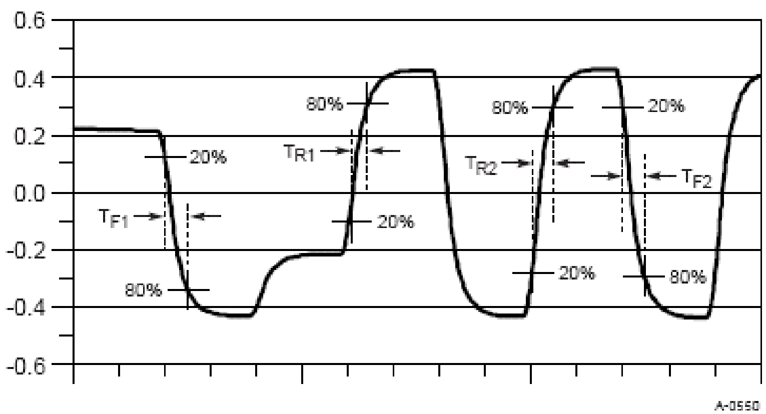


Figure YYY

De-Emphasis

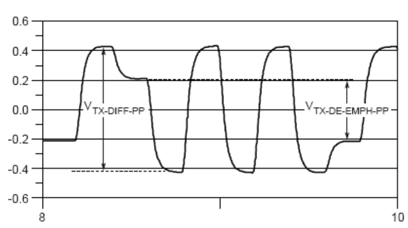
- Add row to Transmitter Characteristics Table 83A-1

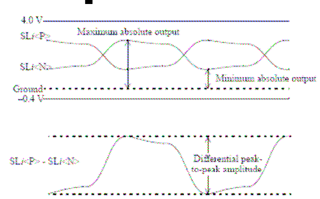
Parameter	Value	Units
Minimum De-emphasis	3.5	dB

- 83A.3.3.1 Output amplitude Text:
- Driver differential output amplitude including transmit equalization shall be less than Y2 and greater than Y1 as defined in 83A-1. DC referenced logic levels are not defined since the receiver is AC-coupled. Single-ended output voltage range shall be between –0.4 V and 4.0 V with respect to ground.
- De-emphasis shall be the ratio between the amplitude following a transition and the amplitude during a non-transition bit as seen in equation EEE. Amplitude measurements are taken using an averaged waveform and taken at the center of the respective UI.
- See Figure 83A–3 for an illustration of absolute driver output voltage limits, definition of differential peak-to-peak amplitude, and definition of pre-emphasis.

$$V_{TX\text{-}DE\text{-}RATIO} = -20\log_{10}(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$$

Equation EEE





[SLi<P> and SLi<N> are the positive and negative sides of the differential signal pair for lane i (i = 0, 1, 2, 3 for XLAUI. For CAUI i = 0:9)]

Figure 83A–3—Driver output voltage limits and definitions

Figure 83A-3 Update

Jitter Methodology

- **83A.5.2.1 Transmit jitter**

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The data pattern for jitter measurements shall be test patterns 1 or 2 as defined in Clause 83. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal. Equalization shall be off during jitter testing. All XLAUI / CAUI channels shall be active during transmit jitter testing to ensure any channel-channel crosstalk is included in the jitter evaluation.

Jitter Methodology

- Table 83A-2 Receiver Characteristics
  - Update Maximum Non-EQ definition to Maximum Deterministic Jitter
- **83A.3.4.8 Jitter tolerance**
- The XLAUI/CAUI receiver shall have a peak-to-peak total jitter amplitude tolerance of at least 0.62 UI. This total jitter is composed of two components: Deterministic jitter and Random Jitter. Deterministic jitter tolerance shall be at least 0.42 UIp-p. The XLAUI/CAUI receiver shall tolerate sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 83A–10. This sub-component of Deterministic jitter is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects.
- **83A.5.2.2 Jitter Tolerance (Test Requirements)**
- XLAUI / CAUI Jitter tolerance evaluation shall be conducted with a stressed input signal which is comprised of at least 0.42UIpp deterministic jitter, and 0.2UIpp random jitter. Deterministic jitter is added to a clean test pattern by adding sinusoidal jitter as defined in 83A.3.4.8, along with low pass filter stress, followed by a limiting function, and FR4 trace stress. The low pass filter stress is added until the 0.32UIpp deterministic jitter is achieved. FR4 trace stress is then added until 0.42UIpp deterministic jitter is achieved. Random jitter is added to the test signal using a interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from *50MHz* to *6GHz* with a crest factor of no less than 5. Figure ZZZ depicts the XLAUI / CAUI Jitter Tolerance test setup. The amplitude and output jitter of the filter stress + Limiter and Random Jitter Injection shall meet the minimum receiver eye mask defined in 83A-2. All XLAUI / CAUI Channels shall be active during jitter tolerance testing

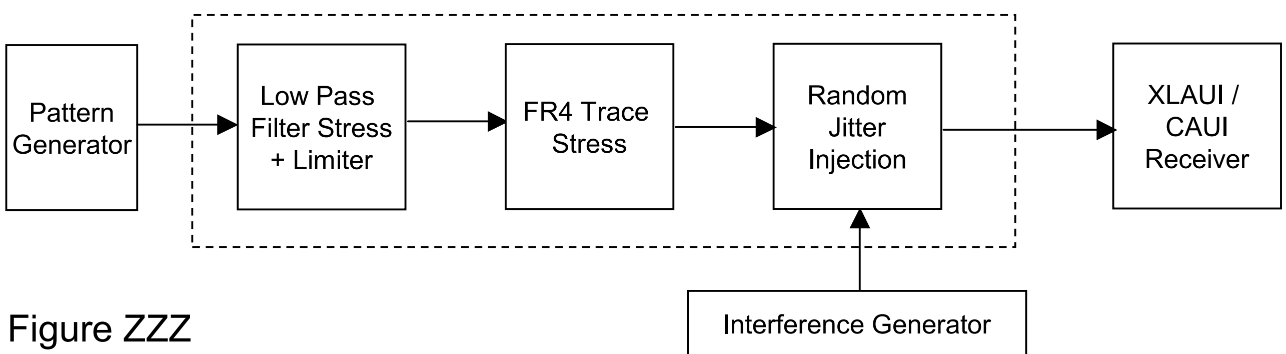
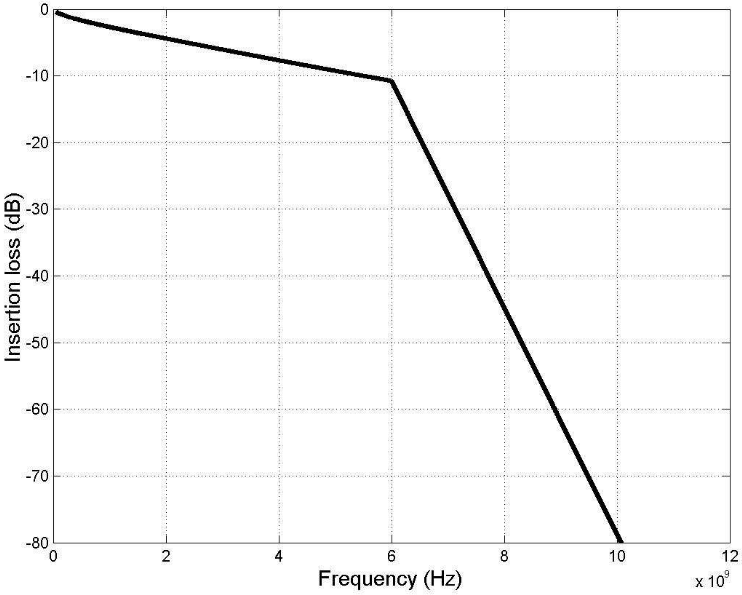


Figure ZZZ

83A.4 Interconnect Characteristics (Informative)

- This section describes informative characteristics which are used to describe an XLAUI / CAUI channel.
- The informative values for insertion loss are summarized in table YYY and equation ZZZ. Other impairments such as crosstalk can have a material impact on the link performance and should be minimized

Parameter	40/100G XLAUI/CAUI	Units
b_1	-6.52e-006	
b_2	-9.55e-011	
b_3	-8.17e-021	
b_4	6.06e-031	
f_1	0.05	GHz
f_2	6	GHz
f_{max}	11.1	GHz



$$S21(f) \le S21_{\max}(f) = 20\log_{10}(e) \times \left(b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3\right)$$

$$\text{for } f_1 \le f \le f_2$$

$$S21(f) \le S21_{\max}(f) = S21(f_2) - 1.7 \times 10^{-8}(f - f_2)$$

$$\text{for } f_2 \le f \le f_{\max}$$