PCS Lane Error Check (BIP-8) Proposal

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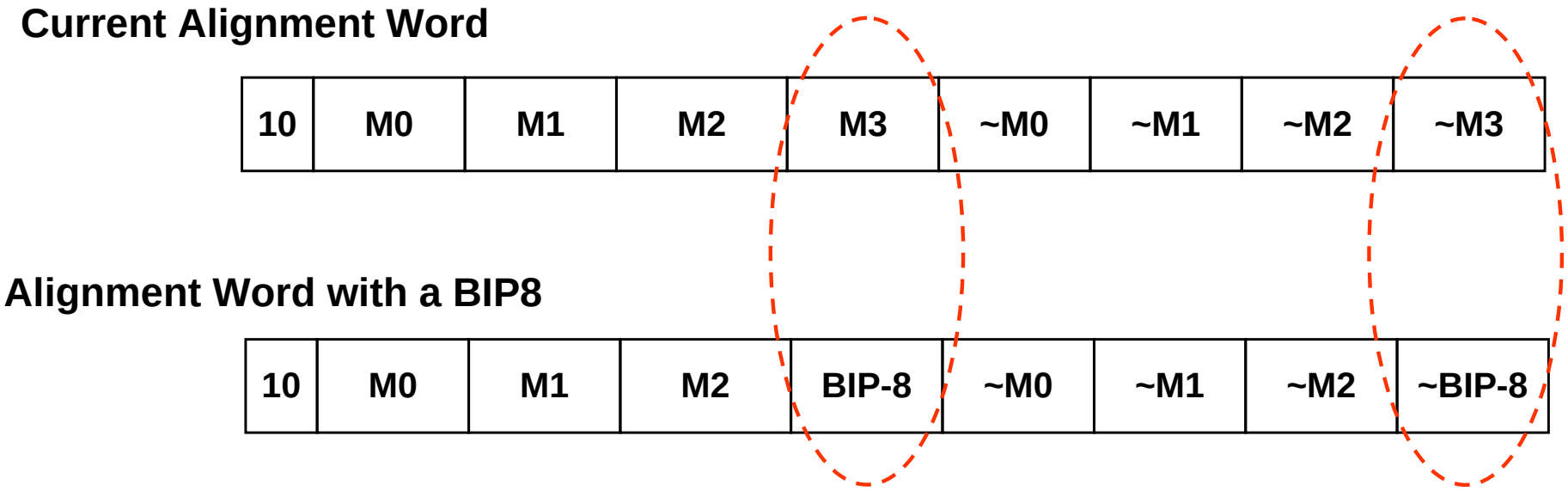
Introduction

- Several customers have commented that while counting sync header errors (nicholl_02_0508 and implemented in D1.1) is very useful for monitoring (estimating) the long term bit error rate on a link, it does not provide a direct method to detect isolated and/or infrequent error events.
- This presentation proposes to address this requirement by adding a simple BIP-8 error check per PCS lane.

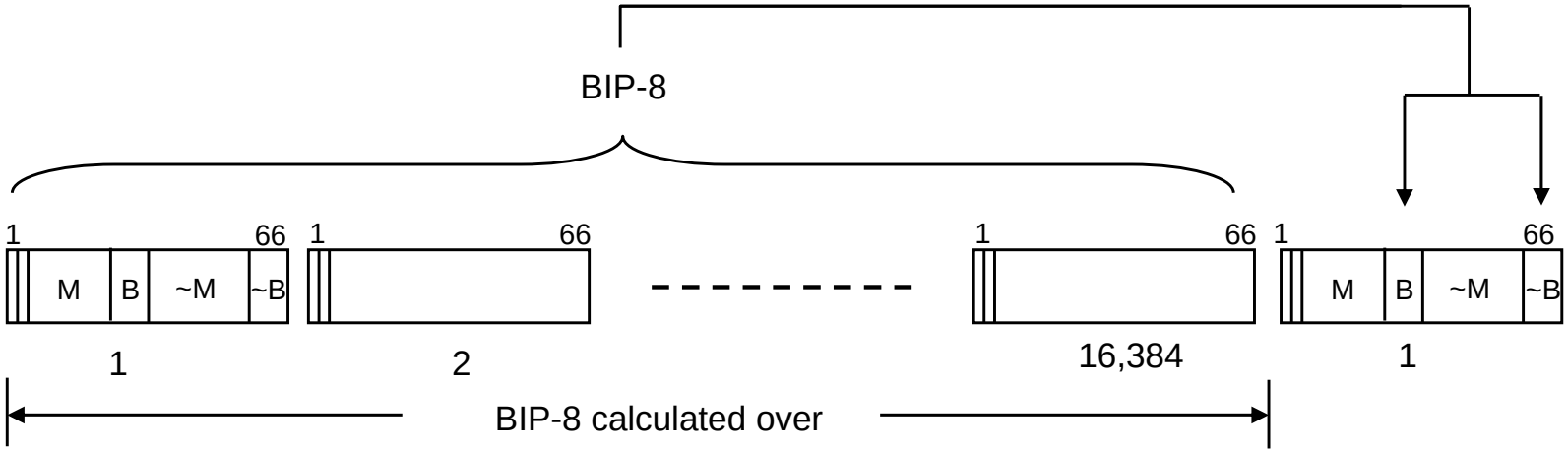
PCS Lane BIP-8 Proposal

- Add a simple BIP-8 (bit interleaved parity) check per PCS lane
- The BIP-8 is carried in the alignment marker, and replaces the current M3 byte.



PCS Lane BIP-8 Coverage

- BIP-8 is calculated over all bits of an alignment marker and subsequent blocks up to (but not including) the next alignment marker and then inserted into the next alignment marker as shown below.
- Sync header bits 0/1 are covered by bits 4/3 of the BIP-8



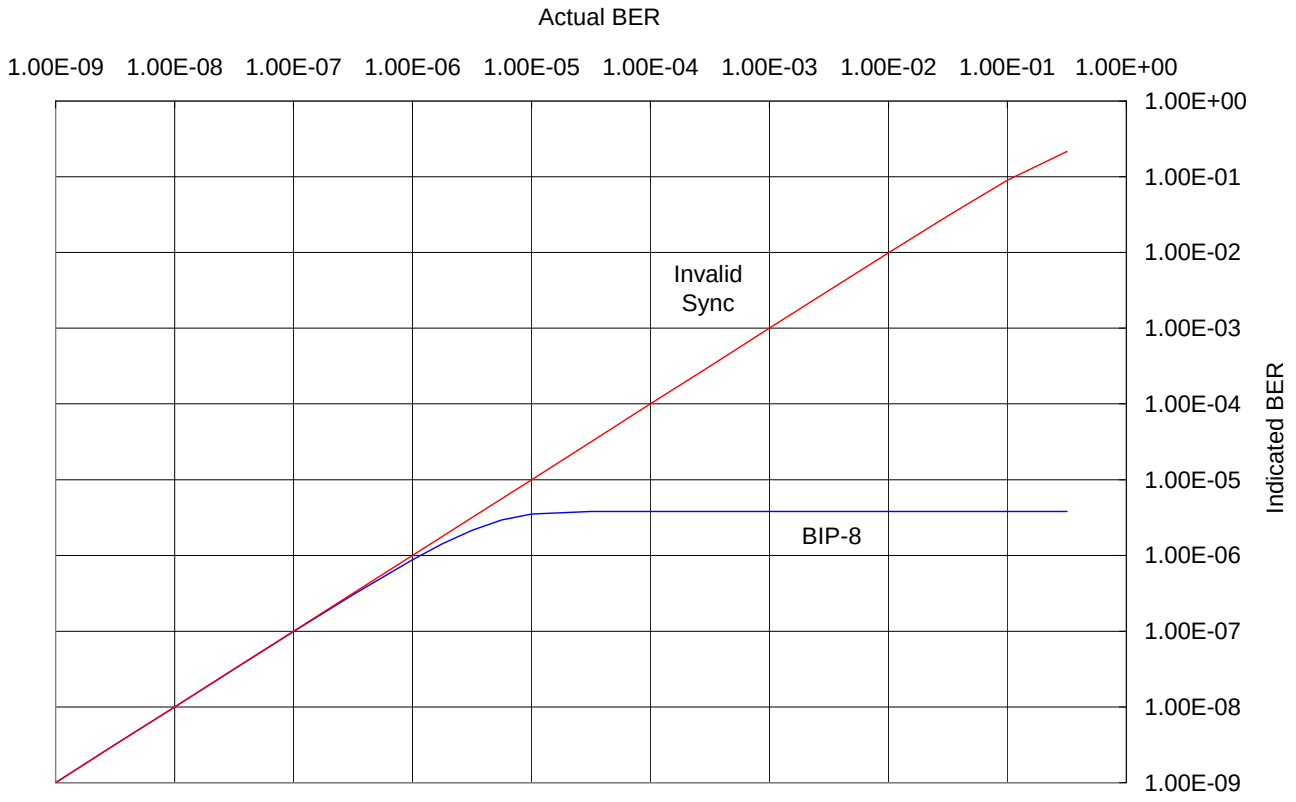
BIP-8 bit7: even parity over bit 7 of all the octets
BIP-8 bit6: even parity over bit 6 of all the octets
BIP-8 bit5: even parity over bit 5 of all the octets
BIP-8 bit4: even parity over bit 4 of all the octets and all of the sync 0 bits
BIP-8 bit3: even parity over bit 3 of all the octets and all of the sync 1 bits
BIP-8 bit2: even parity over bit 2 of all the octets
BIP-8 bit1: even parity over bit 1 of all the octets
BIP-8 bit0: even parity over bit 0 of all the octets

PCS Lane BIP-8 Reporting

- The BIP-8 proposal is not intended to impact any existing state machines
- No consequent actions shall be driven based on detected BIP-8 errors
- BIP-8 errors shall simply be counted and reported to the user over the MDIO interface (in the same way as sync header errors, CRC errors, etc)
- A suitably sized counter shall be allocated in the MDIO memory space for each PCS lane, to ensure that the counter will not saturate (overflow) even if polled at a rate of once per second.

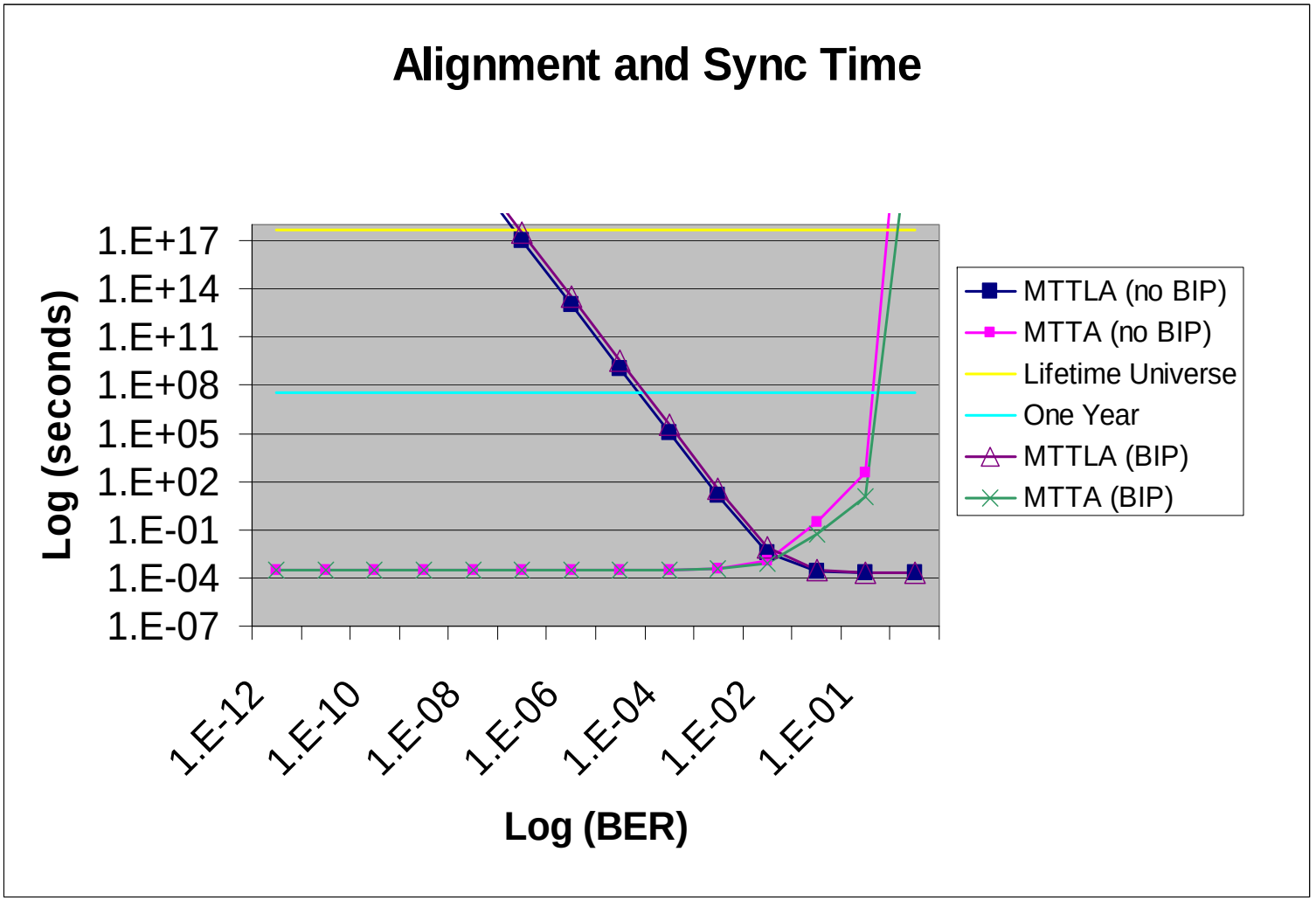
BIP-8 vs Sync violation performance

- BIP-8 accurate up to about 1E-6 BER (after which it saturates)
- Sync header violations accurate up to about 1 in 10 BER but have to wait 33 times longer at low BER for same uncertainty as BIP-8
- BIP-8 also has the advantage that it can detect all isolated error events (up to a 5 bit error burst), which sync header violations cannot (since they are based on only sampling 2 out of every 66 bits)



Impact on PCS Lane alignment ?

- Stealing M3 (~M3) for a BIP-8 means that the PCS lane alignment has to be performed on a marker composed of 6 rather than 8 bytes, but this makes no difference to the performance:



Implementation Complexity

- Trivial …
- 16 extra flip-flops (8 for TX, 8 for RX) and a handful of XOR gates per PCS lane (Farhad Shafai)
- ~ 0.25% increase in MAC/PCS gate count
- Already verified in hardware (Farhad had coded, debugged and verified the feature within one hour of receiving the proposal !)

Summary

- BIP-8 provides a simple method for quickly detecting (all) isolated and infrequent error events
- BIP-8 is well understood and widely used in the industry
- Complexity is very low (~ 0.25% increase in gate count)
- Implementation is trivial (already verified)
- No impact to the performance of the alignment statistics