XLAUI/CAUI Jitter Tolerance Test Proposal

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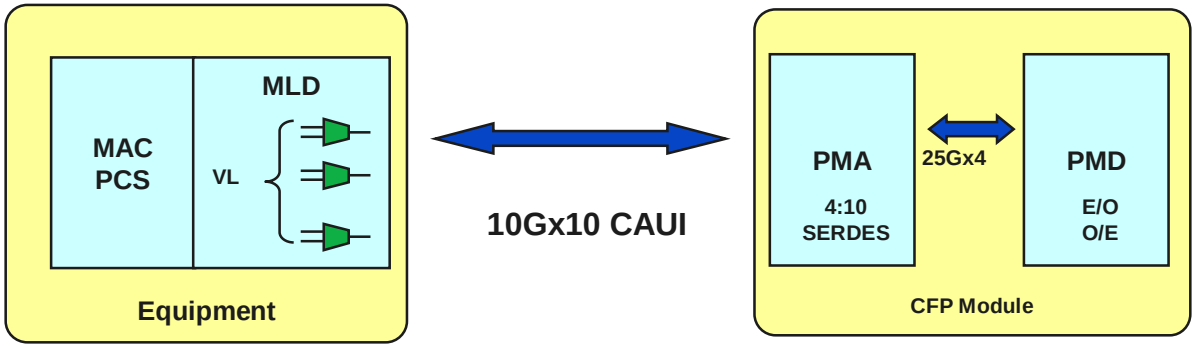
Introduction

* There are two Editor's Note on 83A 5.2.2.
* Those are interference tolerance test and jitter tolerance test pattern.
  This proposal resolves these two unclear items.

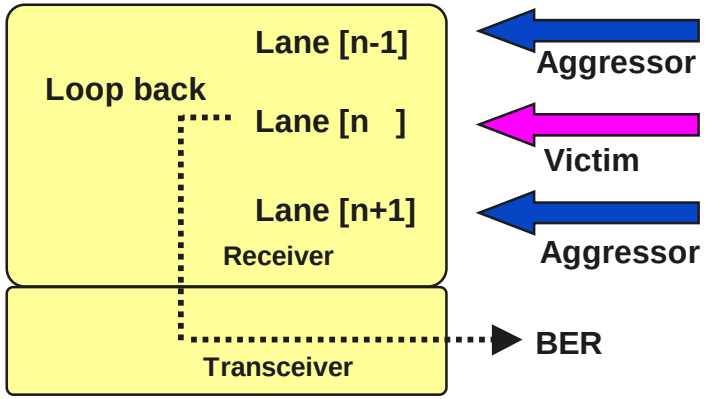


83A.5.2.2 Jitter tolerance

[Editor's note: (to be removed prior to publication) - An interference tolerance test is required]

[Editor's note: (to be removed prior to publication) -In addition to PRBS31, consider including appropriate patterns when performing jitter measurements e.g., MLD and other representative patterns.]

Interference tolerance test system proposal



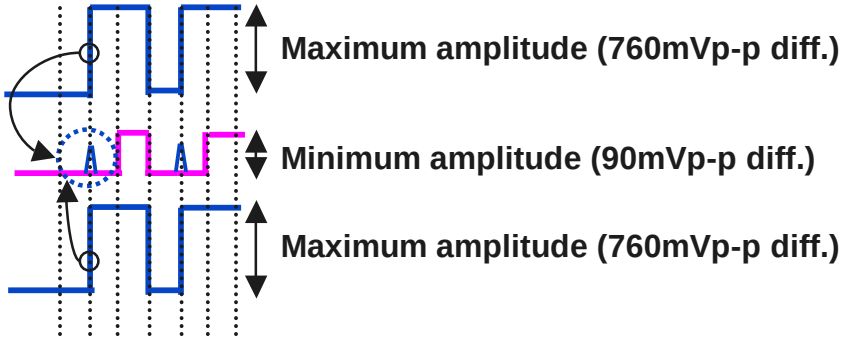


Table 83A–1—Transmitter characteristics

Parameter	Value	Units
Signalling speed per lane (range)	10.3125 ± 100 ppm	GBd
Single-ended output voltage range maximum minimum	 4.0 –0.4	 V V
Maximum Differential Output Voltage, peak-to-peak	760	mV

Table 83A–2—Receiver characteristics

Parameter	Value	Units
Signalling speed per lane (range)	10.3125 ± 100 ppm	GBd
Minimum Differential Input Voltage, p-p	See receiver eye mask definition	mV
Receiver eye mask definition Y1[d]	45	mV

* At least two aggressors and a victim.
  - Same timing
* Aggressors
  - Maximum amplitude
  - Same pattern PRBS 23
* A victim
  - Minimum amplitude
  - PRBS 31

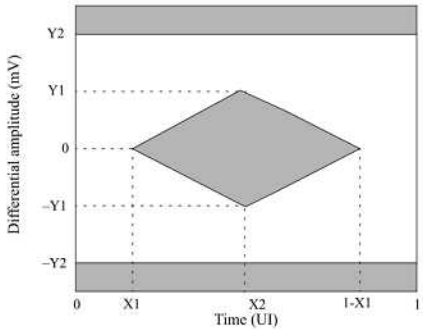


Figure 83A–7—Receiver template

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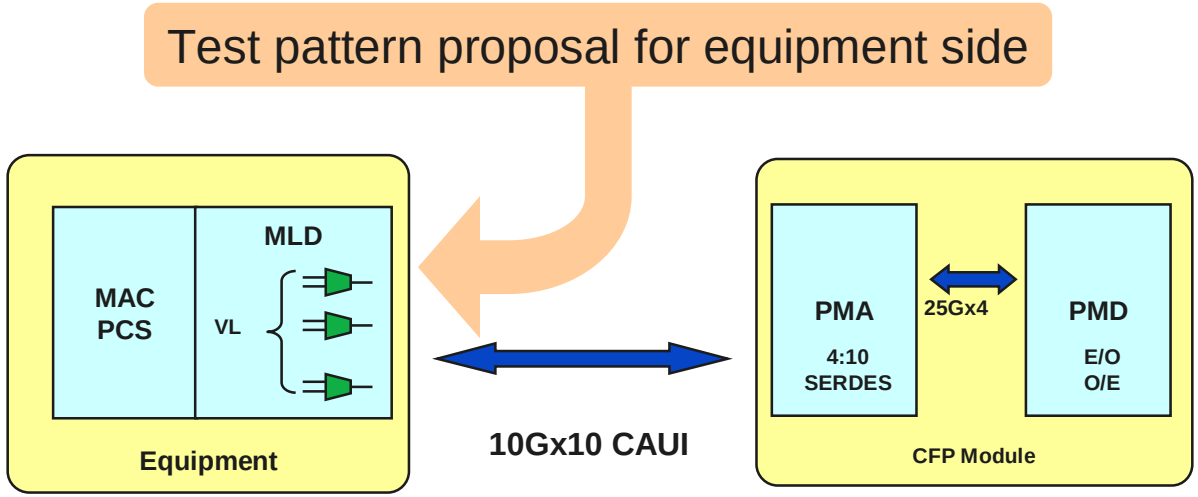
Jitter Tolerance Test Pattern Proposal

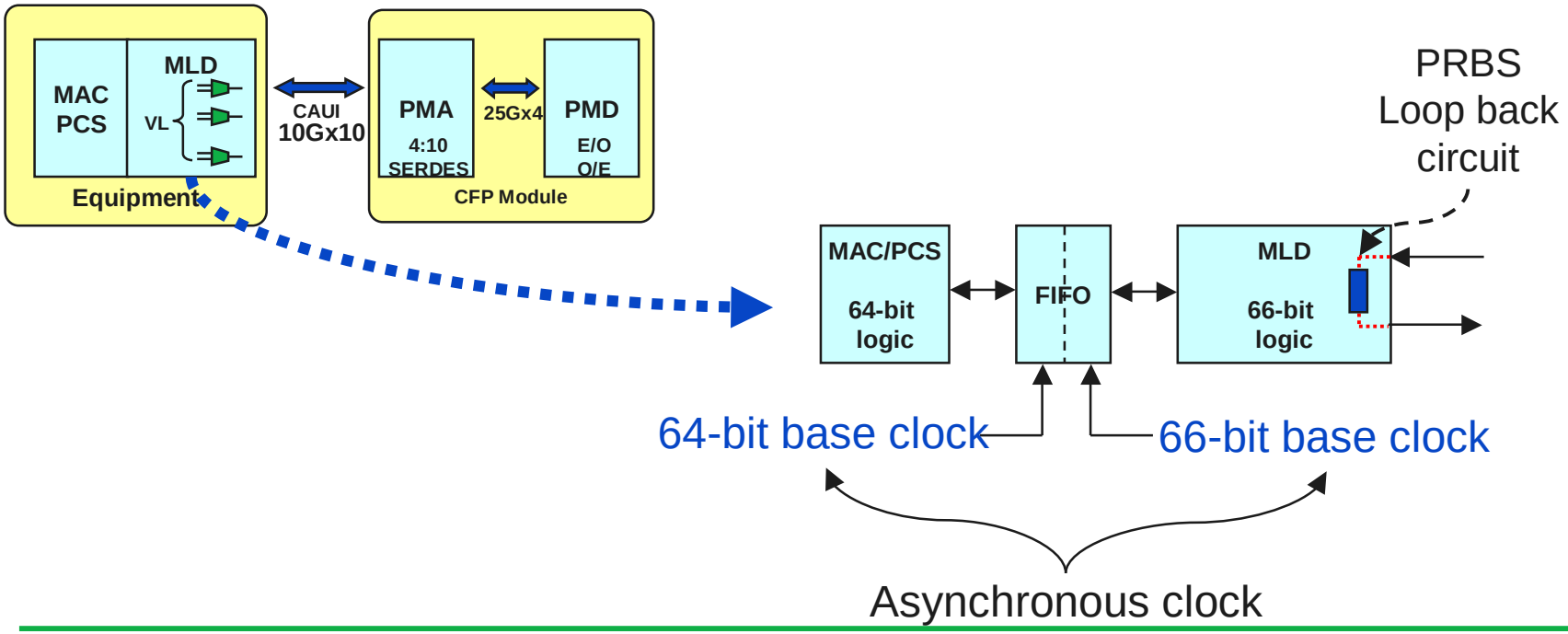
* PRBS31 is good enough for testing jitter tolerance of optical module side. It is just simple physical characteristics test.

* For equipment side, test pattern should be included “Alignment Marker” to drive alignment circuit.



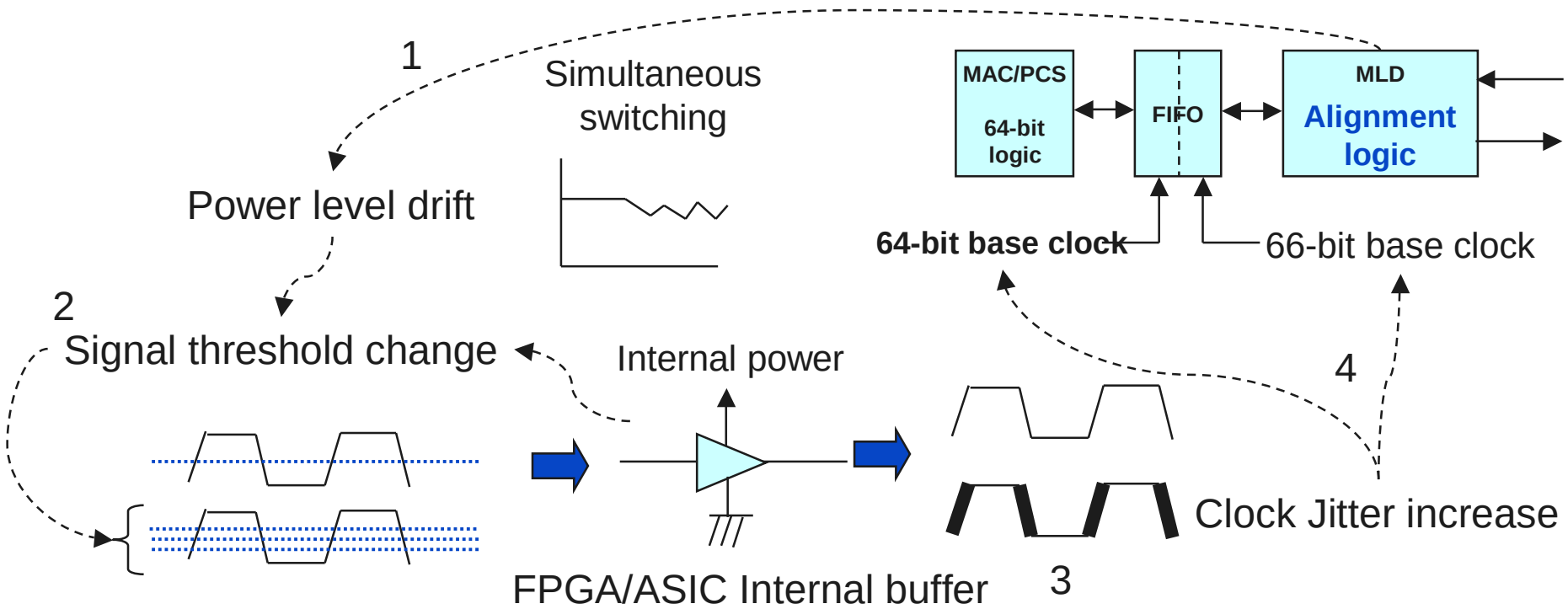
Equipment Circuit Assumption

* Equipment circuit assumptions
  - Skew alignment must be huge logic circuit.
  - During PRBS loop back circuit works, alignment circuit does not work.
  - PRBS Loop back circuit is smaller than skew alignment circuit.
  - The circuit uses at least two asynchronous clocks (64-bit and 66-bit logic).



Increasing jitter inside of large scale logic circuit -1

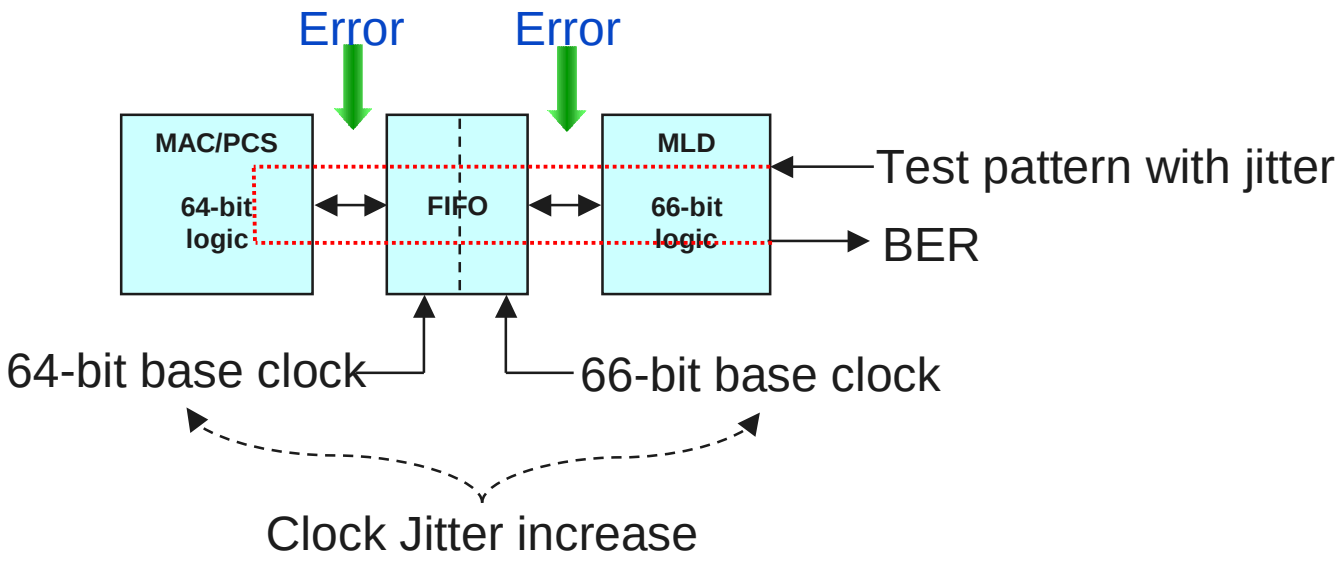
-1. Simultaneous switching of large-scale circuit in FPGA/ASIC causes internal power level drift.
-2. Power level drift changes internal buffer threshold level.
-3. Jitter on buffer output signal increases.
-4. The amount of jitter is different between asynchronous clocks (64-base, 66-base)



Increasing jitter inside of large scale logic circuit -2

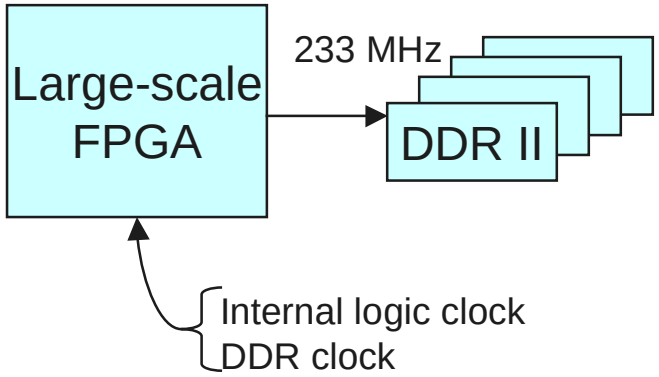
- The different amount of jitter decrease in phase margin at FIFO.
  Or it may cause error at FIFO in the worst case.

- To test jitter tolerance under the worst condition, skew alignment circuit should work.
  ➔ So test pattern should be included “Alignment marker” to drive alignment circuit.



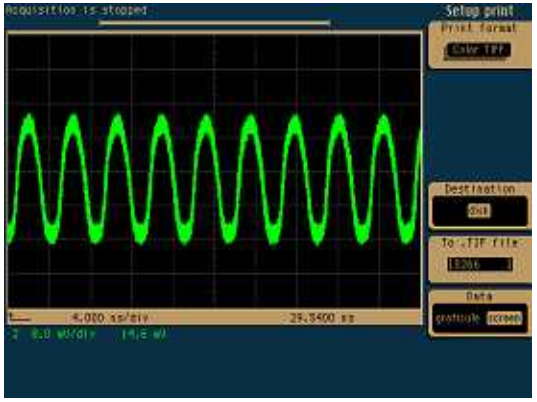
Increasing jitter inside of large scale logic circuit -3

-- Example --

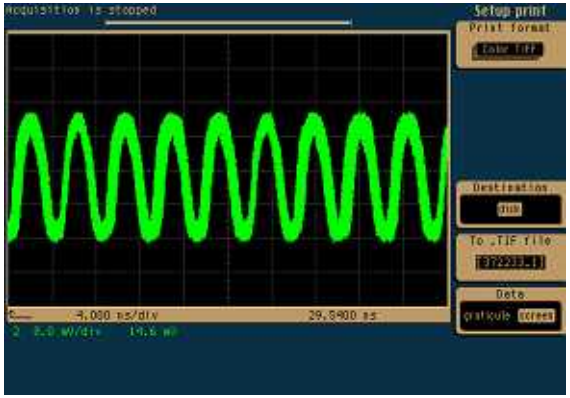


Simultaneous switching causes internal power level drift between two asynchronous clocks in FPGA causing error at DDR access

No error at DDR II



Error at DDR II



Jitter Tolerance Test Pattern Proposal

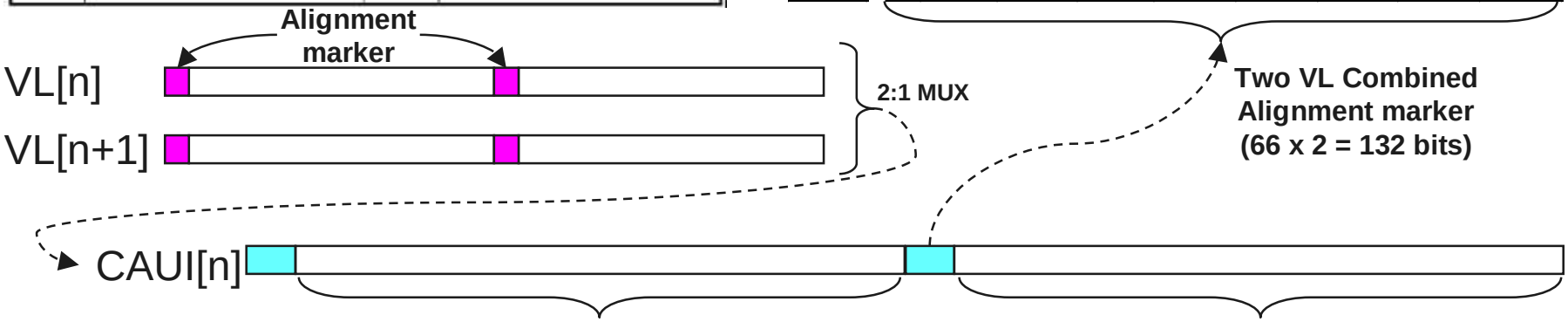
For equipment side, jitter tolerance test pattern should be included “Alignment Marker” to make the worst condition.

Table 82–2—Alignment marker encodings

Lane Number	Encoding[a] {M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7}	Lane Number	Encoding {M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7}
0	0xc1, 0x68, 0x21, 0xf4, 0x3e, 0x97, 0xde, 0x0b	10	0xfd, 0x6c, 0x99, 0xde, 0x02, 0x93, 0x66, 0x2d
1	0x9d, 0x71, 0x8e, 0x17, 0x62, 0x8e, 0x71, 0xe8	11	0xb9, 0x91, 0x55, 0xb8, 0x46, 0x6e, 0xaa, 0x47
2	0x59, 0x4b, 0xa8, 0xb0, 0xa6, 0xb4, 0x17, 0x4f	12	0x5c, 0x b9, 0xb2, 0xcd, 0xa3, 0x46, 0x4d, 0x32
3	0x4d, 0x95, 0x7b, 0x10, 0xb2, 0x6a, 0x84, 0xef	13	0x1a, 0xf8, 0xbd, 0xab, 0xe5, 0x07, 0x42, 0x54
4	0xf5, 0x 07, 0x09, 0x0b, 0x0a, 0xf8, 0xf6, 0xf4	14	0x83, 0xe7, 0xea, 0xb5, 0x7c, 0x38, 0x35, 0x4a
5	0xdd, 0x14, 0xe2, 0x50, 0x22, 0xeb, 0x3d, 0xaf	15	0x35, 0x36, 0xed, 0xeb, 0xca, 0xe9, 0x32, 0x14
6	0x9a, 0x4a, 0x28, 0x15, 0x65, 0xb5, 0xd9, 0xea	16	0xe4, 0x31, 0x4c, 0x30, 0x3b, 0xee, 0xb3, 0xef
7	0x7b, 0x45, 0x86, 0xfa, 0x84, 0xba, 0x99, 0x05	17	0xad, 0xd8, 0xb7, 0x35, 0x52, 0x29, 0x48, 0xca
8	0xa0, 0x24, 0x76, 0xdf, 0x5f, 0xdb, 0x89, 0x20	18	0x5f, 0x66, 0x2a, 0x6f, 0xa0, 0x99, 0xd5, 0x90
9	0x68, 0xe9, 0xfb, 0x38, 0x97, 0x36, 0x04, 0xc7	19	0xe0, 0xf0, 0xe5, 0xe9, 0x3f, 0x0f, 0x1a, 0x16

Alignment Marker for CAUI

CAUI									
0	3	E153	3D81	4856	AB35	1EAC	C27E	B7A9	54CA
1	3	32D3	619B	BDC5	8B00	CD2C	9E64	423A	74FF
2	3	FB73	013A	5086	118A	048C	FEC5	AF79	EE75
3	3	97CD	3099	1C3C	5766	6832	CF66	E3C3	A899
4	3	9C40	5861	7F6D	A7EA	63BF	A79E	8092	5815
5	3	EFE3	69A1	9393	E7E8	101C	965E	6C6C	1817
6	3	23E4	DFC2	CF59	E4E7	DC1B	203D	30A6	1B18
7	3	851B	A53E	F0D9	DE67	7AE4	5AC1	0F26	2198
8	3	E471	5B16	65B5	0F11	1B8E	A4E9	9A4A	F0EE
9	3	72AA	7D28	5C99	7CEB	8D55	82D7	A366	8314



Repeat same “Quasi PRBS” pattern. (16,383 x 2 x 66 → 2,162,556 bits)