Scrambled idle error checker

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Scrambled idle error checker definition

The scrambled idle error checker is defined in 82.2.17:

When align_status is true and the scrambled idle receive test-pattern mode is active, the scrambled idle test-pattern checker observes the output from the descrambler. When the output of the descrambler is the all idle pattern, a match is detected. When operating in scrambled idle test pattern, the test-pattern error counter counts blocks with a mismatch. Any mismatch indicates an error and shall increment the test-pattern error counter.

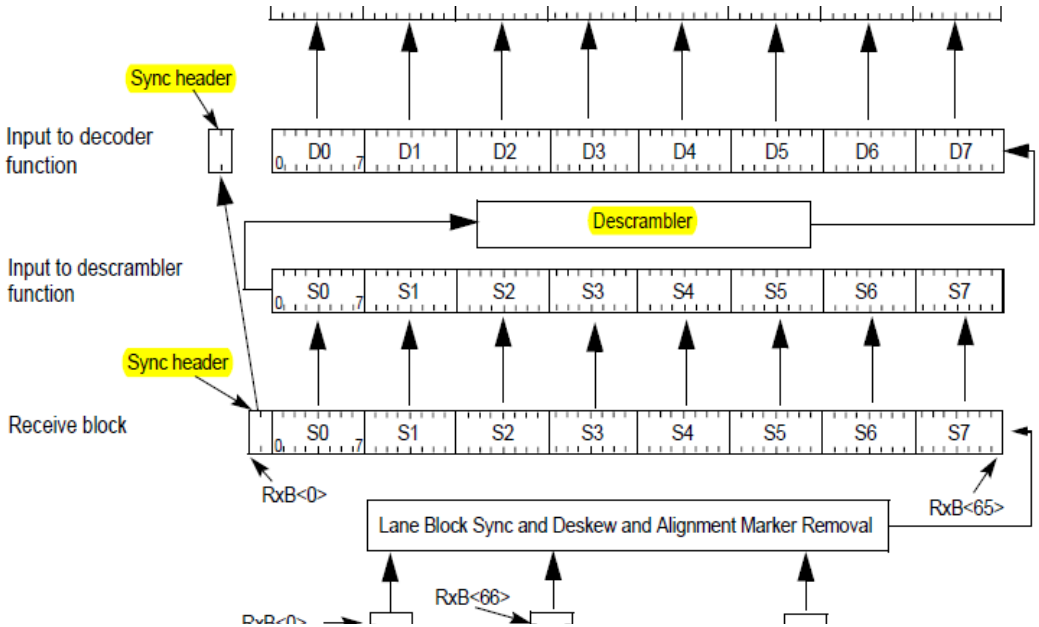
Which says that the scrambled idle test-pattern checker observes the output from the descrambler.

Sync bits

But according to Figure 82-4, the sync bits bypass the descrambler.

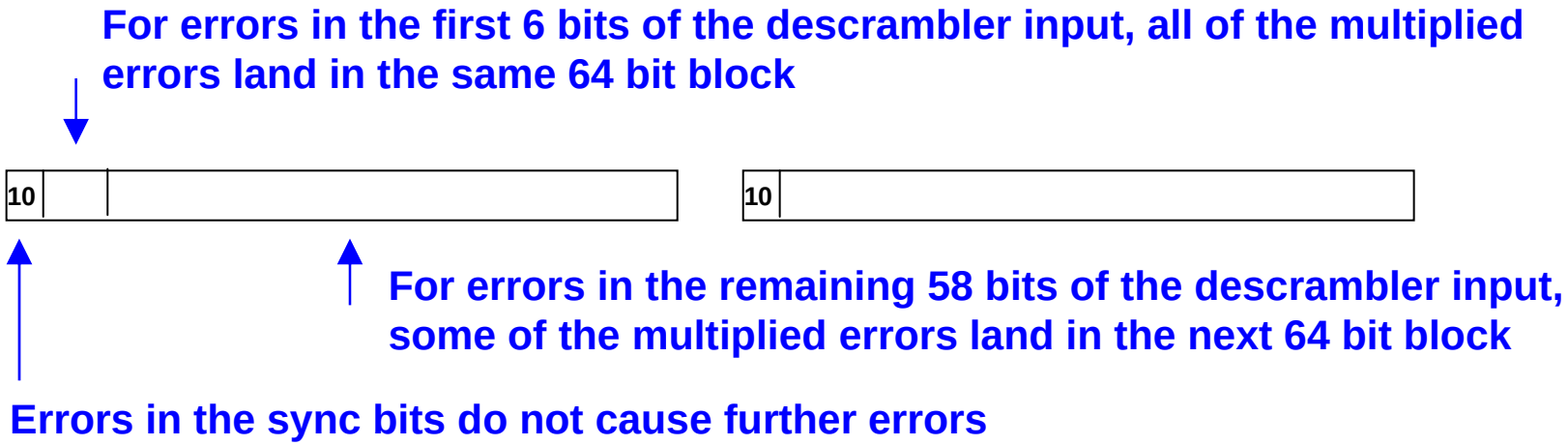
So, are the sync bits checked for errors or not?

To make this checker and the BIP checker cover the same bits we should explicitly include the sync bits.



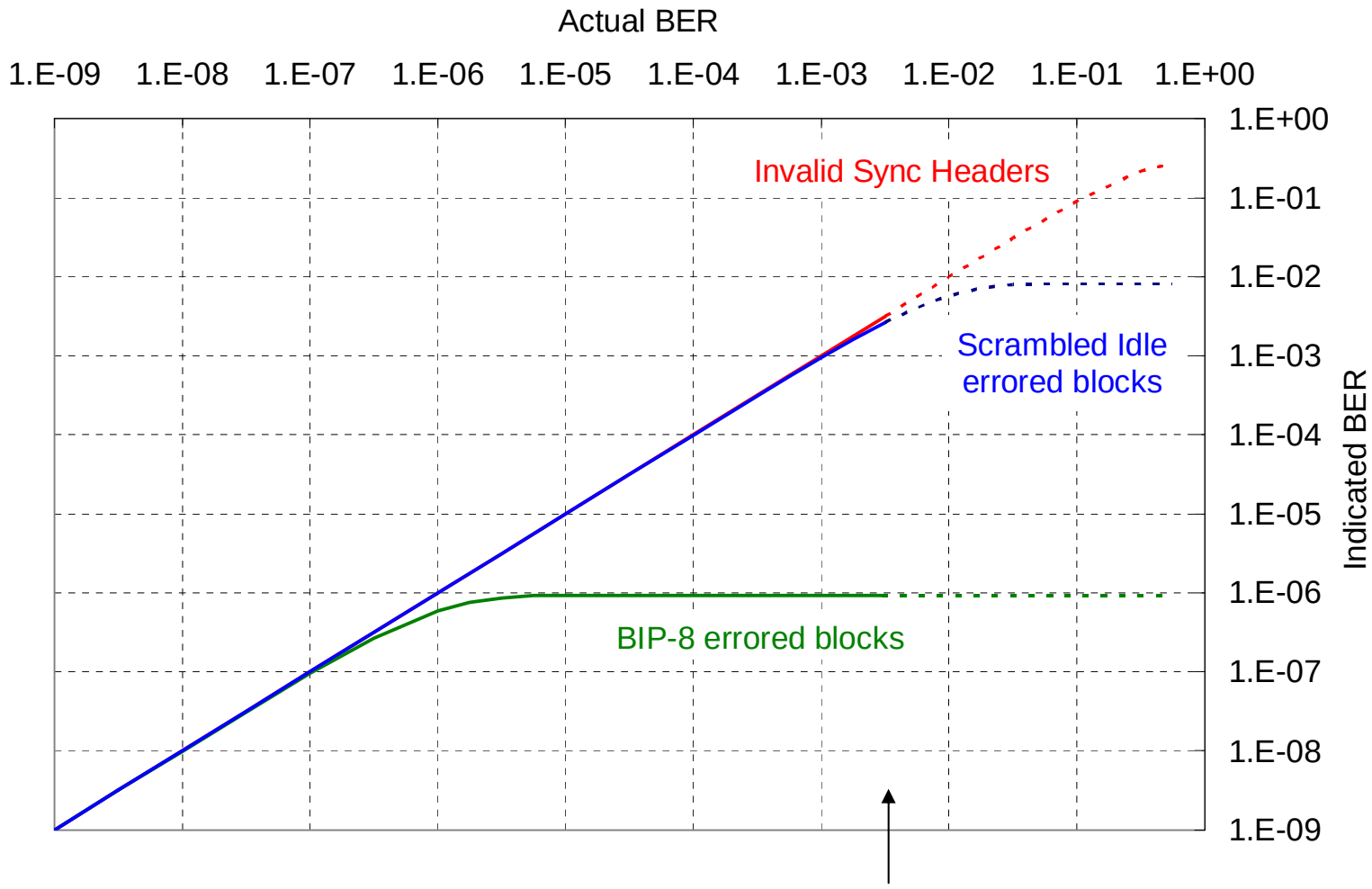
Descrambler error multiplication

The descrambler defined in 82.2.15 generates three errors at its output for every isolated error at its input. These are 39 and 58 bits after the input error.



Consequently, the bit error ratio is the block error ratio divided by a factor of 66*(1+ 58/66). i.e. the BER = block error ratio / 124

Error checker performance



Proposal in comment #461

Change the text in 82.2.17 as below:

When align_status is true and the scrambled idle receive test-pattern mode is active, the scrambled idle test-pattern checker observes the sync header and the output from the descrambler. When the sync header and the output of the descrambler is the all idle pattern, a match is detected. When operating in scrambled idle test pattern, the test-pattern error counter counts blocks with a mismatch. Any mismatch indicates an error and shall increment the test-pattern error counter. Because of the error multiplication characteristics of the descrambler, the incoming bit error ratio can be estimated by dividing the 66-bit block error ratio by a factor of 124.

Change the text in 82.2.14 as below:

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated BIP value for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.90 through 3.99) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1 081 344.

Thanks!