0. Changes to 86 and 86A for multi-lane BER counting and specification

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0.1 Rationale

Any PMD should provide the same BER performance at the MAC-PLS service interface irrespective of the number of lanes. It doesn't matter how the errors are divided among the lanes. This applies whether parallel optics, WDM or electrical (nPPI).

Test time is an important element of cost. D3.0 over-specifies BER to individual lanes when all that matters is the interface-wide BER. Measuring lanes in turn takes 4 or 10 times as long as for a serial interface. Even measuring all lanes at the same time takes 2 or 3 times as long because 4 or 10 times as many errors have to be counted.

D3.0 causes over-performance (excess cost) on top of any deliberate margin, because it is not likely that all lanes will be as bad as each other.

Different test patterns are checked on an interface wide basis (e.g. Pattern 5, scrambled idles) and checked by lane (e.g. Pattern 3, PRBS31). Each way can be used, but the meaning of BER in the two situations has not been spelled out.

Comments 300, 342, 305 and 568 address these issues, coming at the problem from two directions 300, 342, 305 address over-specification, 568 addresses clarity in the spec). This document is a synthesis of the ideas in these comments showing how they can be implemented for Clause 86.

0.2 Method

Define OMA and TDP per lane. Define stressed receiver sensitivity and receiver jitter tolerance interface wide.

0.3 Result

Transmitter remains over-specified as compared with a serial PMD with the same margin.

Channel remains over-specified as compared with a serial PMD with the same margin.

Receiver becomes specified fairly as compared with a serial PMD with the same margin.

Cost of optical receiver (PMD) and host receiver (PMA) can be better optimised as volumes grow.

Overall spec remains extremely conservative (more than for a serial PMD), as it is still unlikely that the same lane will be worst for transmitter, channel and receiver, and even less likely that all channels will be spec-worst.

0.4 Implementation of changes

Next pages show proposed changes to Clause 86.

Insert 86.8.2.1 as below

86.8.2.1 Multi-lane testing considerations

TDP is defined for each lane, at a BER of 10^{-12} on that lane. Stressed receiver sensitivity, receiver jitter tolerance and host input signal tolerance (in Annex 86A) are defined for an interface BER of 10^{-12}. The interface BER is the average of the four or ten BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three or nine unstressed lanes, and the BER for that stressed lane alone must be found, e.g. by multiplying by 4 or 10 if the unstressed lanes have low BER. To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means. In stressed receiver sensitivity and receiver jitter tolerance measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Either each receive lane is stressed in turn while all are operated, or all can be stressed together. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagaing and counter-propagating lanes operational so that crosstalk effects are included. While the lanes in a particular direction share a common clock, the Tx and Rx directions are not synchronous to each other.

Change 86.8.4.4 as follows

86.8.4.4 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) is as defined for 10GBASE-S in 52.9.10 with the following exceptions:

a) Each optical lane is tested individually with all other lanes in operation;
b) The test pattern is as defined in Table 86–12;
c) The transmitter is tested using an optical channel with an optical return loss of 12 dB;
d) The reference receiver (including the effect of the decision circuit) has a fourth order Bessel-Thomson filter response with a bandwidth of 6.2 GHz. The transversal filter of 52.9.10.3 is not used;
e) The reference sensitivity S and the measurement P_DUT are both measured with the sampling instant displaced from the eye center by ± 0.15 UI. For each of the two cases (early and late), if P_DUT(i) is larger than S(i), the TDP(i) for the transmitter under test is the difference between P_DUT(i) and S(i), TDP(i) = P_DUT(i) – S(i). Otherwise TDP(i) is zero, TDP(i) = 0. The TDP is the larger of the two TDP(i).
f) The BER of 10^{-12} is for the lane under test on its own. See 86.8.2.1 for multi-lane pattern considerations.

NOTE—Because practical receivers and decision circuits have noise and timing impairments, the sampling instant offsets have to be calibrated. One method of doing this is via a jitter bathtub method using a known low-jitter signal.

Change 86.8.4.7 and 86.8.4.8 as follows

86.8.4.7 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 86–8 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) 52.9.9 defines the reference test procedure for a single lane. See 86.8.2.1 and below for multi-lane considerations.
b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator;
c) The sinusoidal jitter is at a fixed 80 MHz frequency;
d) The Gaussian noise generator, the amplitude of the sinusoidal jitter and the Bessel-Thomson filter are adjusted so that the VECP, J2 and J9 specifications given in Table 86–8 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).
e) The pattern for the received compliance signal is specified in Table 86–12.
f) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the same receive OMA.
g) Where nPPI or XLAUI/CAUI is exposed, a PMD receiver is considered compliant if it meets the module electrical output specifications at TP4 given in Table 86A–3 for nPPI, or the requirements in Table 83B–3 for XLAUI/CAUI.
h) The mode-conditioning patch cord suitable for 62.5/125 μm fiber is not used.

~~For each lane, the stressed~~ Stressed receiver sensitivity is defined with ~~the~~ all transmit ~~section~~ and receive lanes in ~~operation on all~~ operation. All receive lanes ~~and with~~ may be stressed at the same time, or each receive ~~lanes not under test~~ lane may be stressed in ~~operation~~turn. Pattern 3 or Pattern 5, or a valid 40GBASE–R4 or 100GBASE–R10 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 40GBASE-SR4 and 100GBASE-SR10, the relevant BER is the interface BER. The interface BER is the average of the four or ten BERs of the receive lanes when stressed: see 86.8.2.1.

86.8.4.8 Receiver jitter tolerance

Receiver jitter tolerance ~~for each lane~~ is defined as in 68.6.11, with the following differences:

a) 68.6.11 defines the reference test procedure for a single lane: see 86.8.2.1 for multi-lane considerations;
a) The pattern to be received is specified in Table 86–12;
b) The parameters of the signal are specified in Table 86–8;
c) All receive lanes may be stressed at the same time, or each receive lane may be stressed in turn;
d) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 40GBASE-R4 or 100GBASE-R10 signal;
e) The transmitter is transmitting one of these signals using all lanes;
f) The transmitter and the receiver are not synchronous~~.~~;
g) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed.

Change two rows of PICS as below

86.11.4.4 Definitions of parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
SOM8	Stressed receiver conformance	86.8.4.7	~~Each lane, per~~ Per 52.9.9 as modified	M	Yes [ ]
SOM9	Receiver jitter tolerance	86.8.4.8	~~Each lane, per~~ Per 68.6.11 as modified	M	Yes [ ]

Annex 86A

86A.1 Changes for multi-lane testing shown

86A.4.2 nPPI module to host electrical specifications

Change Table 86A-4 as below

Table 86A–4—nPPI host electrical input specifications at TP4 and TP4a

Parameter description	Test point	Min	Max	Units	Conditions
Receiver signal ~~tolerance, each lane~~ tolerance (interface BER)		–	10^{-12}	–	

86A.5 Definitions of electrical parameters and measurement methods

Test points are defined in 86A.5.1, compliance boards in 86A.5.1.1, test patterns in 86A.5.2 and parameters in 86A.5.3 and 86.8. Multi-lane testing considerations are given in 86.8.2.1.

86A.5.2 Test patterns and related subclauses

Compliance is to be achieved in normal operation. Table 86–11 lists the defined test patterns, and Table 86D–2 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Multi-lane testing considerations are given in 86.8.2.1. As Pattern 3 is more demanding than Pattern 5 (which itself is the same or more demanding than other 40GBASE-R or 100GBASE-R bit streams) an item which is compliant using Pattern 5 is considered compliant even if it does not meet the required limit using Pattern 3.

86A.5.3 Parameter definitions

86A.5.3.8 Host electrical receiver signal tolerance

To be compliant the host electrical receiver signal tolerance shall satisfy the requirements of 86A.5.3.8.1 to 86A.5.3.8.6.

86A.5.3.8.1 Introduction

This clause provides guidance for jitter tolerance testing at the Rx host (PMA) compliance point TP4/TP4a. Compliance is required with input jitter, vertical eye closure (Y1), and vertical peak level (Y2) as specified in Table 86A–4. Compliance is defined at an ~~error ratio~~ interface BER (the average of the BERs of all the

lanes when stressed) of 10^{-12}. There are two test conditions: once each for the sensitivity and overload vertical eye parameters conditions. The reference test procedure is described in detail for a single stressed lane. Either each Rx lane is stressed in turn or they are all stressed at the same time.

86A.5.3.8.6 Test procedure

Testing is performed differentially through a Host Compliance Board (see 86A.5.1).

Using a test signal arranged according to 86A.5.3.8.2 and calibrated according to 86A.5.3.8.5, operate the system with the test pattern specified in Table 86A-6. Either each lane is stressed in turn while all are operated, or all can be stressed together. The BERs of all the lanes when stressed are averaged to form the interface BER. See 86.8.2.1.

All signals and reference clocks that operate during normal operation are active during the test including all the other host lanes in both directions. The test signal and the host's transmitted signals are asynchronous. The host transmits Pattern 3 (PRBS31), Pattern 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal. The sinusoidal jitter is stepped across the frequency and amplitude range according to Table 86A-7and illustrated in Figure 86A–10, while monitoring the ~~BER~~BER of the lane(s). The interface BER of a compliant host receiver remains below 10^{-12}.