Choosing 25G CRU BW and CDR BW Wisely

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Background Statement

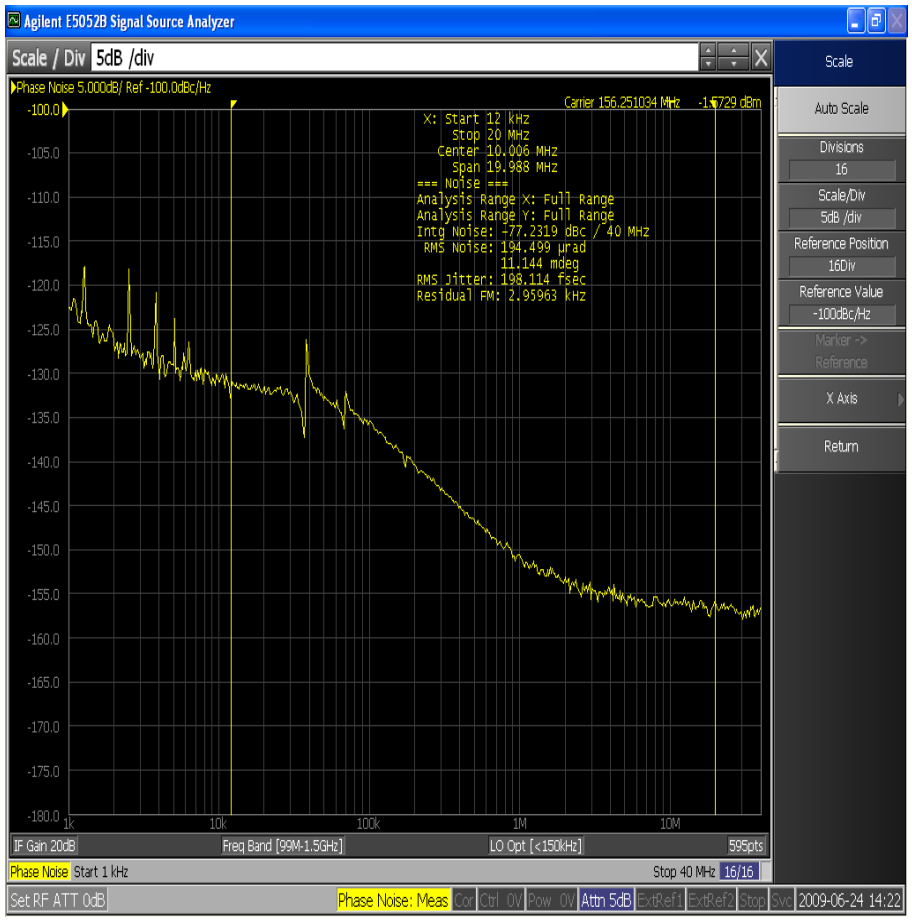
- 88.8.5.3 Reference Receiver defines CRU BW of 10 MHz for TDP measurement
- 88.8.8 Transmitter optical waveform defines CRU BW of 10 MHz
- 88.8.10 Stress receiver sensitivity defines effective corner frequency of 10 MHz
- With changes made in Chicago we now have consistent transmitter CRU BW and jitter tolerance definition but scaling 10GbE CRU BW by factor of 25.7/10.3 results in extra burden on the receiver with no clear benefit for the transmitter
- Comment 790 and 787 propose to reduce the CRU BW from 10 MHz to 7 MHz and comment 788 proposes to use the same corner frequency for jitter tolerance

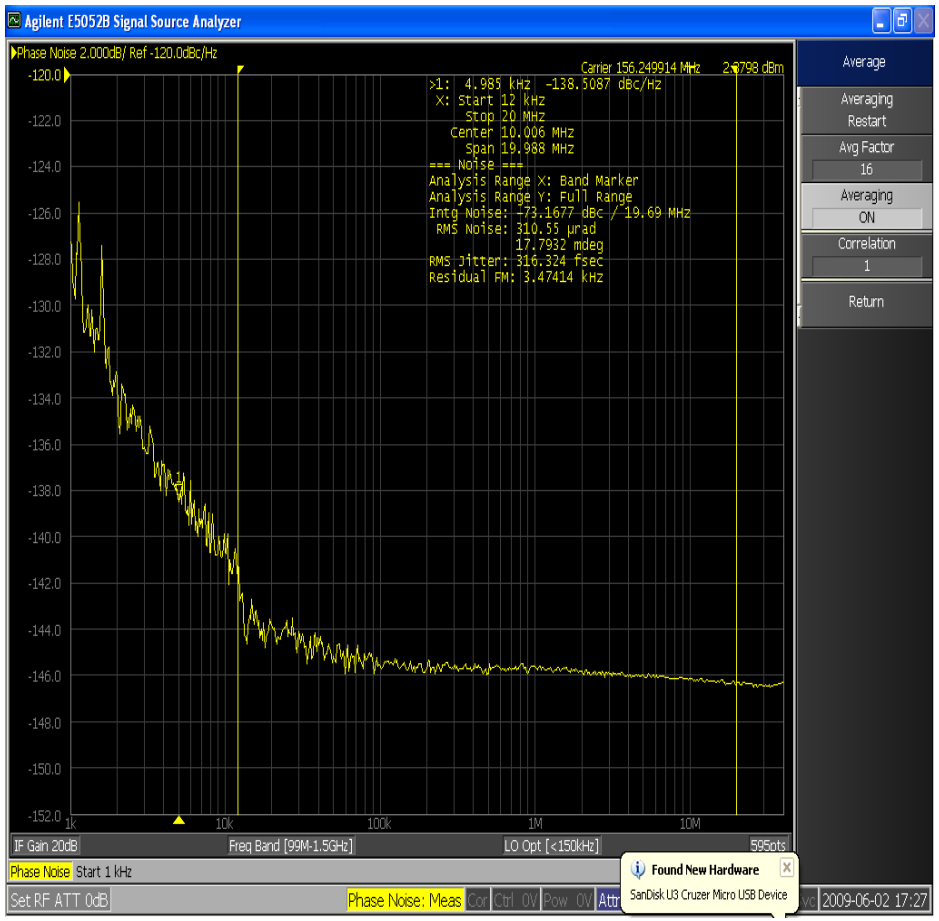
Considerations for CRU and CDR BW

- Consideration for the golden PLL CRU BW
  - Oscillator phase
    - Typically no benefit as the phase noise is flat >1 MHz
  - Crosstalk
    - High frequency effect >> CRU BW
  - VCO Phase noise
    - No benefit for CRU BW > 5 MHz
- Consideration for CDR BW
  - Pattern dependent effects
    - Does not apply to 64B/66B with its spectrum in the 100KHz
  - Power
    - Higher BW loop BW would result in higher power
  - Receiver with DFE
    - DFE receiver timing recovery introduces latency making jitter tolerance more challenging, this is the reason LRM and KR jitter tolerance are more accommodating.

Typical Low Cost Oscillator Phase Noise Plot

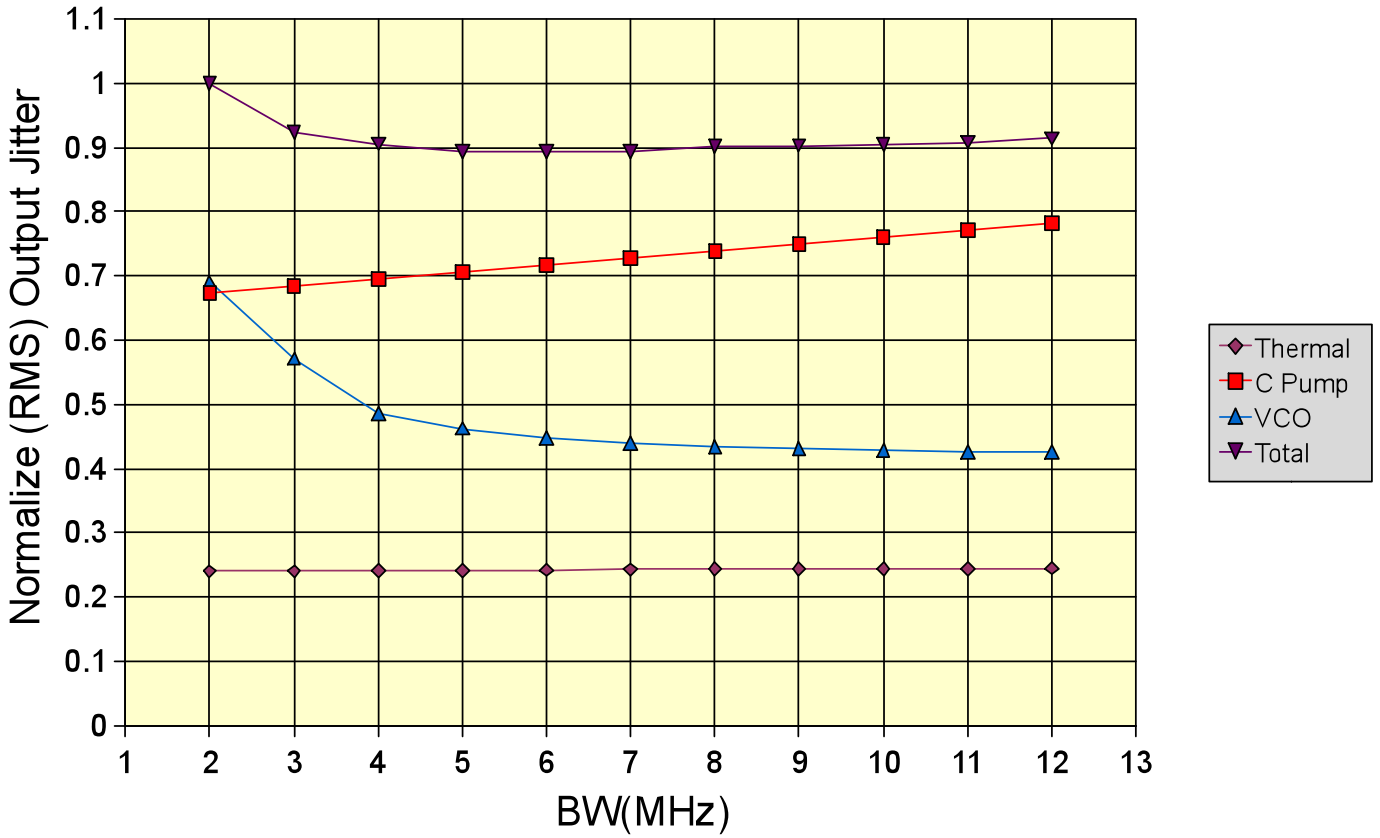
- Most oscillator phase noise is flat after 1 MHz
  - There is no benefit to higher CRU BW!





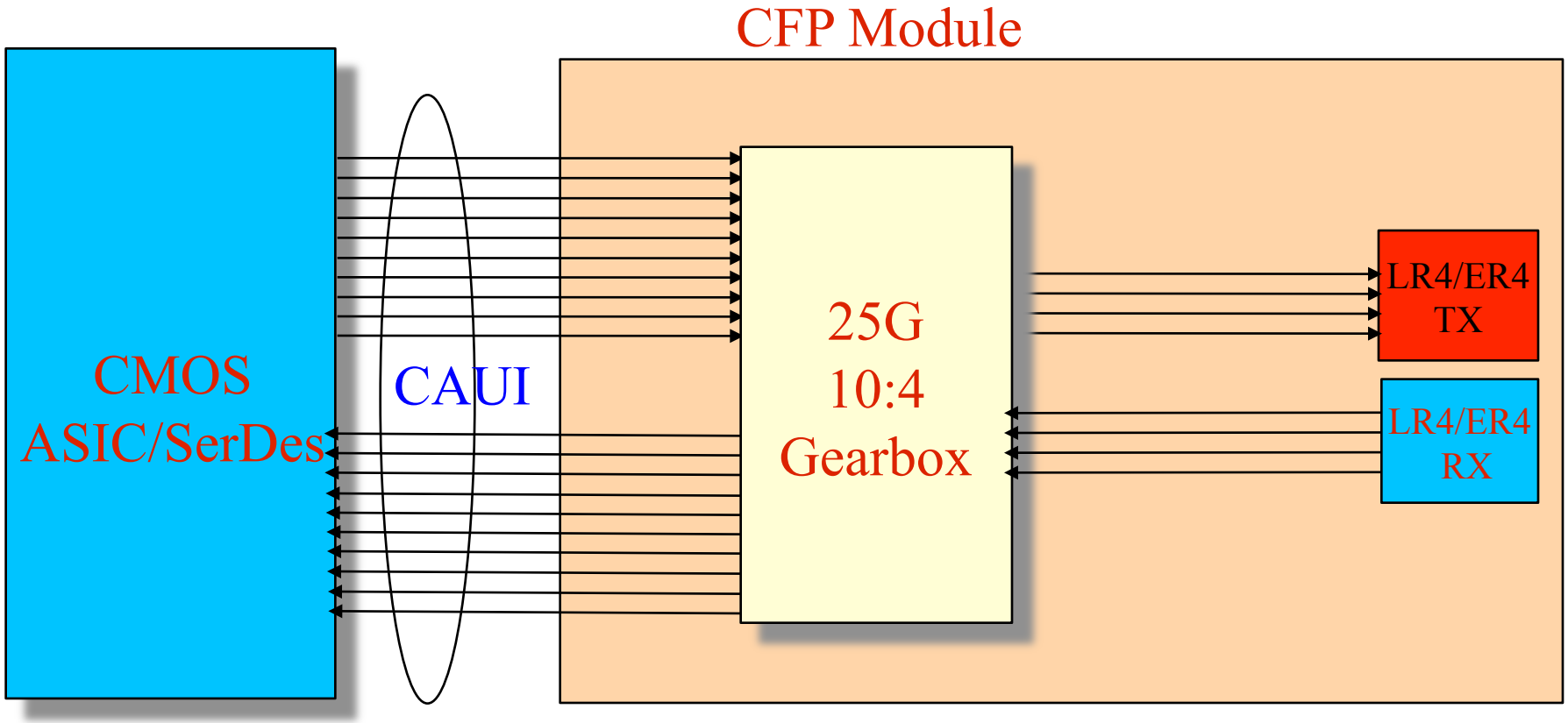
SerDes Transmitter Relative Jitter

- Thermal, charge pump, VCO, and total relative output jitter as function of BW
  - BW of 5-7 MHz gives best total output jitter and there is no benefit having CRU BW> 7 MHz



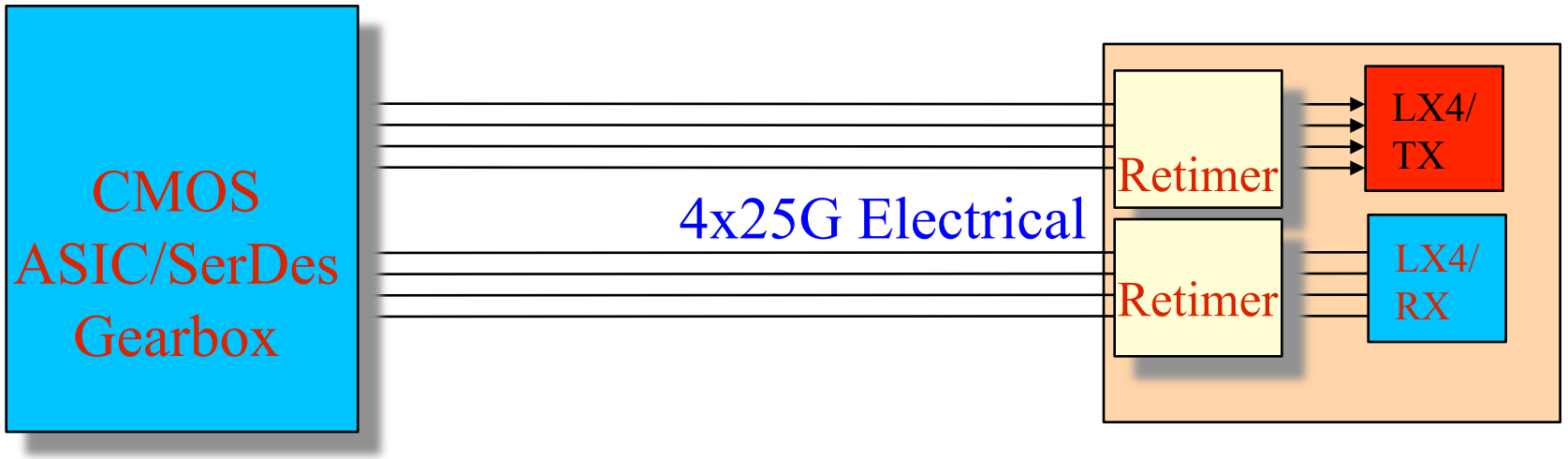
100GBase-LR4/ER4 Current Implementation

- Module interface based on CAUI
- The Gearbox chip FIFO absorbs higher frequency absorb SJ



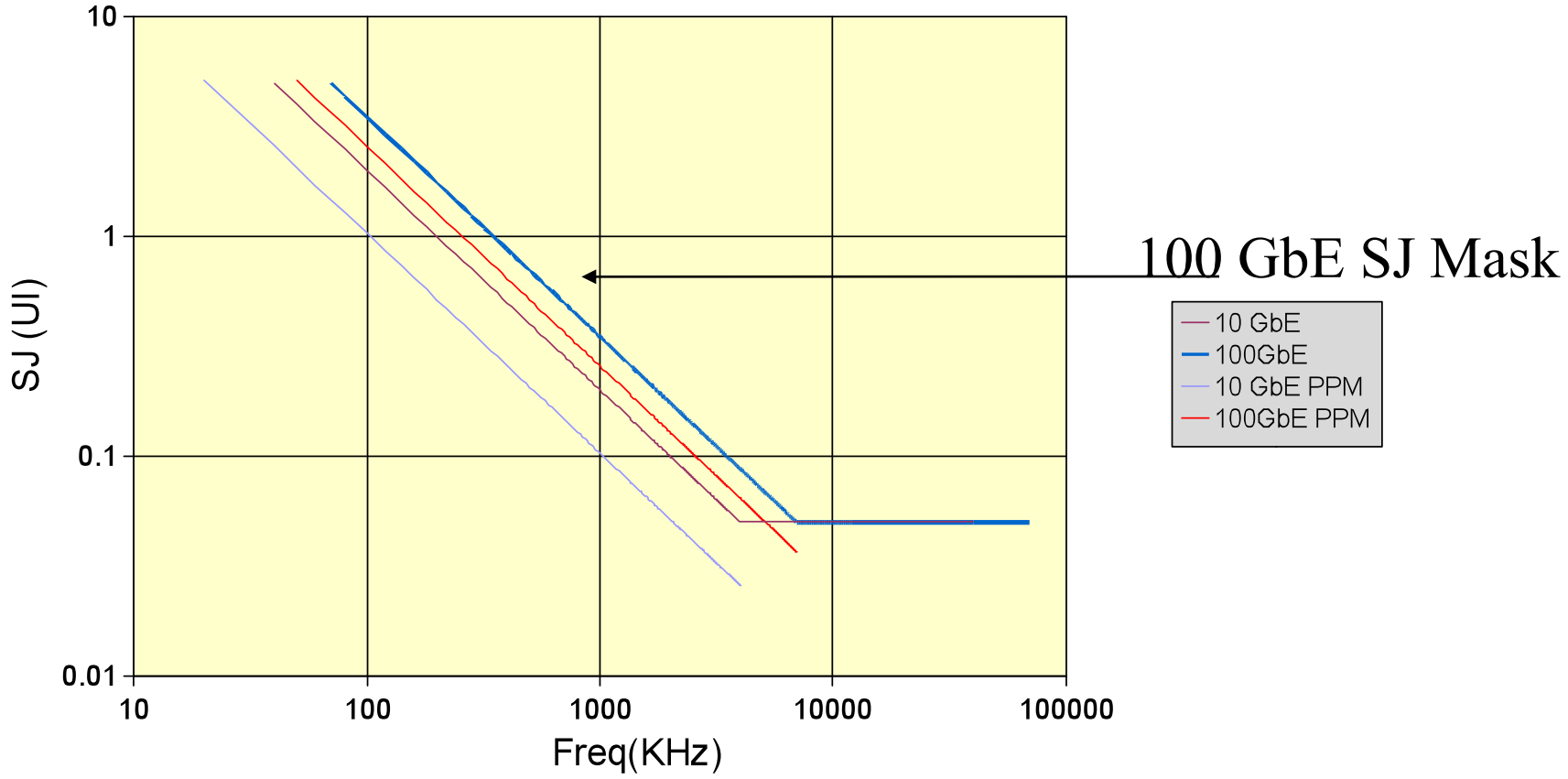
Next Generation 100GBASE-LR4/ER4

- Future ASIC/Serdes will integrate the 4x25G gearbox
- Simpler retimer without FIFO will pass SJ to the host
- The 4x25G host receiver must now absorb the SJ!
- Host ASIC/SerDes with DFE receiver operating at 25.7 Gbd must equalize the channel under more stressful jitter tolerance for no good reason!



10 GbE SJ Mask and Proposed 100 GbE Mask

- 100 GbE mask with proposed compromised 7 GHz BW



Overview of 10GbE Jitter Tolerance Specifications

- SR/LR/ER
  - 4 MHz transmit CRU
  - Comprehensive stress sensitivity with 4 MHz SJ corner frequency
- LRM
  - 4 MHz transmit CRU
  - Tested unstress 5UI @ 75 Khz and 1 UI @ 375 Khz
- KR
  - 4 MHz transmit CRU
  - Comprehensive stress sensitivity with SJ of 0.115UI >15 MHz

Summary

- Current 10 MHz CRU BW has no clear benefit for the transmitter but it burdens the receiver in term of power, implementation, and burdens future generation host ASIC/SerDes operating 25.7 Gbd
- The 7 MHz CRU and SJ corner frequency is a compromise between the current 10 MHz CRU BW and 4 MHz SJ corner frequency
  - 5-7 MHz BW results in the lowest output jitter
  - SJ corner frequency of <=7 MHz allow lower cost and power DFE receiver
- Proposed resolution assuming 7 MHz for CRU and SJ corner frequency
  - Change 88.8.5.3 and 88.8.8 CRU BW from 10 MHz to 7 MHz
  - Change 88.8.10 SJ corner frequency from 4 MHz to 7 MHz
    - f<70 KHz not specified
    - 70 KHz <= f <=7 MHz 3.5x10^5/f + s – 0.05
    - 7 MHz <= f <=10 LB 0.05 <=S <=0.15