Proposals to allow unretimed 40GBASE-LR4 module to operate with nPPI specs (comments 886, 793, 792)

Jonathan King, Finisar

New Orleans, January 2010

Supporters

- Chris Cole - Finisar
- Jon Anderson - Opnext
- Marco Mazzini - Cisco
- Alessandro Cavaciuti - Cisco
- Gary Nicholl – Cisco
- Mike Dudek – QLogic
- Ali Ghiasi – Broadcom
- Jeff Maki – Juniper Networks
- Ryan Latchman – Gennum
- Eddie Tsumura – Sumitomo Electric
- Tom Palkert – Xilinx
- Steve Swansen – Corning Cable Systems
- John D'Ambrosia – Force10
- Tim Warland – Applied Micro
- Frank Chang – Vitesse
- Dan Andrea – Lightwire

Introduction

- Enabling an unretimed 40G LR4 module to use the same host board slot as unretimed SR4 and CR4 would be a significant benefit to the industry
- The 40GBASE-LR4 optical specs and nPPI specs in 802.3ba Draft 3.0 do not close the jitter budget for an unretimed LR4 module
- Comments 793, 792, and 886, suggested a combination of changes to nPPI and LR4 optical specs to remedy this; they were developed further during consensus building teleconference calls. The resulting proposal is presented here

Notes on determining optical specs

To calculate optical parameter specs which would close the jitter budget, consistent with the various new nPPI jitter budget proposals, the 10 Gigabit Ethernet spreadsheet was used with these adjustments:

- J2 and J9 calculated at TP1 to TP4
  - 20-80% rise/fall times at each test point, host Qsq, RIN, and Rx noise terms, used to calculate amplitude noise-jitter conversion
- Deterministic jitter components of J2 are added linearly through link model
  - A reasonable approach for low numbers of independent jitter mechanisms and worst case budgeting, follows from a simple treatment of jitter statistics
    - treat jitter as dual-Dirac contributor at each TP; note that after more than one contributor the accumulated jitter is no longer dual Dirac in nature
- RJ jitter components added as RMS
  - Note:RJ at TP4 is dominated by Rx noise and RIN; RJ component at TP1 makes negligible contribution to J9 at TP4 for LR4
    - (increasing J9 at TP1 from 0.26 to 0.29 UI changes TP4 J2 by ~0.001 UI, TP4 J9 by ~ 0.002 UI).
- Noise-limited equivalent Rx sensitivity used to calculate Rx RJ contribution at TP4
  - Set to 1 dB below unstressed Rx sensitivity (i.e. Noise Limited Equivalent Rx sensitivity set to -12.5 dBm OMA) – this is not a specified parameter in 802.3ba
- Unstressed Rx sensitivity of -11.5 dBm OMA used for power budget calculation
- Decreased $Ts_{(20\text{-}80)}$ to 38 ps from 40 ps, in line with improved DMLs
  - this is not a specified parameter in 802.3ba, but affects the TDP calculation
- Keep $RIN_{20}OMA$ spec value of -128 dB/Hz, but use -130dB/Hz in spreadsheet
  - Tx RIN and jitter is controlled by the TDP spec: allows Tx trade off of jitter vs RIN at TP2

Summary of proposal

- Proposed changes to 802.3ba 40GBASE-LR4 optical specs:
  - Increase TDP by 0.3 dB to 2.6 dB
  - Increase SRS in line with VECP by 0.3 dB to -9.6 dBm OMA for retimed module
    - Unretimed Rx must meet nPPI TP4 jitter specs at SRS conditions, by a combination of lower deterministic and/or lower random jitter contribution
  - Rx sensitivity (unstressed) held at -11.5 dBm
- Proposed changes to 802.3ba nPPI specs:
  - Decrease nPPI TP1 J2 spec to 0.17 UI, TP1 J9 increased to 0.29 UI
  - Increase nPPI TP4 J9 spec to 0.65 UI, TP4 J2 decreased to 0.42 UI
  - Change SRS test description to be consistent with the proposals above

D3.0 values used as reference

Jitter Budget proposals for nPPI

	D 3.0	793	886	Proposal
Table 86A-1				
J2 Jitter output for 40G (max) UI	0.18	0.17	0.18	0.17
J2 Jitter output for 100G (max) UI	0.18	0.18	0.18	0.17
J9 Jitter output (max) UI	0.26	0.26	0.26	0.29
Table 86A-2				
J2 Jitter input for 40G (min) UI	0.18	0.17	0.18	0.17
J2 Jitter input for 100G (min) UI	0.18	0.18	0.18	0.17
J9 Jitter input (min) UI	0.26	0.26	0.26	0.29
Table 86A-3				
J2 Jitter output (max) UI	0.46	0.46	0.42	0.42
J9 Jitter output for 40G (max) UI	0.62	0.64	0.65	0.65
J9 Jitter output for 100G (max) UI	0.62	0.62	0.65	0.65
Table 86A-4				
J2 Jitter tolerance UI	0.46	0.46	0.42	0.42
J9 Jitter tolerance for 40G UI	0.62	0.64	0.65	0.65
J9 Jitter tolerance for 100G UI	0.62	0.62	0.65	0.65

- Jitter budget revisions intended to allow an unretimed 40GBASE-LR4 module to operate with nPPI
  - Comments 793 and 886 proposals from individual contributors via comment
  - The 'proposal' jitter budget is a consensus from several teleconference calls
    - optimises J2 and J9 specs for an nPPI compliant host and an unretimed LR4 module

Optical proposals for 40GBASE-LR4

	D 3.0	792	consistent with 793 (40G)	consistent with 886	Proposal
Table 87-7					
Total average launch power (max) dBm	8.3	8.6	8.3	8.3	8.3
Average launch power, each lane (max) dBm	2.3	2.6	2.3	2.3	2.3
Average launch power, each lane (min) dBm	-7	-6.7	-7	-7	-7
OMA each lane max dBm	3.5	3.8	3.5	3.5	3.5
OMA each lane min dBm	-4	-3.7	-4	-4	-4
OMA - TDP each lane min dBm	-4.8	-4.5	-4.8	-4.8	-4.8
TDP each lane max dB	2.3	2.6	2.6	2.7	2.6
$RIN_{20}OMA$ (max) dB/Hz	-128	-130	-128	-128	-128
Table 87-8					
Damage threshold (min) dBm	3.3	3.6	3.3	3.3	3.3
Average receive power, each lane (max) dBm	2.3	2.6	2.3	2.3	2.3
Average receive power, each lane (min) dBm	-13.7	-13.4	-13.7	-13.7	-13.7
Receive power, each lane (OMA) (max) dBm	3.5	3.8	3.5	3.5	3.5
Receiver sensitivity (OMA), each lane (max) dBm	-11.5	-11.5	-11.5	-11.5	-11.5
Stressed Rx sens OMA, each lane dBm	-9.9	-9.6	-9.6	-9.5	-9.6
Vertical eye closure penalty	1.6	1.9	1.9	2.0	1.9

- Note 1: The $RIN_{20}OMA$ spec doesn't need to change from the D3.0 value, because the normative TDP spec ensures that a higher RIN transmitter must have lower jitter in order to pass the normative TDP test. Allows RIN vs jitter trade off in Tx.

Optical proposals for 40GBASE-LR4 cont.

	D 3.0	792	consistent with jitter budget 793	consistent with jitter budget 886	Proposal
Table 87-9					
Power budget (for max TDP) dB	9	9.3	9.3	9.4	9.3
Allocation for penalties (for max TDP) dB	2.3	2.6	2.6	2.7	2.6

- Note: power budget for max TDP = TDP + Link and connector loss

Back up

Modifications to 10GE spreadsheet for unretimed 40GBASE-LR4 jitter budget calculations

10GEPBud3_1_16a spreadsheet model, sheet 1310S, was amended as below:

- Added cells to calculate J2 and J9 for TP1, TP2, TP3 and TP4 vs link length
- Added cell for Noise Limited Equivalent Rx sensitivity, for jitter budget calculations only (affects TP4 values only)
- Added cell for host clock phase noise contribution (RJ)
- Host Tx, Module Tx, and Rx output 20-80% rise/fall times used to calculate amplitude noise-jitter conversion
  - (Host Qsq, RIN and Rx noise terms)
- Conceptual model of J2 : deterministic, bounded jitter ("J.3"), plus 2.N x RJ (where +/-N.σ encompasses 99% of jitter)
  - J.3 adds linearly from each stage; host Tx, module Tx, module Rx
  - few contributors: a simple treatment of jitter statistics is possible
    - treats jitter like dual Dirac model for each contributor to deterministic jitter for the purposes of the spreadsheet
      - *after more than one contributor the jitter is no longer dual Dirac in nature.*
    - 2-valued at host Tx output, 4-valued at module Tx out, 8-valued at module Rx out
- "Det.Jitter" and "DCD_DJ" in 10G spreadsheet are modified to use linearly combined J.3 contributions from host, module Tx, and module Rx
  - 50% of J.3 assumed to be DCD

J2 accumulation - 1

Conceptually, J2 composed of deterministic and random jitter components.

Add deterministic jitter linearly, add random jitter as rms

- Simple case: bi-valued, bounded deterministic jitter contributions from each of host Tx, module Tx and module Rx.
  - Tx host deterministic jitter ("J.3") = 0.094 UI, RJ=0.0163 UI
    - host Qsq = 45, Clock jitter=0.0154, host rise/fall time 20-80%=28ps
    - Tx host J2 = 0.17, J9 = 0.29
  - Module Tx adds J.3 = 0.06 UI
  - Module Rx adds J.3 = 0.06 UI

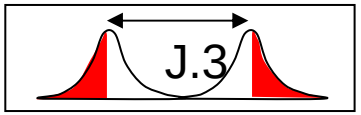


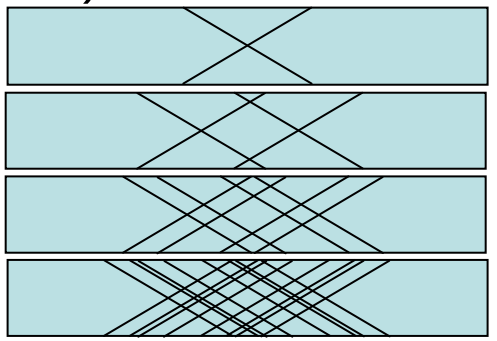
Illustration of crossing points of eyes (without RJ):

Clean data – 1 crossing point

Tx host output – 2 crossing points

Module Tx output – 4 crossing points

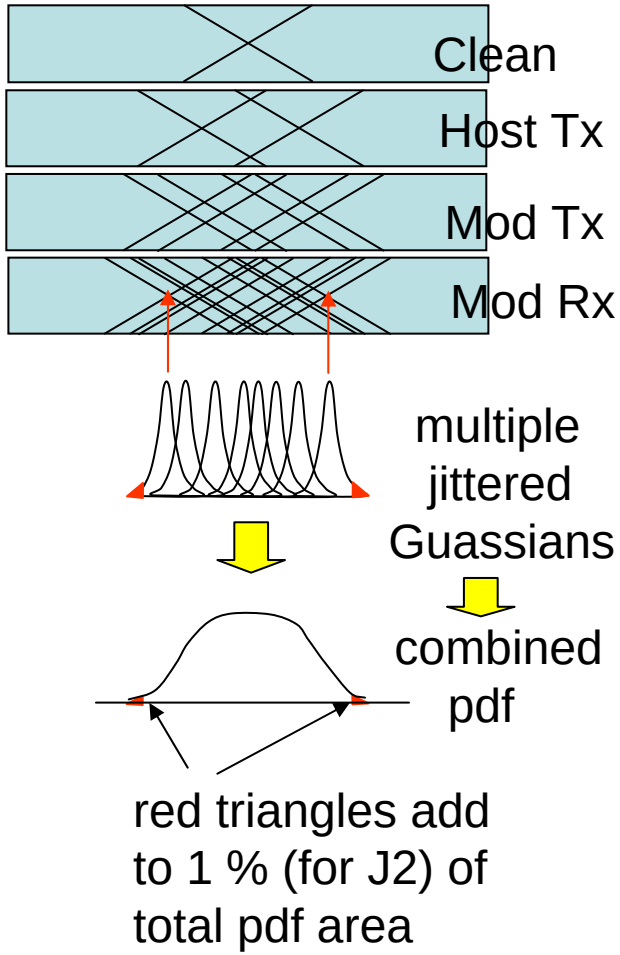
Module Rx output – 8 crossing points



J2 accumulation - 2

- Outer crossing points separated by linear sum of J.3 contribution
- Each crossing point occurs 1/8th of the time.
- Since J2 is defined by the points at which 1% of the pdf lies outside J2, and only the outer crossing points are significant contributors to J2 *, the module Rx output J2 needs to include fewer σ from outer crossing points than the host Tx output does. Similar argument applies for J9.
- ~30% difference in RJ contribution for J2
- ~5% difference in RJ contribution for J9

*true for J.3 contributions is >~RJ/2



P	N	
5e-3	2.59	zero DJ
1e-2	2.34	2-valued DJ
2e-2	2.06	4-valued DJ
4e-2	1.75	8-valued DJ
5e-10	6.11	zero DJ
1e-9	6.01	2-valued DJ
2e-9	5.89	4-valued DJ
4e-9	5.77	8-valued DJ
5e-13	7.13	zero DJ
1e-12	7.04	2-valued DJ
2e-12	6.94	4-valued DJ
4e-12	6.84	8-valued DJ