# 802.3ba copper cable assembly baseline proposal

Chris Di Minico MC Communications cdiminico@ieee.org

### **Contributors**

- Galen Fromm, Jay Neer Molex
- Jens Aumann, Leoni Special Cables
- Vivek Telang, Broadcom
- Howard Baumer, Mobius Semiconductor
- Amir Mezer, Intel

### **Supporters**

- Dan Dove, ProCurve Networking by HP
- Shimon Muller, Sun Microsystems
- Tom Palkert, Luxtera
- Gourgen Oganessyan, Quellan
- Ed Cady, Meritec
- Herb Van Deusen, Gore
- Hugh Barrass, Cisco
- ·ilango Ganga, Intel
- Rich Mellitz, Intel
- Greg McSorley, Amphenol
- Bob Thornton, Fujitsu
- Bill MacKillop, Cinch Connectors
- Jim McGrath, Cinch Connectors

### **Summary**

- •Considerations for 802.3ba Cu cable assembly specifications for 802.3ba baseline proposal.
- •Measurement models and simulation models developed to validate usage of 10GBASE-KR (Clause 72) for 10 Gb/s lane options for both 40GBASE-CR4 and 100GBASE-CR10 cable assemblies.
- •CX4 twinaxial cable assembly differential parameters proposed as basis for 40GBASE-CR4 and 100GBASE-CR10 link specification (i.e., S-parameters).
- •Considerations for configuring QSFP low speed electrical hardware pins for 40GBASE-CR4 operation.
- •Two independent demonstrations of 10GBASE-KR operation over 10 meters of passive copper cable assemblies.

### 802.3ba objectives

- Support full-duplex operation only
- Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
- Preserve minimum and maximum FrameSize of current 802.3 standard
- Support a BER better than or equal to 10<sup>-12</sup> at the MAC/PLS service interface
- Provide appropriate support for OTN
- Support a MAC data rate of 40 Gb/s
- Provide Physical Layer specifications which support 40 Gb/s operation over:
  - at least 10km on SMF
  - at least 100m on OM3 MMF
  - at least 10m over a copper cable assembly
  - at least 1m over a backplane
- Support a MAC data rate of 100 Gb/s
- Provide Physical Layer specifications which support 100 Gb/s operation over:
  - at least 40km on SMF
  - at least 10km on SMF
  - at least 100m on OM3 MMF
  - at least 10m over a copper cable assembly

### Copper cable assembly: lane options considered

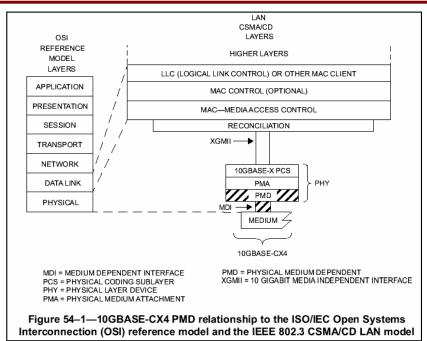
- Support a MAC data rate of 40 Gb/s
- Provide Physical Layer specifications which support 40 Gb/s operation over:
  - at least 10m over a copper cable assembly
  - 4 x 10 Gb/s lane
- Support a MAC data rate of 100 Gb/s
- Provide Physical Layer specifications which support 100 Gb/s operation over:
  - at least 10m over a copper cable assembly
  - -10 x 10 Gb/s lane

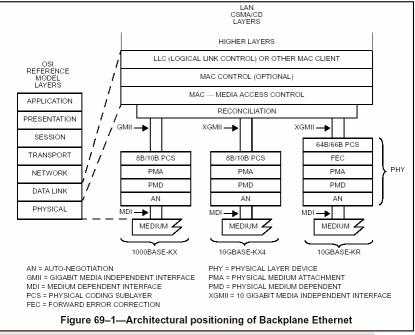
### 802.3ba Cu cable assembly proposal

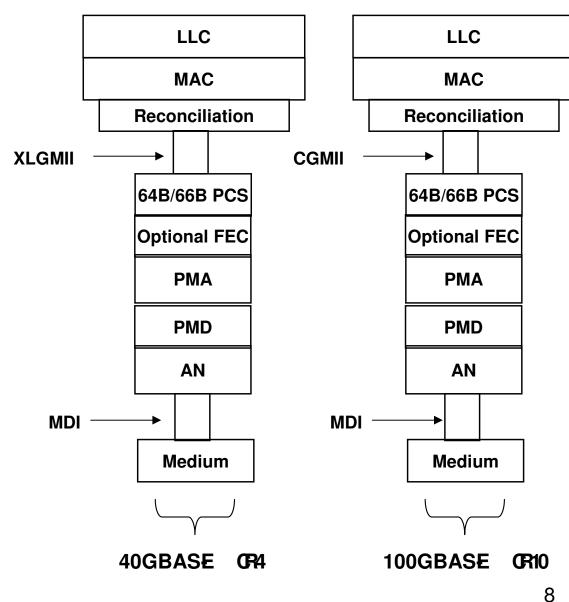
- Utilize 10GBASE-KR (Clause 72) and 10GBASE-CX4 to specify 40GBASE-CR4 and 100GBASE-CR10.
  - 64B/66B PCS
  - Signaling speed 10.3125 Gbd (per lane)
  - 4x and 10x KR transmit and receive functions
  - Commonality with 40 GbE backplane proposal
  - S-parameters cable assembly differential parameter
  - x4 MDI considered: QSFP and IEC 61076-3-113 mechanical mating interface (10GBASE-CX4 mechanical)
    - QSFP- module and connector dimensions common for both fiber and copper
      - For 40GBASE-CR4, QSFP low speed control and sense signals set to non-operational QSFP state.
    - CX4 connector mechanicals for copper (allows for backward compatibility)
  - SFF-8092 MDI considered for 100GBASE-CR10: (proposals evaluated in IBTA)
- Optional FEC sublayer PCS to interface to optional FEC sublayer consider Clause 74 specification commonality with 40 GbE backplane proposal
- Auto-Negotiation consider Clause 73 specification negotiate FEC capability through Auto-Negotiation

802.3ba – July 2008

### 40GBASE-CR4 and 100GBASE-CR10 layer diagrams







### 802.3ba copper cable assembly link diagram

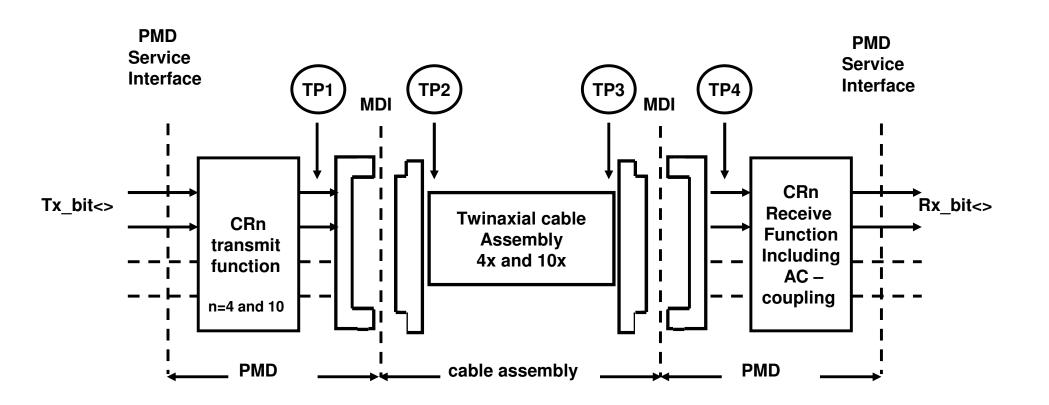


Figure XX–X—40GBASE-CR4 and 100GBASE-CR10 link

### 40GBASE-CR4 and 100GBASE-CR10 cable assembly

#### Cable assembly differential parameters

Description	Value	Unit
Insertion Loss $(f) \le TBD \sqrt{f} + TBD \times f + \frac{TBD}{\sqrt{f}}$	TBD	dB
$NextLoss(f) \ge TBD - TBD \times \log\left(\frac{f}{TBD}\right)$	TBD	dB
$ReturnLoss(f) \ge TBD$	TBD	dB
$MDNextLoss(f) \ge TBD - TBD \times \log\left(\frac{f}{TBD}\right)$	TBD	dB
$ELFEXT (f) \ge TBD - TBD \times \log\left(\frac{f}{TBD}\right)$	TBD	dB
$MDELFEXT(f) \ge TBD - TBD \times \log\left(\frac{f}{TBD}\right)$	TBD	dB

•TBD's > to be determined from measurement models.

#### 100GBASE-CR10 - MDI considered: SFF-8092

- •SFF-8092 Specification for Mini Multilane Series: Shielded High Density Connector (mechanicals).
  - -Scope: The specification defines the plug, guide/strain relief shell, mating interface, footprint, and latching requirements.
  - -x12 proposals currently under consideration in IBTA EWG-QDR
- •40GBASE-CR4 and 100GBASE-CR10 for cable assembly differential parameters.

### 40GBASE-CR4 and 100GBASE-CR10 Auto-Neg

- Adopt Clause 73 (Auto-Negotiation) as a baseline for 40GBASE-CR4 and 100GBASE-CR10 with applicable changes for CR4 and CR10 operation.
  - Use Auto-Neg to Negotiate FEC capability
  - Auto-Neg allows backward compatibility with legacy 10 GbE CX4 PHYs
- Clause 73 provides parallel detection function for compatibility with legacy PHYs that do not support Auto-Negotiation
  - New 40 GbE PHY can use parallel detection for auto-detection of legacy CX4 devices
  - No impact to 10GBASE-CX4 devices
- See ganga\_03\_05\_08.pdf ("FEC and Auto-Neg Proposal for 40/100G Copper Cable Assembly")

### 40GBASE-CR4 and 100GBASE-CR10 Auto-Neg

- Proposed changes for 40GBASE-CR4 and 100GBASE-CR10
  - Add Technology Ability bits from the reserved space to indicate
    - 40GBASE-CR4 ability
    - 100GBASE-CR10 ability
  - Reuse AN management registers
  - No change to negotiate FEC ability
    - FEC when selected to be enabled on all lanes
    - FEC is enabled when both sides advertise FEC ability and at least one side requests to enable FEC
  - No change to Pause ability and Remote Fault bits
  - Parallel detection function to detect legacy 10GBASE-CX4 PHYs

•See ganga\_03\_05\_08.pdf ("FEC and Auto-Neg Proposal for 40/100G Copper Cable Assembly")

#### 40GBASE-CR4 and 100GBASE-CR10 FEC

- Adopt Clause 74 FEC as baseline for an optional sublayer for 40GBASE-CR4 and 100GBASE-CR10 with appropriate changes for CR4 and CR10 operation.
  - Negotiate FEC capability through Auto-Negotiation
  - FEC is optional- allows lowering BER of 10<sup>-12</sup> for integration into systems which require lower BER
  - Correction of burst errors up to 11 bits
  - 2-2.5 dB coding gain
  - No penalty in signaling rate
- Enumerate the FEC encode and decode functions for 4 lane and 10 lane operation
  - Each lane is encoded and decoded independently
  - The coding is performed on a virtual lane basis
  - 4 in case of 40 Gb/s
  - 20 in case of 100 Gb/s
- Commonality with 40 Gb/s backplane solution
- Reuse the management register format
- See ganga\_03\_0508.pdf ("FEC and Auto-Neg Proposal for 40/100G Copper Cable Assembly") for details
- See <a href="http://www.ieee802.org/802">http://www.ieee802.org/802</a> tutorials/july06/10GBASE-KR FEC Tutorial 1407.pdf for FEC tutorial

### QSFP low speed electrical hardware pins

# •For 40GBASE-CR4 copper QSFP low speed control and sense signals set to non-operational QSFP state

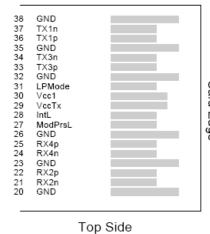
#### 3.1.1.4 ModPrsL

ModPrsL is pulled up to Vcc\_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

#### 3.1.1.5 IntL

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

ModPrsL	IntL	Condition	Signal state
1	0	copper module	ModPrsl open, IntL set low
1	1	no module	both signals open
0	х	module present	ModPrsL set low, IntL either state operational



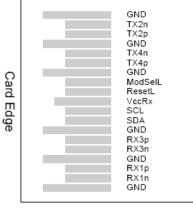


Figure 2 — QSFP Transceiver Pad Layout

Top Side Viewed from Top

Bottom Side Viewed from Bottom

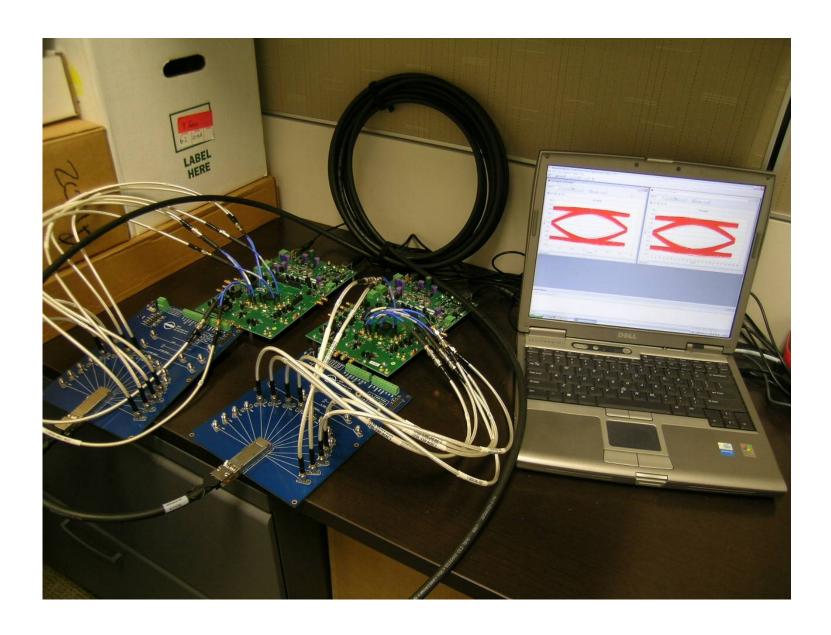
### 10GBASE-KR cable assembly demonstration - Intel

- 10GBASE-KR based device tested over 10 m passive copper assembly under the following setup and conditions
  - 10 meter Leoni 26 AWG passive twinaxial cable with 2 x SFP+ connectors and 1 x 2" and 1 x 4" FR-4 traces on test boards (6" total); ~5 dB worse @ 5 GHz than QSFP 10 meter cable assembly
  - Single NEXT aggressor
  - Adaptive TXFFE with the 10GBASE-KR protocol
  - 5-tap DFE at the receiver
- Test results
  - BER=0 with PRBS31 was measured for 1500 seconds
- Summary
  - Feasibility demonstrated at 10 Gb/s, very promising results with single NEXT aggressor
  - Margin should be sufficient for QSFP Xtalk environment

### 10GBASE-KR cable assembly demonstration - Broadcom

- 10 meter QSFP passive cable assembly including test fixtures (Molex connectors and Leoni cable) tested with Broadcom PHYs designed for compliance to the 10GBASE-KR specification.
- Operation over two lanes; simultaneously transmitting and receiving.
- Lanes selected in closest proximity; pair-to-pair crosstalk but not multi-disturber.
- Additional insertion loss of demonstration:
  - 2 x device verification board trace (2x (1-1.5 in))
  - 2 x 2 ft SMA cables, 2 x .5" SMP cables
- Test ran for more than a day with 0 errors exceeded 10-12 BER objective.
- 10 meter QSFP passive cable assembly including test fixtures:
  - utilized in the 802.3ap ICR analysis validating 802.3ap KR operation over 10 meters of twinaxial copper cable assembly
  - utilized to generate measurement models for Broadcom simulations

### 10GBASE-KR demonstration setup - Broadcom



Source: Vivek Telang, Broadcom

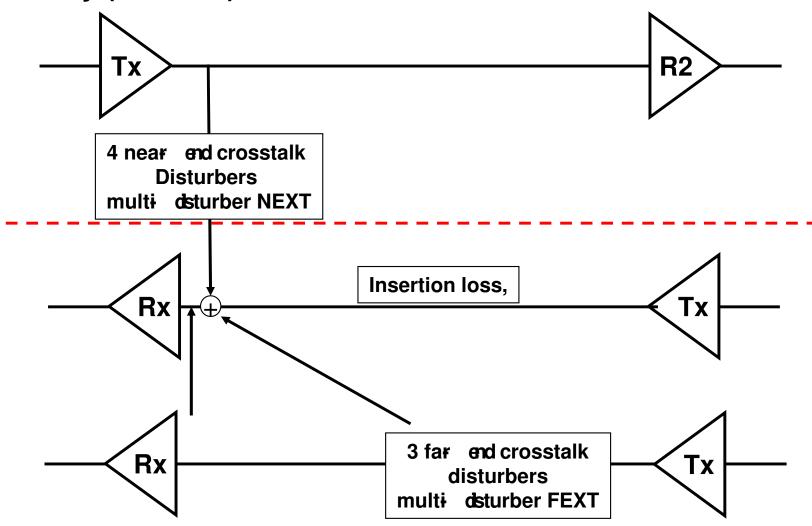
#### 40GBASE-CR4 and 100GBASE-CR10 baseline

- Adopt 10GBASE-KR electrical specifications (Clause 72) for 40GBASE-CR4 and 100GBASE-CR10 baseline electrical specifications with applicable revisions to account for differences in channel parameters e.g., copper cable assembly versus backplane and the 4-lane and 10-lane operation versus serial operation.
- Adopt 10GBASE-CX4 (Clause 54) cable assembly characteristic transmission parameters for 40GBASE-CR4 and 100GBASE-CR10 with TBD's (slide 10) to be determined from measurement models utilized in the feasibility analysis with the additional consideration of specifying the PCB loss between the transmit function and TP1 and the PCB loss between the receiver function block and TP4 in Figure xx-x. TP2 will be used as test reference point for the transmit function which will include the additional specified PCB loss to be measured with the appropriate test fixture; nicholl\_01\_0708.pdf to be used as guidance on minimum PCB length. The channel parameters are expected to fall within the high confidence region as defined for 10GBASE-KR in 802.3ap Annex 69B.
- Adopt 40GBASE-CR4 (x4) MDI QSFP and IEC 61076-3-113 mechanical mating interface (10GBASE-CX4 mechanical) and 100GBASE-CR10 MDI - SFF-8092 Specification for Mini Multilane Series: Shielded High Density Connector (mechanicals).
- Adopt Clause 73 (Auto-Negotiation) as a baseline for 40GBASE-CR4 and 100GBASE-CR10 with appropriate changes for CR4 and CR10 operation.
- Adopt Clause 74 FEC as baseline for an optional sublayer for 40GBASE-CR4 and 100GBASE-CR10 with appropriate changes for CR4 and CR10 operation.

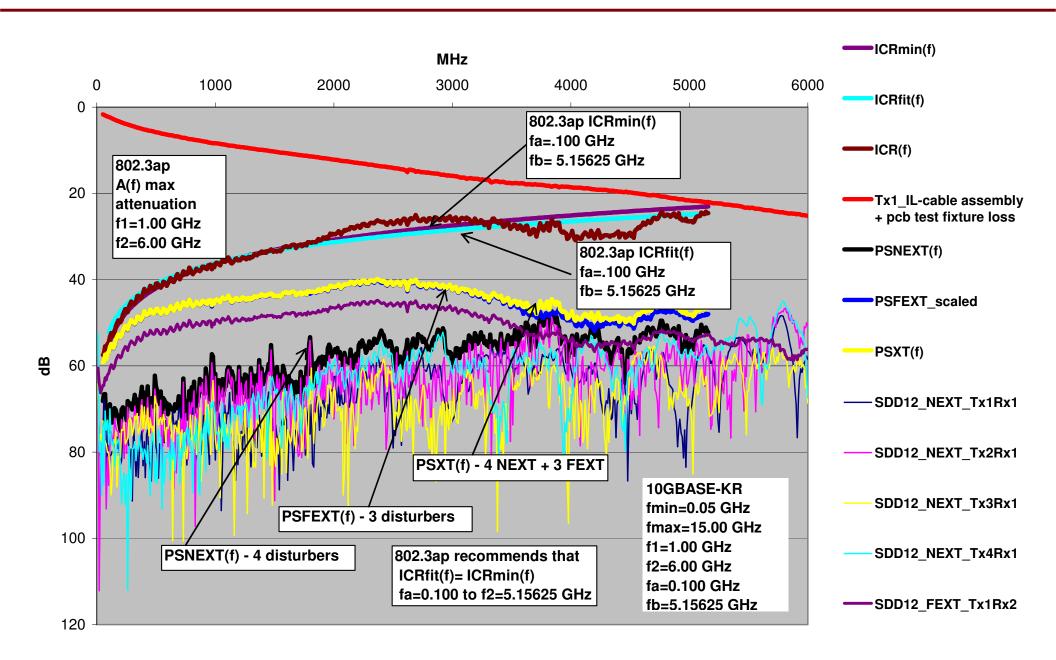
## Backup

### 802.3ap – channel parameter comparisons

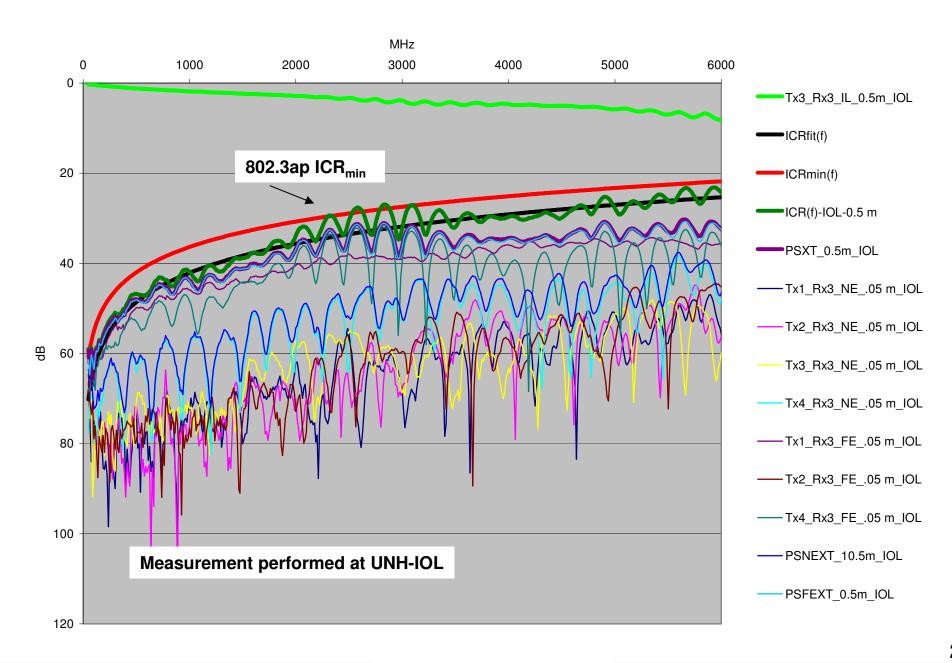
•Insertion loss to crosstalk ratio (ICR) computed from S-parameter measurements and models of QSFP 10 meter copper cable assembly (24 AWG).



#### 802.3ap ICR limits vs 10 m QSFP cable assembly 24 AWG including test fixture



#### 802.3ap ICR limits vs 0.5 m QSFP cable assembly 24 AWG including test fixture

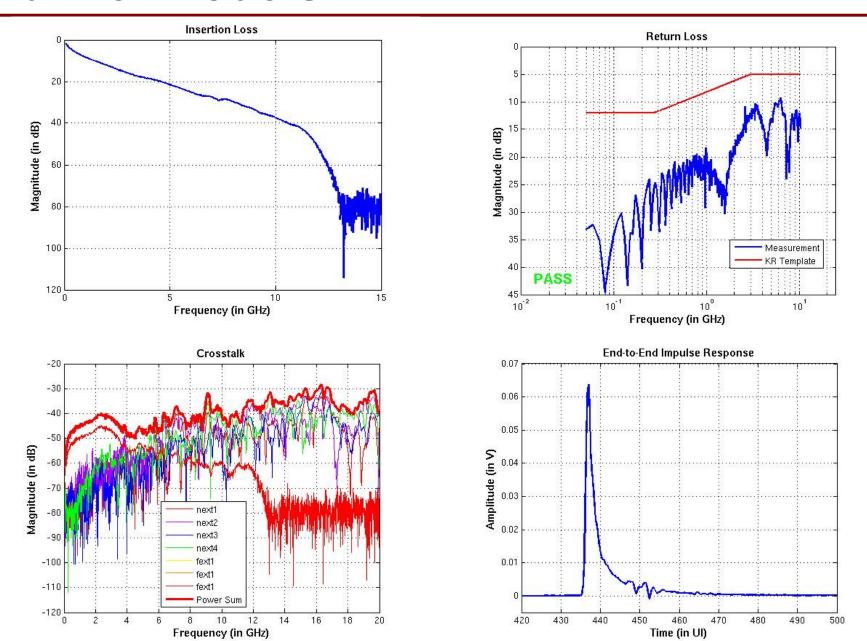


### **Simulation Setup**

- Insertion Loss, Return Loss, Crosstalk per data from Chris DiMinico
- Package models based on measured data
- Receiver architecture same as that used in KR group (802.3ap)
- MATLAB simulations
  - Pulse Response "Frequency-domain" Analysis, with MMSE optimization
- Performance evaluation based on detailed, worst-case error probabilities (not simple Gaussian assumption)
- On-chip impairments included
  - Clock jitter, Offsets, Front-end noise, Detailed analog circuit models, Detailed equalizer implementation penalties
- Worst-casing of ISI data patterns and crosstalk phase

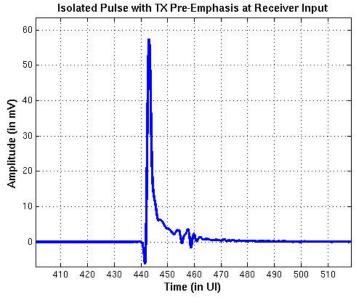
Source: Vivek Telang, Broadcom

### **Channel models**

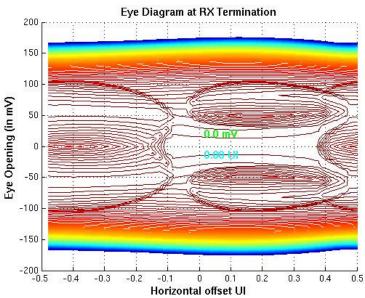


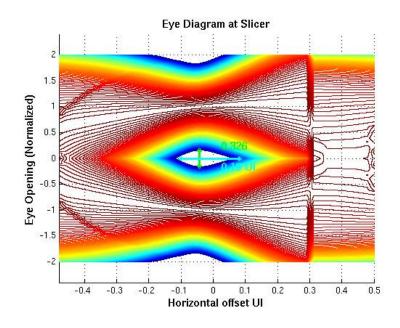
Source: Vivek Telang, Broadcom

### Simulation results



Slicer SNR & BER		
SNR (dB)	BER	
18.5	1.4x10 <sup>-17</sup>	





Source: Vivek Telang, Broadcom

### 1000BASE-CX (short-haul copper) - MDI

39. Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

Connectors meeting the requirements of 39.5.1.1 (Style-1) and 39.5.1.2 (Style-2) shall be used as the mechanical interface between the PMD of 39.3 and the jumper cable assembly of 39.4. The plug connector shall be used on the jumper cable assembly and the receptacle on the PHY. Style-1 or style-2 connectors may be used as the MDI interface. To limit possible cross-plugging with non-1000BASE-CX interfaces that make use of the Style-1 connector, it is recommended that the Style-2 connector be used as the MDI connector.

39.8.3 Major capabilities/options

39.8.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

39.8.4.1 PMD functional specifications

\*STY1 Style-1 MDI 39.5 Either the style-1 or the style-2

MDI must be provided O/1 Yes [] No [] \*STY2 Style-2 MDI 39.5 O/1 Yes [] No []