PMD Clocking Discussion

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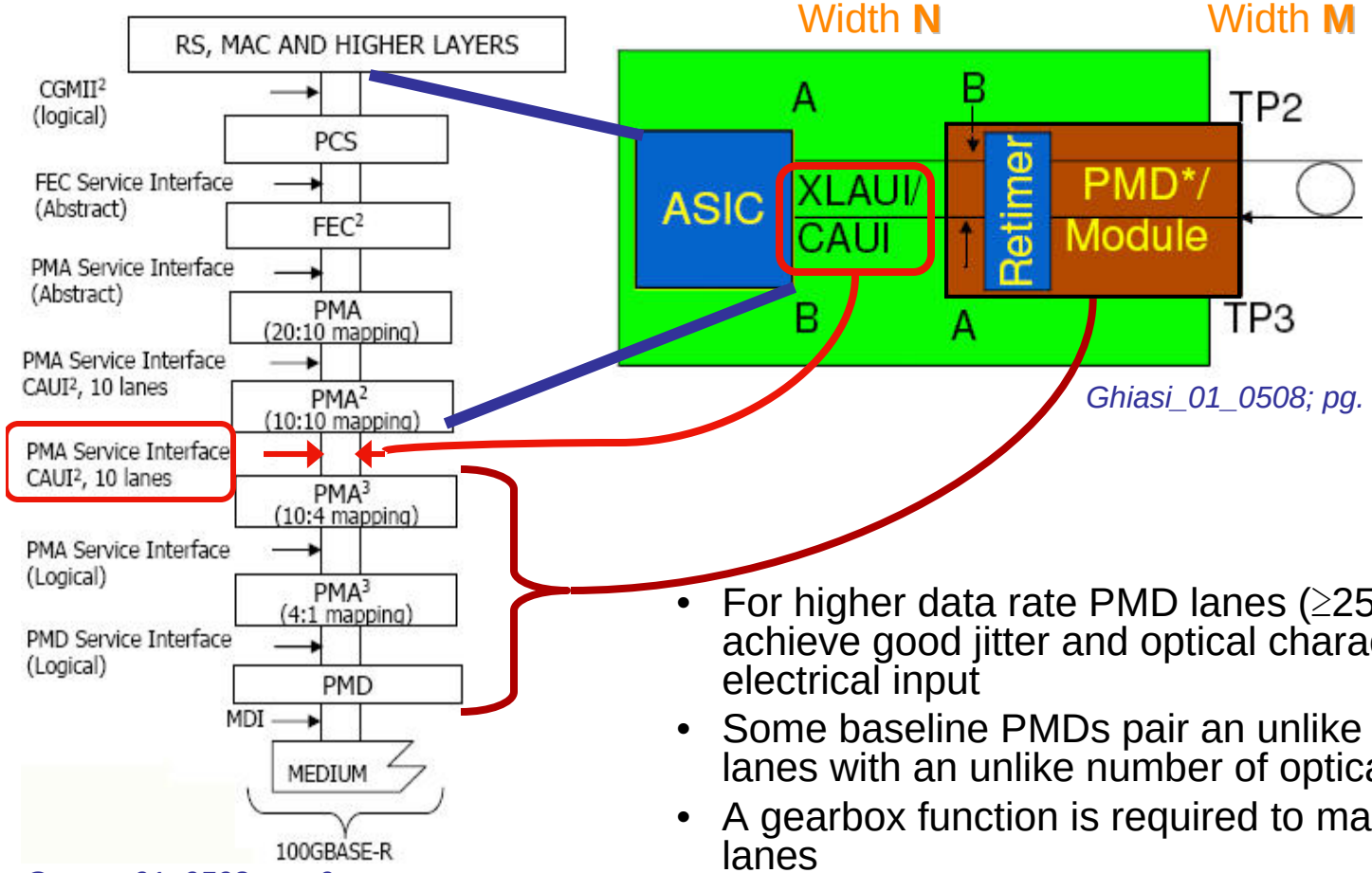
Tadashi Hatano
Matt Traverso

Implementation Example for N ≠ M (1)



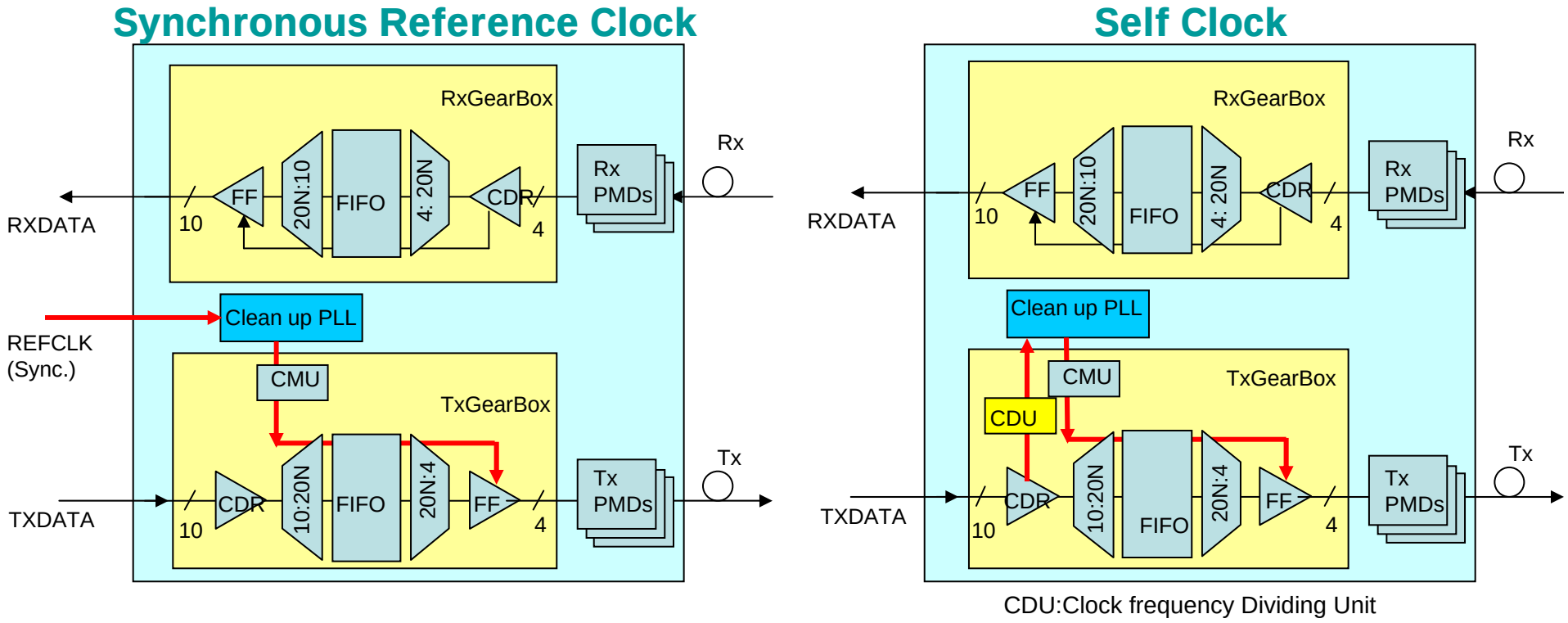
Ganga_01_0508; pg. 6

Ghiasi_01_0508; pg. 6

- For higher data rate PMD lanes (≥25G) it is difficult to achieve good jitter and optical characteristics with degraded electrical input
- Some baseline PMDs pair an unlike number of electrical lanes with an unlike number of optical lanes; N ≠ M
- A gearbox function is required to map the N lanes to the M lanes
- A clock is required to provide superior jitter & optical characteristics & perform this mapping correctly

Implementation Example for N ≠ M (2)

- Shown below is an example of 100GBASE-LR4 or ER4 with CAUI interface
- Two clock philosophies are possible; Synchronous vs. Self (embedded in data)



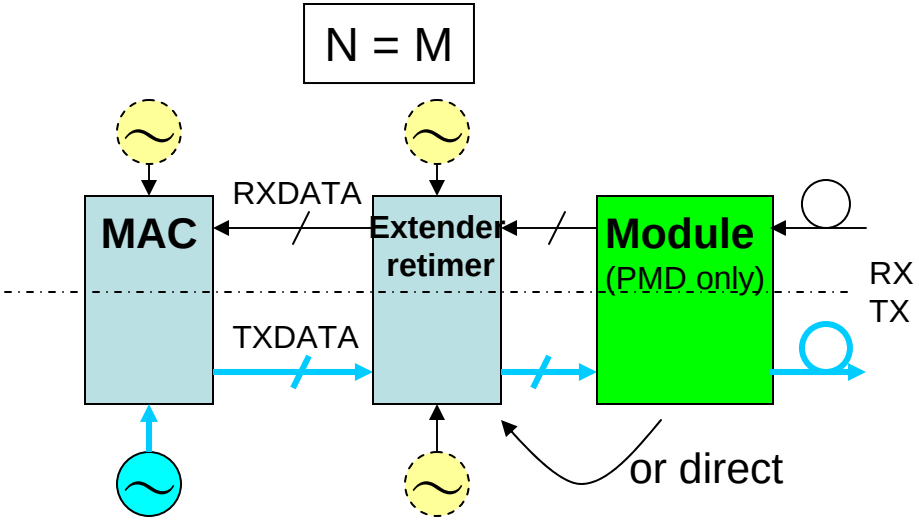
CDU:Clock frequency Dividing Unit

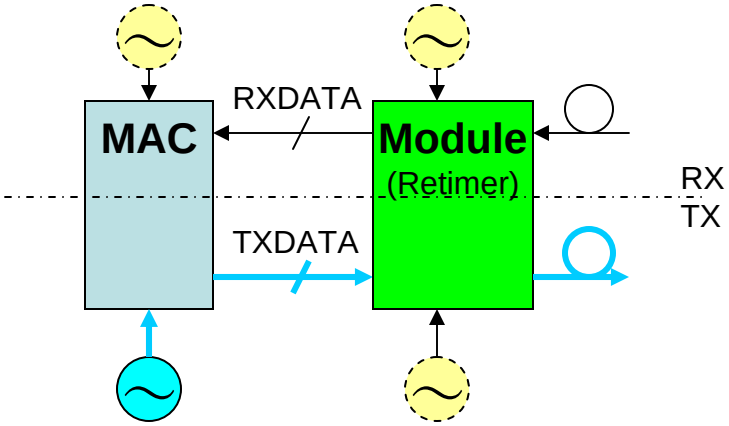
Clocking path (synchronous to Tx data)
: determines Tx output characteristics.

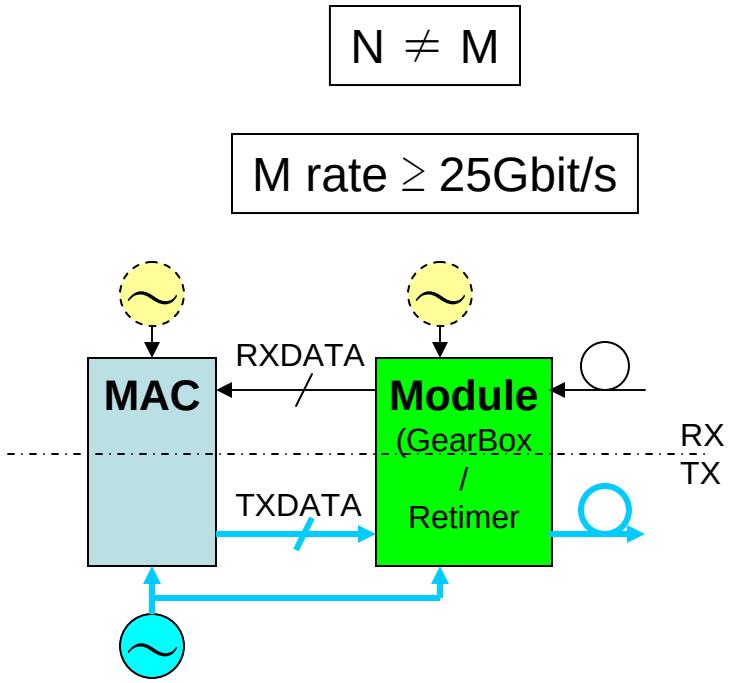
Clocking Discussion

- Clocking can impact jitter and waveform characteristics
  - Self clocking type can be more sensitive to data channel & emphasis effects
  - CDU (Clock Dividing Unit) may be adversely affected by unexpected channel characteristics
- Longer reaches & higher baud rates benefit from better jitter and waveform characteristics
  - Longer reaches such as >40km (possibly 40km) will benefit from a “cleaner” signal
  - Higher baud rates – eg. future serial implementation – will require very low jitter interfaces

Suggested Clocking Scheme for 100GbE/40GbE







: Synchronous(Tx) clock

: Local (Async.) clock

Conclusion

- Propose that the XLAUI / CAUI contain an optional (but recommended) synchronous clock for those PMDs where $N \neq M$

- Propose that the XLAUI / CAUI contain an optional synchronous clock for those PMDs where the PMD lane rate is 25Gbit/s or greater