



40GbE 10km SMF Objective: Serial

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(Network Carrier)

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Glenn Wellbrock, Verizon
Osamu Ishida, NTT
Shoukei Kobayashi, NTT
Hidenori Takahashi, KDDI Labs
Ralf-Peter Braun, Deutsche Telekom
Dirk Breuer, Deutsche Telekom

(System Supplier)

Hiroshi Onaka, Fujitsu
Youich Akasaka, Fujitsu labs
Satoshi Obara, Fujitsu
Shinji Nishimura, Hitachi Ltd
Hidehiro Toyoda, Hitachi Ltd
Mike Shahine, Ciena
Sashi Thiagarajan, Ciena
Li Zeng, Huawei

(Transceiver Supplier)

Mike Dudek, JDSU
Ed Cornejo, Opnext
Atsushi Takai, Opnext

(Device Supplier)

Farzin Firoozmand, SMI
Craig Hornbuckle, SMI
Med Belhadj, Cortina
Hitoshi Watanabe, Mitsubishi Electric
Sosaku Sawada, Eudyna
Keiji Sato, Eudyna
Hao Feng, Eudyna
Tetsuya Kinoshita, Kyocera Corporation
Walter Crofut, Narda
Med Belhadj, Cortina
Jen Fiedler, U2T
Frank Chang, Vitesse

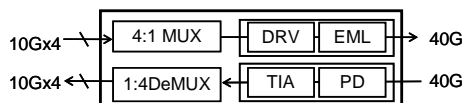
Outline

- Status
- Technical Feasibility
- Economic Feasibility
- Link Budget
- Summary

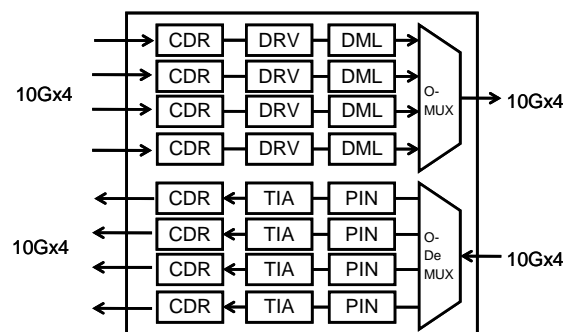
Status

- 40GbE over 10km of SMF was adopted as an Objective to address servers, datacenters and access interconnection (*barbieri_01_0308*, *simsarian_01_0308*)
- In the past two options have been discussed

Serial (*jewell_03_0508*)



CWDM 4x10G (*cole_03_0508*)



- This proposal addresses the merits of **Serial 40 GE**
 - **Technical feasibility**
 - **Economic feasibility**
 - **Link Budget**

Technical Feasibility

40GbE Serial Risk Assessment

“ With the availability of low cost package, faster process, higher volume of Ethernet the cost for 40G optics and Serdes will be significantly reduced.”

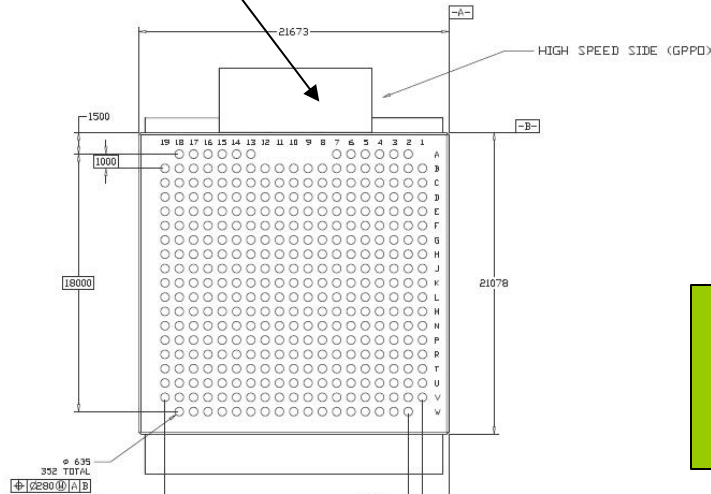
Excerpt “jewell_03_0508.pdf”

- Low Cost Package
- Faster Process
- Higher Volume Ethernet
- *See subsequent foils for each bullet*

Low Cost Package (1) – Serdes

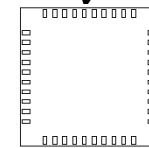
Serdes packaging

Today's OC768 Serdes (16:1)
Package

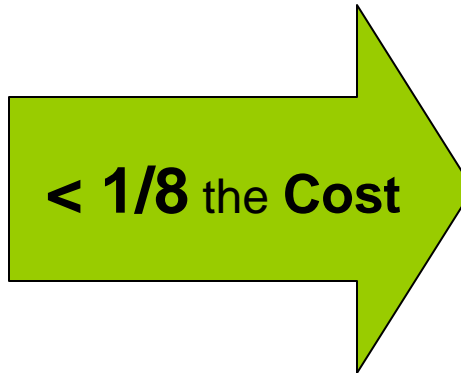


21x21mm
Connectorized GPPO

40GE Proposed Serdes (4:1)
Package

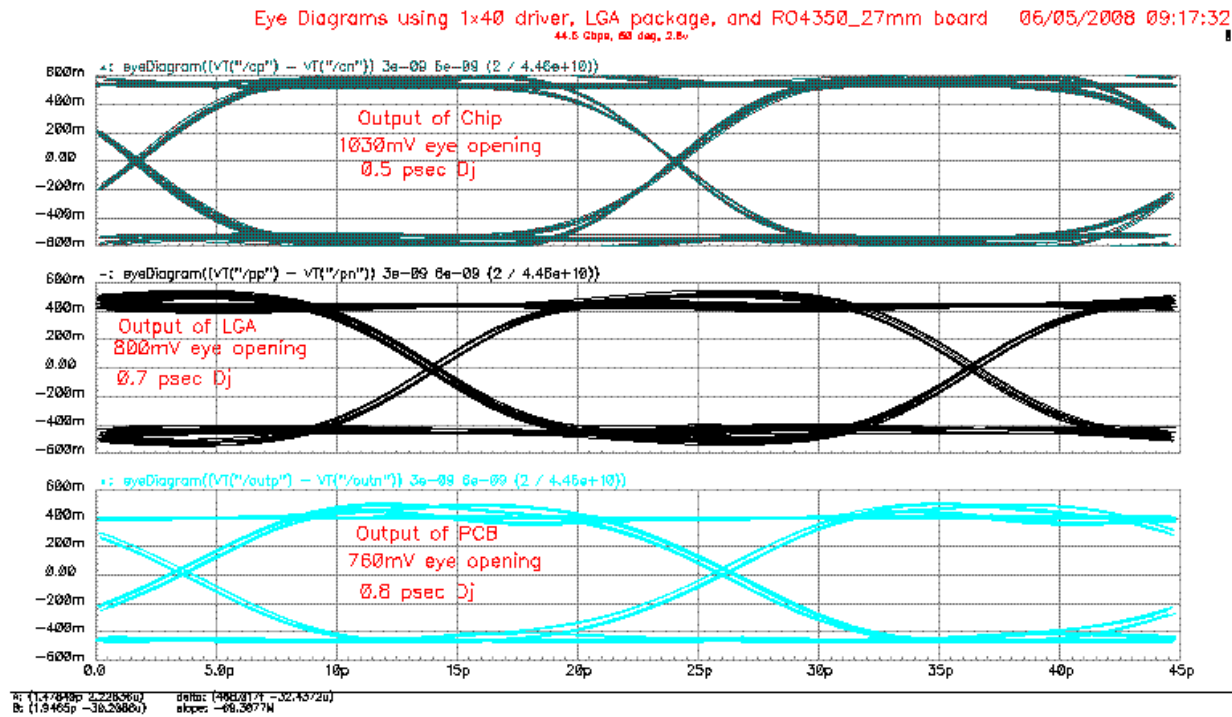


7x7mm SMT package
AVAILABLE TODAY



Low Risk -- Available today

Low Cost Package (1): Simulation Results of Serdes



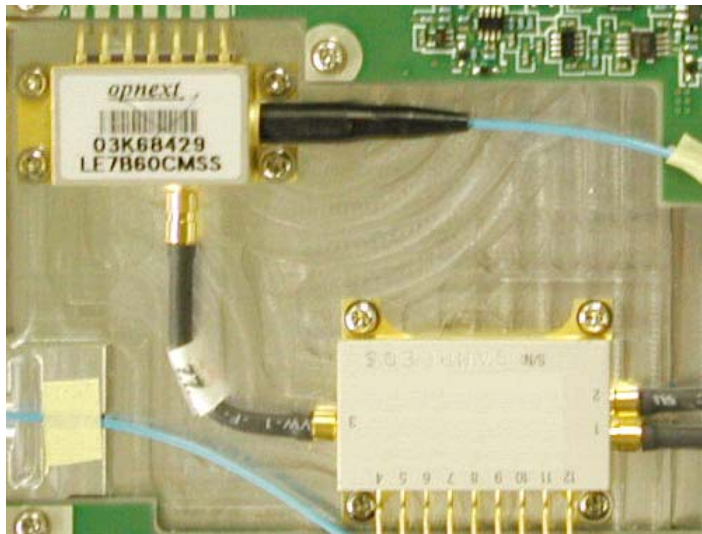
**Mux Driver
Output**

**LGA Pad
(PCB Launch)**

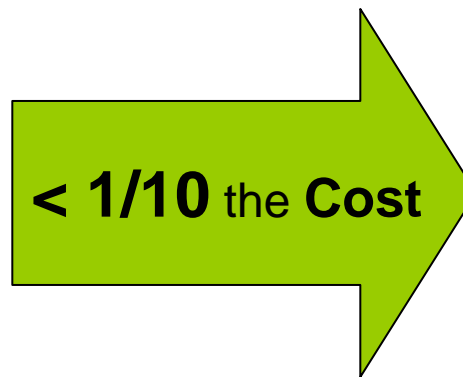
**PCB Far-end
(EML Driver)**

Signal integrity over receiver path (PIN/TIA to Demux) has also been verified to meet the proposed sensitivity and link budget with margin.

Low Cost Package (2)- Optical Components



OC768: EA-DFB and EA Driver are packaged separately and GPPO interconnected between them



40GE Proposed TOSA Package (*1)



Small package TOSA w/ EA driver (13.3x8.0x5.6 mm)

*1; T. Yagisawa, et al., OECC/ACOFT 2008, Fujitsu Labs

Low Risk -- Available today

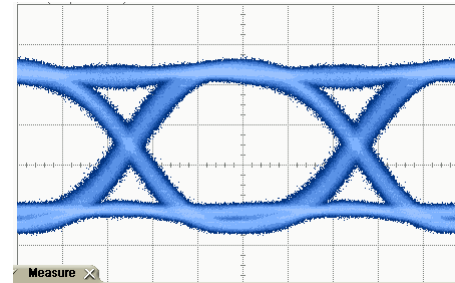
Low Cost Package (3): Measurement Results of TOSA Output Waveform



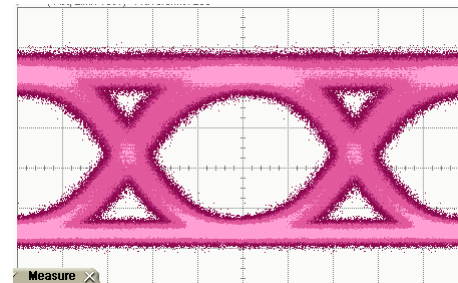
Small package TOSA
w/ EA driver

39.8Gb/s PRBS31 Waveform

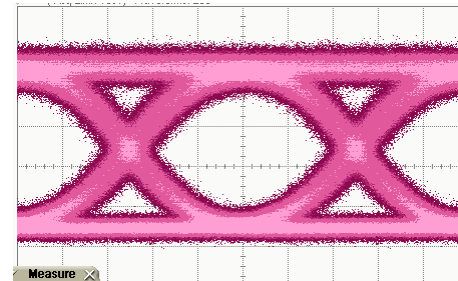
Electrical input



Optical Output
@Tc=25C

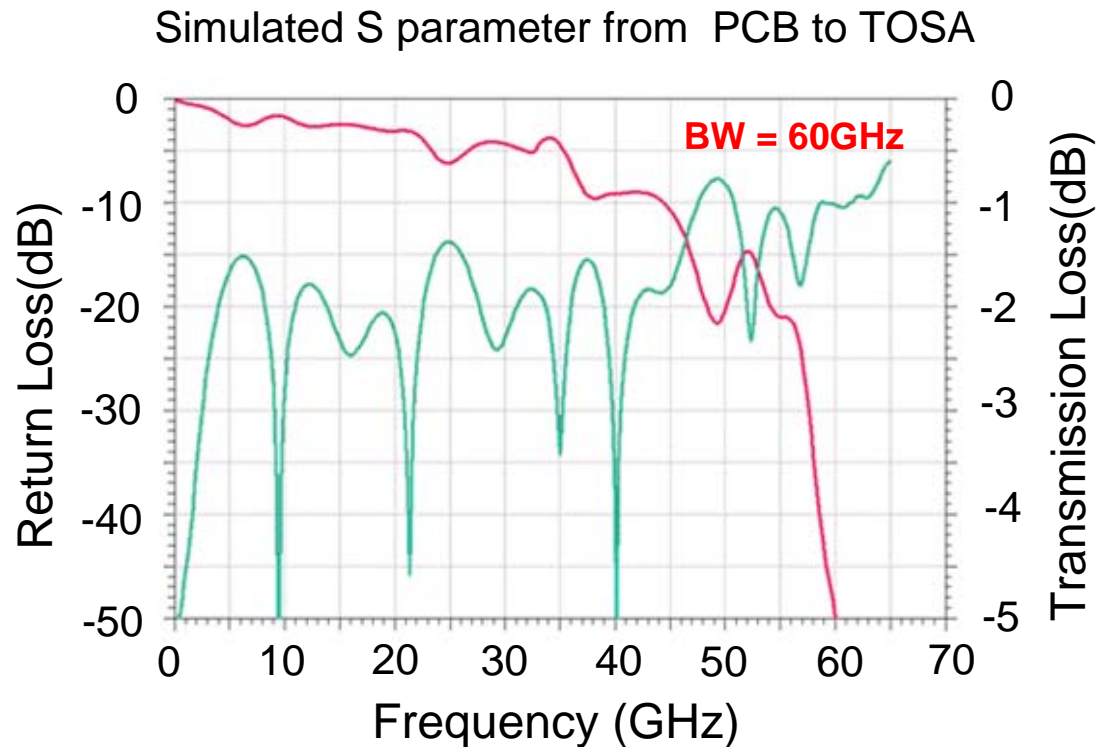
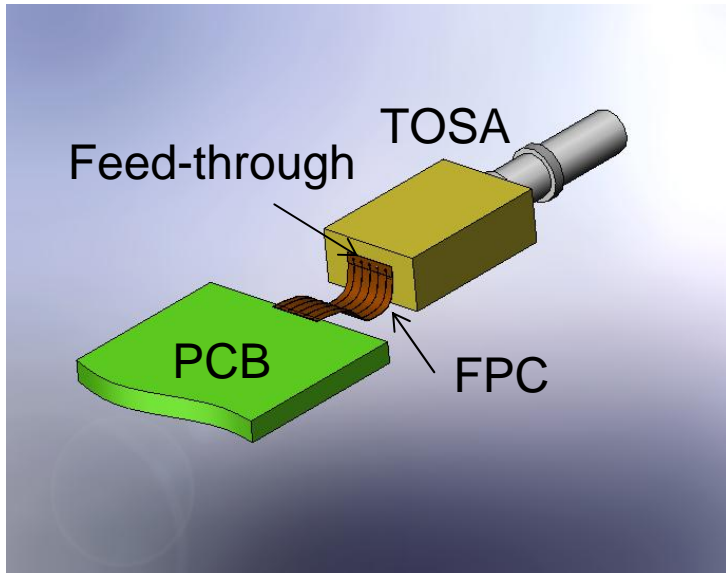


Optical Output
@Tc=70C



H: 5ps/div.

Low Cost Package (2): Simulation Results of Frequency Responses



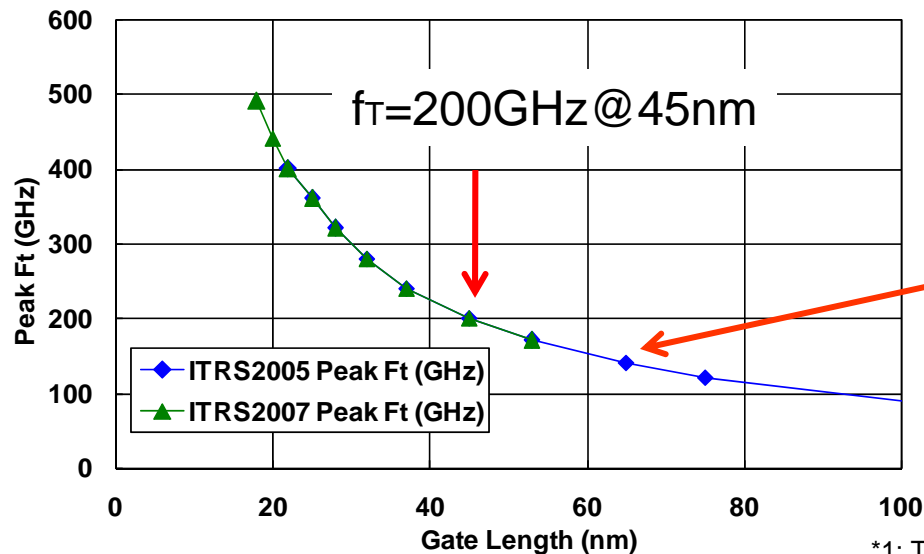
Almost the same interconnection method with 10G-XMD MSA is applicable.

Faster Process

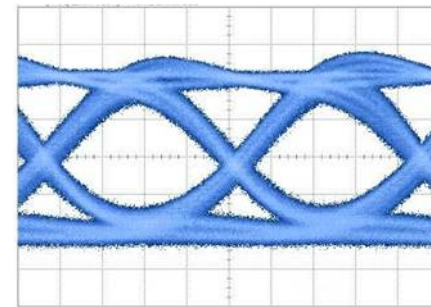
- SiGe is available to meet the immediate requirement; CMOS can address the long term demand
- CMOS; Low power CDR (73mW) is available today (*1)

45nm CMOS is sufficient for 40Gb/s Driver

CMOS f_T ITRS Road-Map (*2-3)



**40Gb/s Driver Output Waveform
In 65nm standard CMOS**



V: 100mV/div.
H: 5ps/div.

*1; T. Toifl, et al., D12-3, ISSCC2007, IBM

*2; http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Wireless.pdf

*3; <http://www.itrs.net/Links/2005ITRS/Wireless2005.pdf>

Low Risk -- Available today

IEEE 802.3ba Task Force - July 14-17, 2008 - Denver, CO

Power Comparison -- Serial vs. CWDM

From "jewell_03_0508.pdf"

40G 10km Serial	Y2009 Power (W)	Y2011 Power (W)	40G 10km CWDM	Y2009* Power (W)	Y2011** Power (W)
EML TOSA TEC + Laser Bias	1.5	1.0	DML TOSA/Mux	0	0
EML Driver	0.8	0.6	4X DML Driver	2.1	1.7
4:1 / 1:4 MUX/DMUX/CDR	2.0†	1.5††	XFI CDR	1.8	1.0
PIN/TIA	0.4	0.3	4XPIN/TIA ROSA	0.7	0.5
Other	0.1	0.1		0.4	0.4
Total Power	4.8	3.5		5.0	3.6
Ratio to CWDM	0.96	0.97		1	1

* Intermediate between "Now" and "2010" values from Tsumura's presentation to the 40GbE SMF Ad-hoc

** Slightly reduced from the "2010" values from Tsumura - 40GbE SMF Ad-hoc

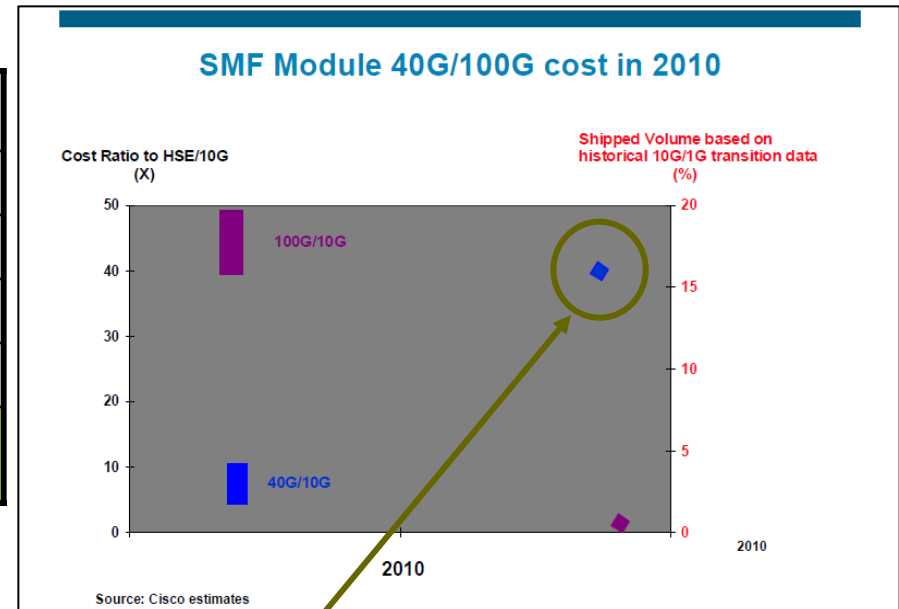
† SiGe

†† CMOS

Higher Volume for 40GE 10km SMF

From "carter_40_01_0208.pdf"

	2010	2011	2012	
10GE Total	1600K	1800K	2500K	<i>Note1</i>
40/10 ratio	15%	20%	20%	<i>Note2</i>
40GE Total	240K	360K	500K	
40GE LR %	50%	50%	50%	<i>Note3</i>
40GE 10km	120K	180K	250K	



40GbE is estimated to be 15% of the volume of 10GbE

Note1; LightCounting estimation for 2010 & 2011. Yr 2012 is estimate

Note2; Estimated from carter_40_01_0208.pdf (40GbE SMF Ad-hoc)

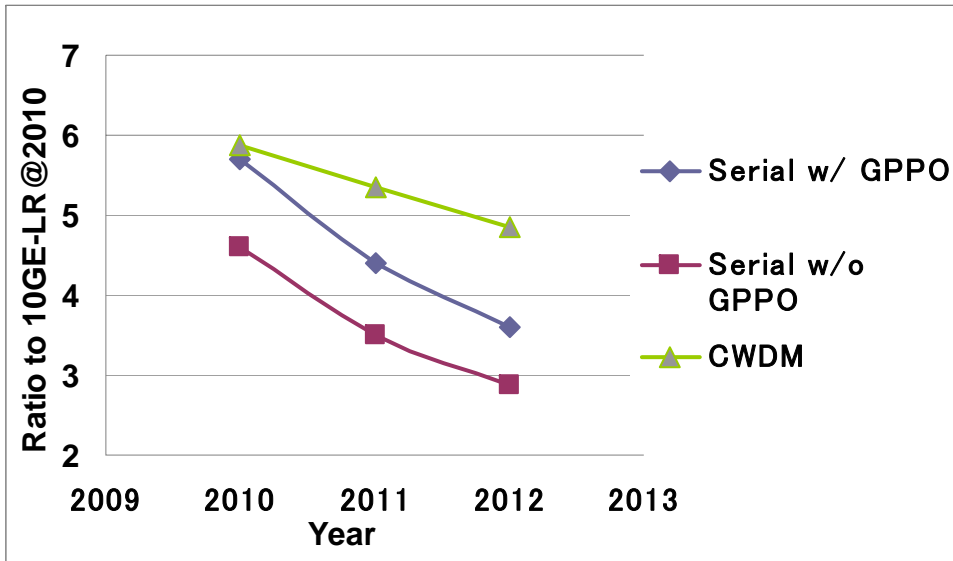
Note3; Ratio on distance is referred to "goergen_01_1107", where around 50% for 10km category is reported.

Economic Feasibility

- Known cost factors, reliable data
 - Reasonable cost for performance
 - Consideration of installation costs
-

- The general consensus (including CWDM advocates) is that serial will be cost effective in long term.
- Recent survey among many optical and electronic component vendors suggests the serial will be MORE cost competitive than CWDM in mid YR 2010
- LX4 is NOT cost effective comparing to 10GBASE-LR, 10GBASE-SR and 10GBASE-LRM.
- CWDM will require significant investment in optical packaging. High Speed IC technology is amortized across all IC applications.

Cost analysis versus 10GbE-LR for both 40G 10km CWDM & Serial



Serial provides more cost-effective solution than CWDM after yr2010.

Estimated values are ratio referred to 10GE LR for each component respectively.

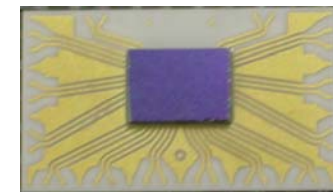
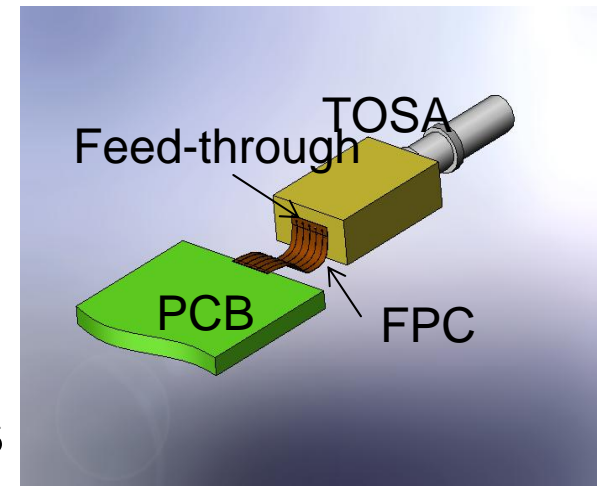
Relative Cost Comparison

Component	10GE LR	Serial w/o GPPO			CWDM		
	2010	2010	2011	2012	2010	2011	2012
TOSA/ROSA w/O-Mux, Demux	1.0	5.9	4.4	3.4	8.4	7.5	6.8
CDR/SerDes	1.0	7.5	5.0	4.0	4.0	3.6	3.2
Other component	1.0	1.8	1.8	1.8	1.7	1.7	1.7
TEST	1.0	2.0	1.8	1.6	4.0	3.6	3.2
Total	1.0	4.6	3.5	2.9	5.9	5.3	4.9

Main Drivers to Drop Serial Cost in 2010

(From “traverso_04_0308.pdf”)

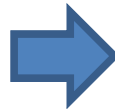
- Optics packaging
- 4:1 Serdes instead of 16:1 Serdes
- Low cost SerDes packaging
- Low cost RF interconnect
 - Substrate interconnection via micro-stripline or stripline
- High volume



40G Serial Link Budget

40G Serial (Based on jewell_03_0508)

ITU based		
TX ER	8.0	dB
Tx_min_Ave	0.2	dBm
Fiber loss	4.2	dB
Connector loss	2.0	dB
Margin	0.0 *1	dB
Path Penalty	1.0	dB
Rx_Sen_Ave	-7.0 *2	dBm



IEEE Based			
TX ER	8.0	dB	
Tx_min_OMA	1.8	dBm	
Fiber loss	4.2	dB	
Connector loss	2.0	dB	
Margin	0.0	dB	
TDP	Dispersion Penalty	1.0	dB
	Transmitter Penalty	1.6 *3	dB
Rx_Sen_OMA	-7.0	dBm	
Power Budget	8.8	dB	

*1; Set margin 0dB for even comparison with CWDM case

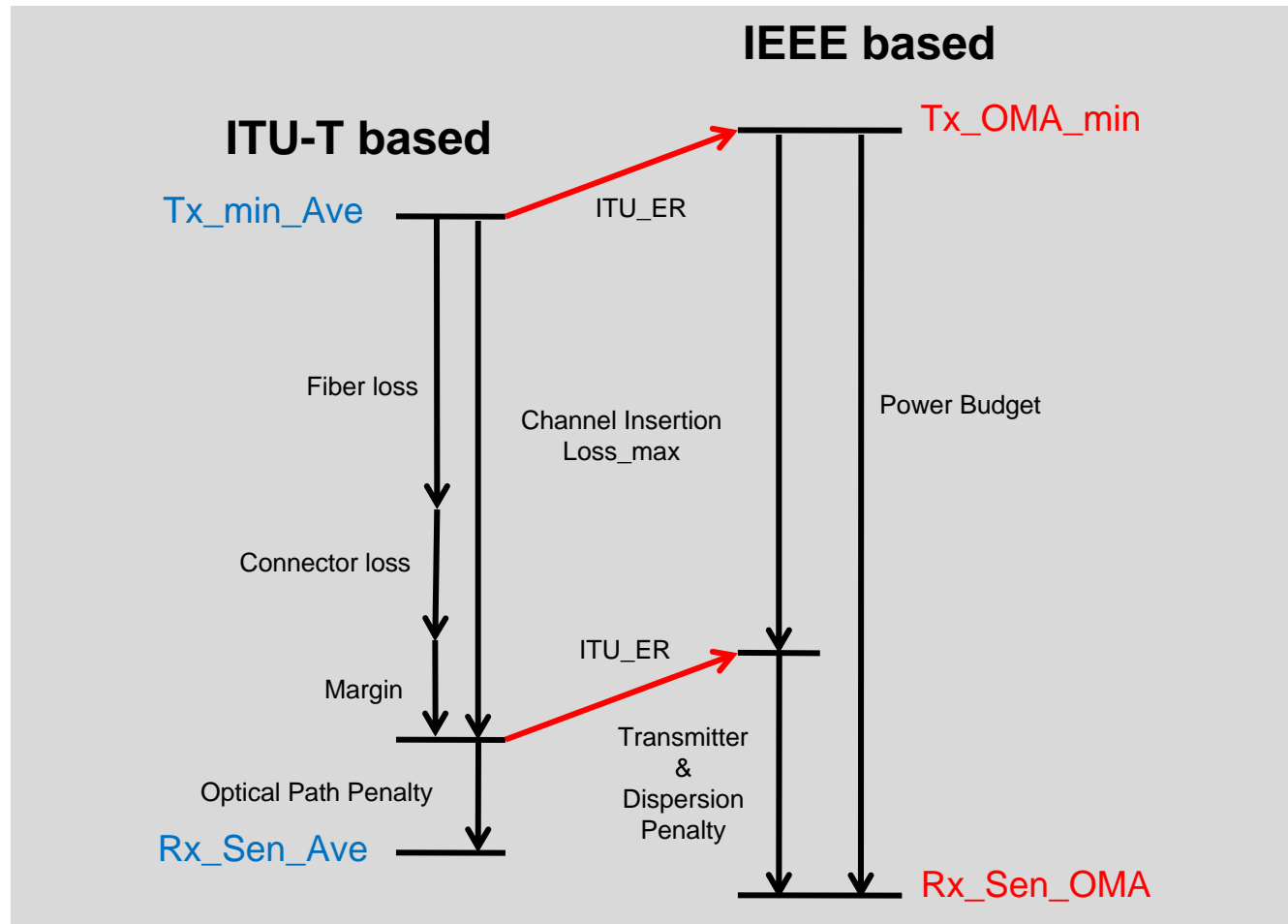
*2; Set Rx_Sen_Ave same value of ITU spec.

*3; Calculated with IEEE spreadsheet

The IEEE Rx sensitivity is defined for perfect signal, Tx penalty is assigned given the real eye pattern.

Link Budget (IEEE vs. ITU)

Based on 3av_0707_hamano_1.pdf for easy understand

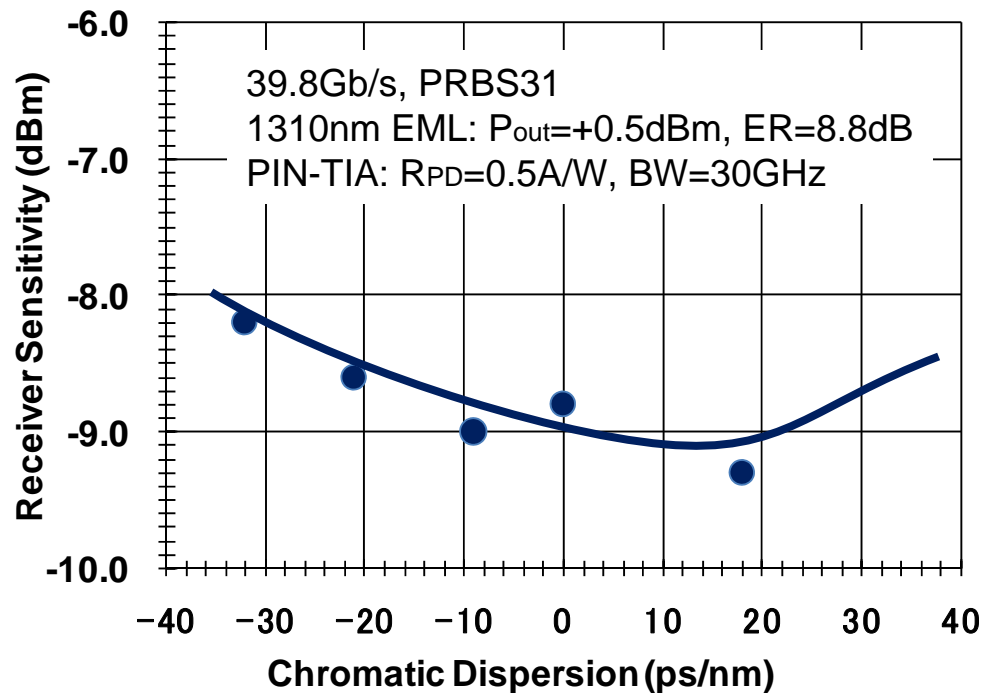


Technical Feasibility – Practical Link Demo

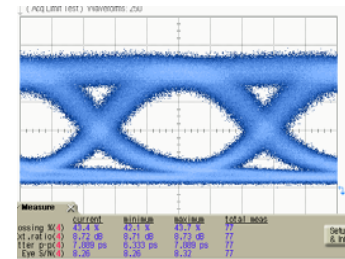
- 40G serial transmission results from 1310nm EML and PIN/TIA ROSA

CD penalty: <1.0dB

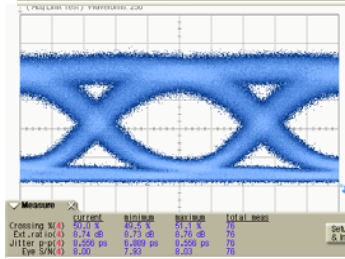
Rx sensitivity: <-9dBm(Avr.)



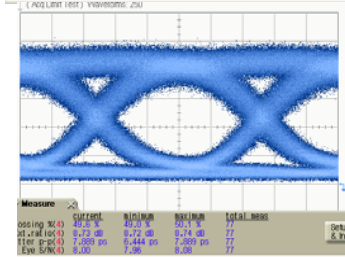
-21 ps/nm



B to B



+17 ps/nm



5ps/div.

Summary

- Recommend the 802.3ba task force to adopt 40GbE Serial PMD for 10Km SMF
 - Is the only long term viable solution to stay
 - Technical feasibility
 - Packaging technology – Available today
 - Process technology – Available today
 - Power consumption – Lower than CWDM
 - Economic feasibility
 - Lower cost than CWDM when volume ramps (mid 2010)
 - Serial PMD cost reduction follows silicon cost reduction path
 - Accelerates the deployment of high volume 40Gb Ethernet
 - Eliminates standardization of 2 PMDs