Additional Concerns on CR4/CR10 Specifications

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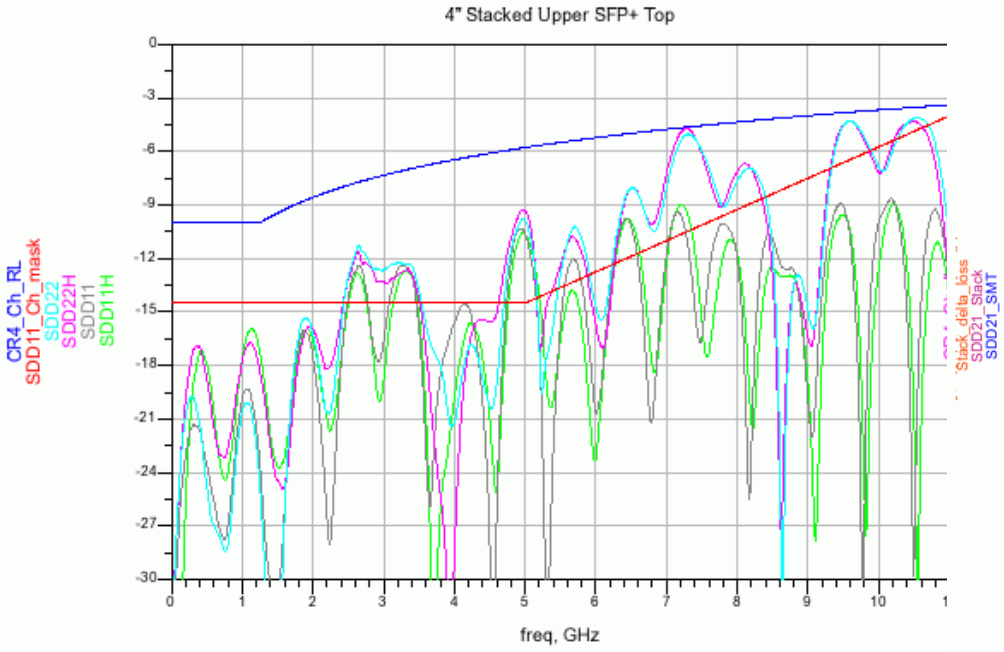
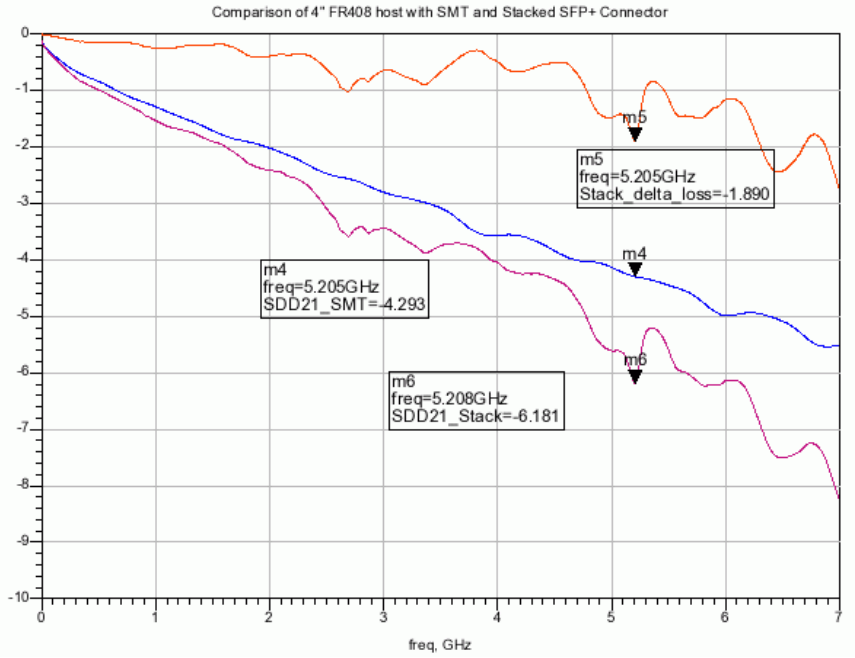
CR4/CR10 High Level Problem Statement

- Current PCB loss from TP0-TP1 or from TP4-TP5 has only 2.3 dB loss allocation which does not allow a practical physical implementation
- 3 dB ILD margin was taken out of KR and allocated to IL without consideration for stacked connector combined with relaxed cable return loss
- Reference cable data used for CR4/CR10 simulation has about 10 dB better return loss than cable return loss specifications
- The Reference QSFP 10 m cable loss from pair to pair varied by as much as 3 dB, but the cable with lowest loss is included in the standard
- FEXT on adjacent pair are not included in the CR4/CR10 baseline analysis, when worst case FEXT included then PSXT increase by 6-10 dB in the critical high frequency region resulting in ILD crossover in just few 100 MHz!
- CR4/CR10 electrical level are 50% higher than SR4/SR10
- CR4/CR10 still require significant amount work to improve the compliance and test methodology but this is secondary at this point!

PCB Loss for Common Host Implementation

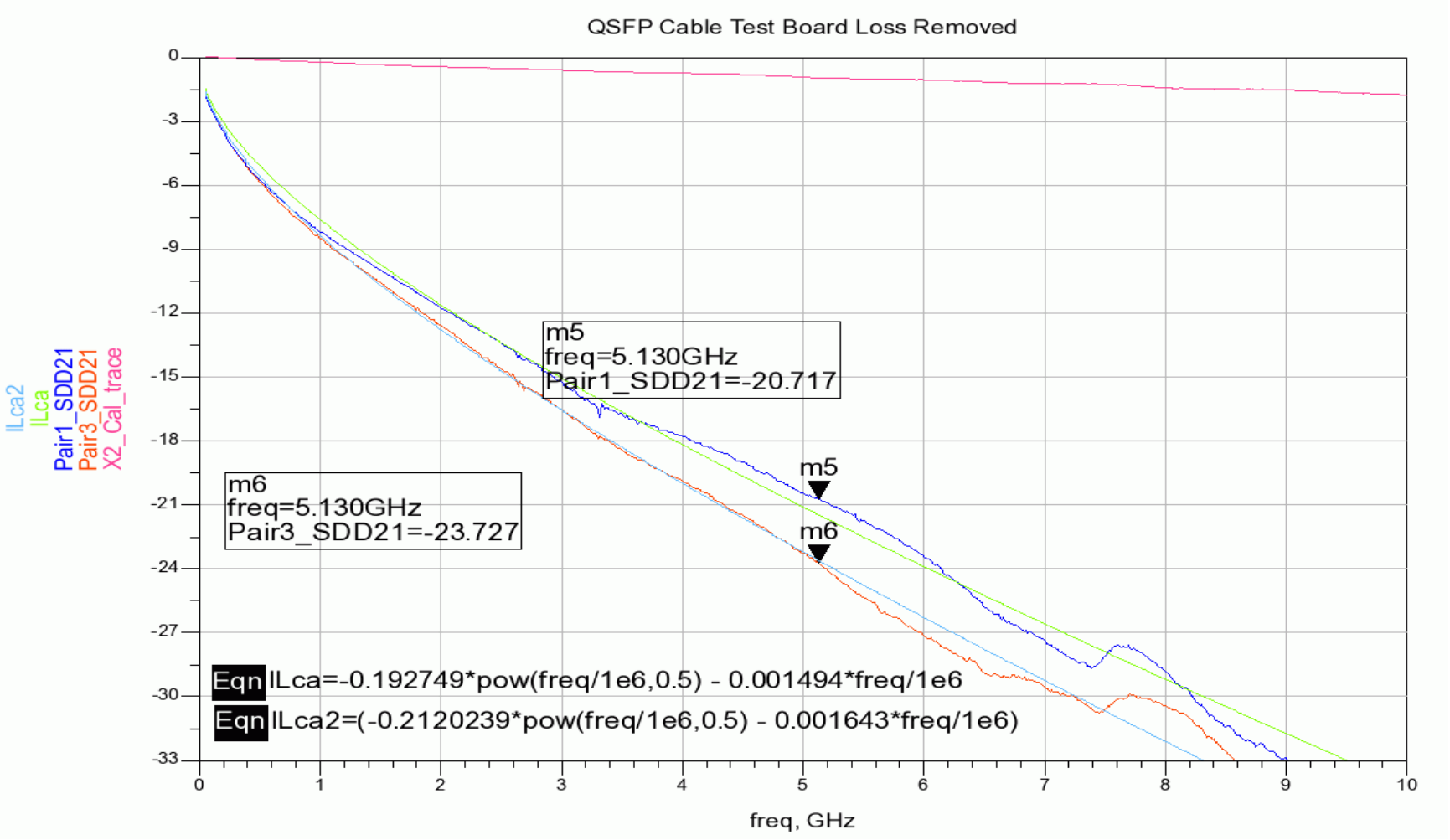
- **Host with 4” trace 5 mils stripline on FR4-08 has 6.2 dB for stack connector and 4.3 dB for the SMT connector**
  - **The stack connector delta loss is about 1-1.5 dB!**
- **Large port count switches require at least 10” of PCB trace!**
  - **With current CR4/CR10 PCB loss budget even N4000-13 will not meet the 2.3 dB budget.**
- **Current CR4/CR10 PCB and cable RL as shown below can produce 2-3 dB of ILD on each end!**





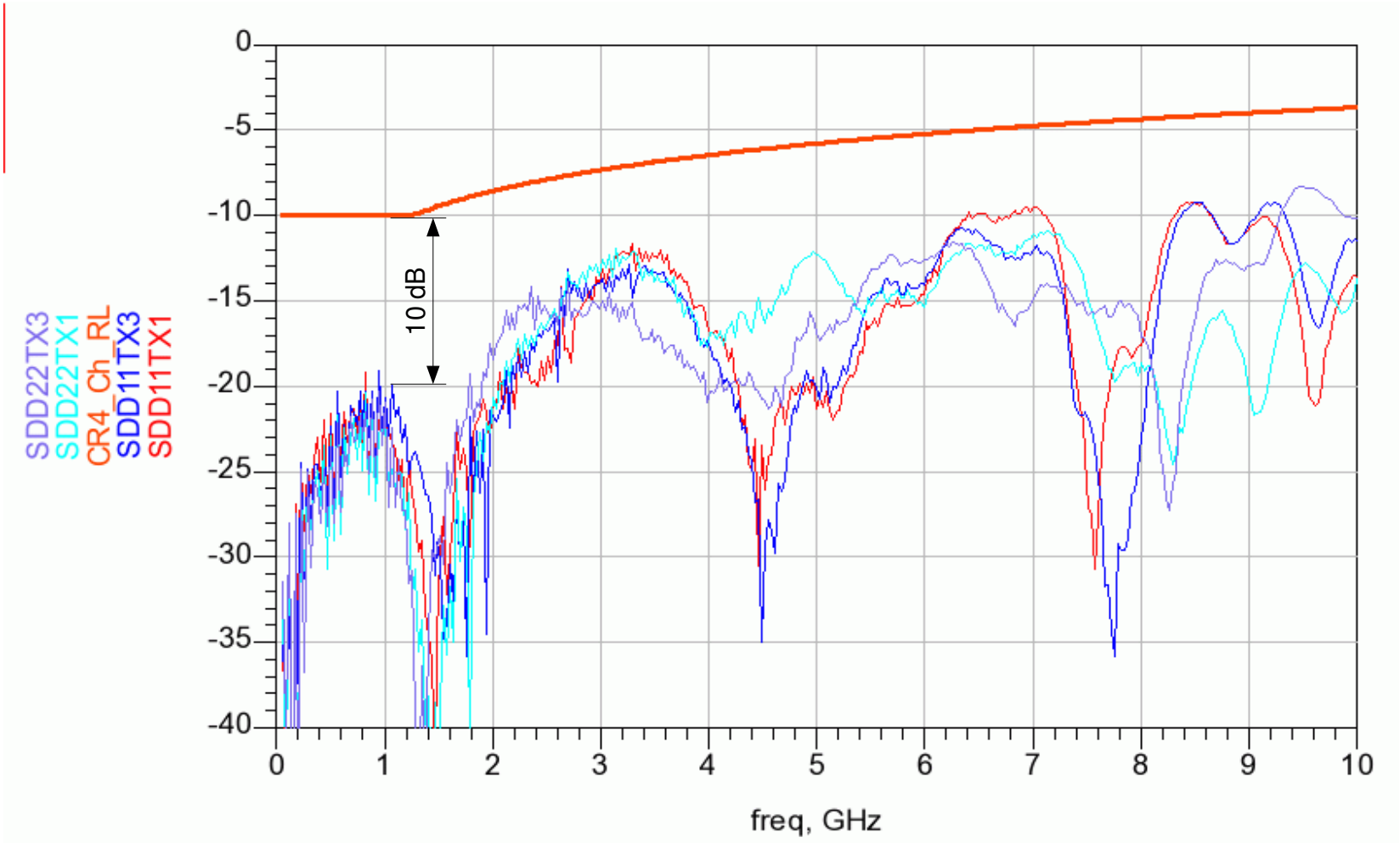
Reference 10 m QSFP Cable Loss

- **Low loss pair matches Eq 85-50 exactly, but high loss pair has 3 dB more loss!**



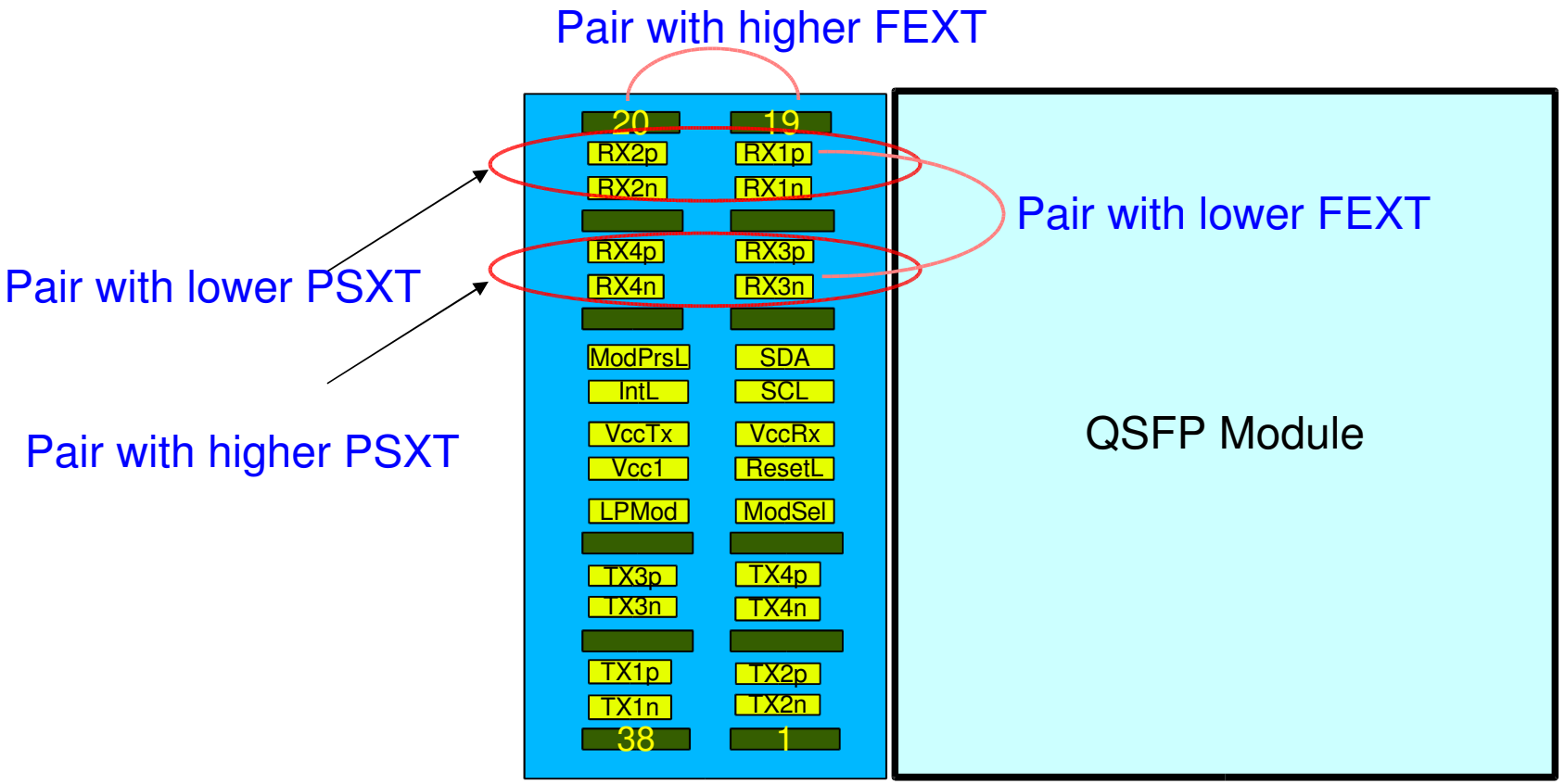
Reference 10 m QSFP Cable Return Loss

- **Cable return specifications Eq 85-60 is 10 dB worse than reference cable!**

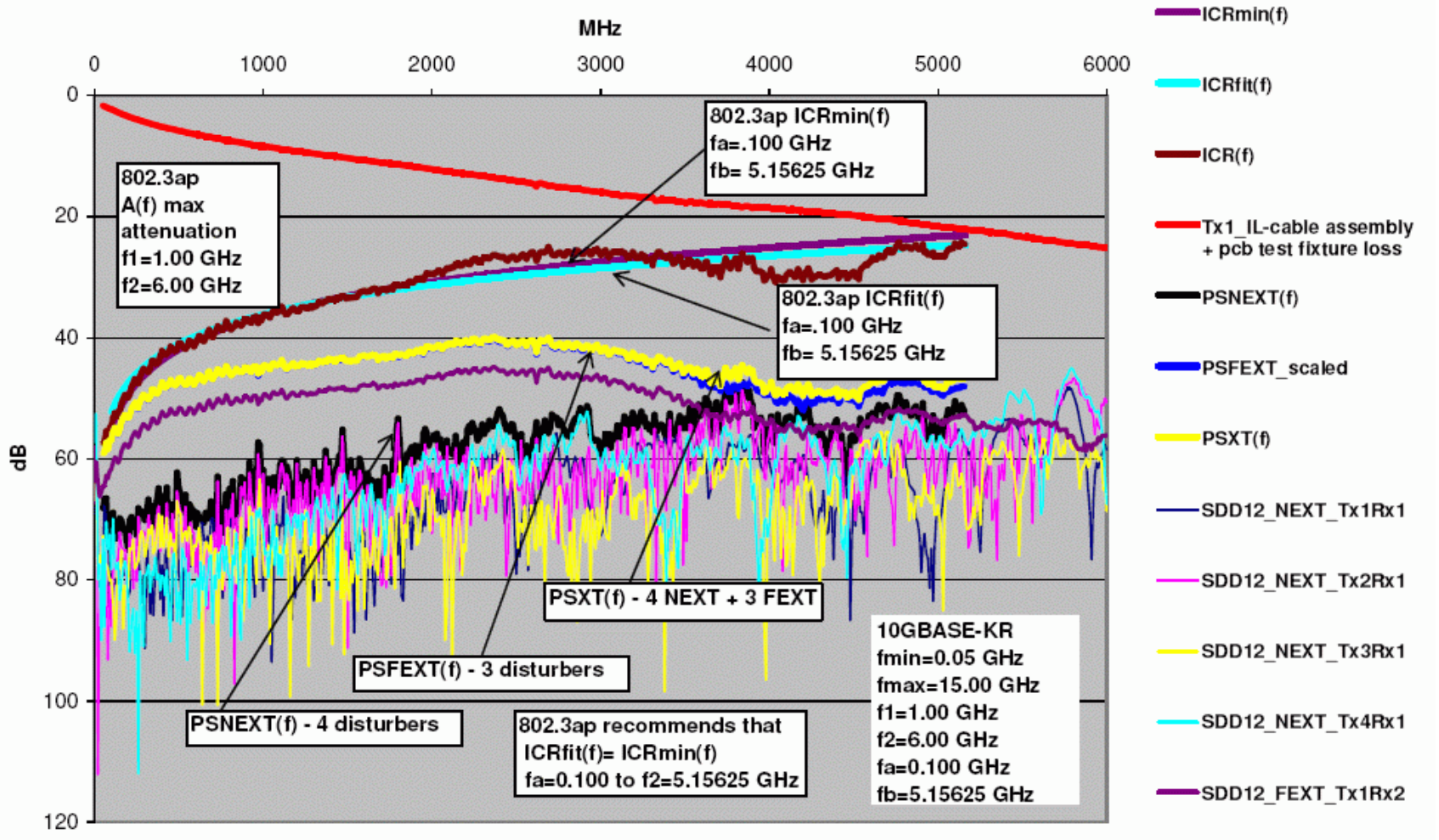


Where is the Source of Additional FEXT

- **It appear that worst case FEXT data (RX4 and RX3) were not included in daminico_01_0708**

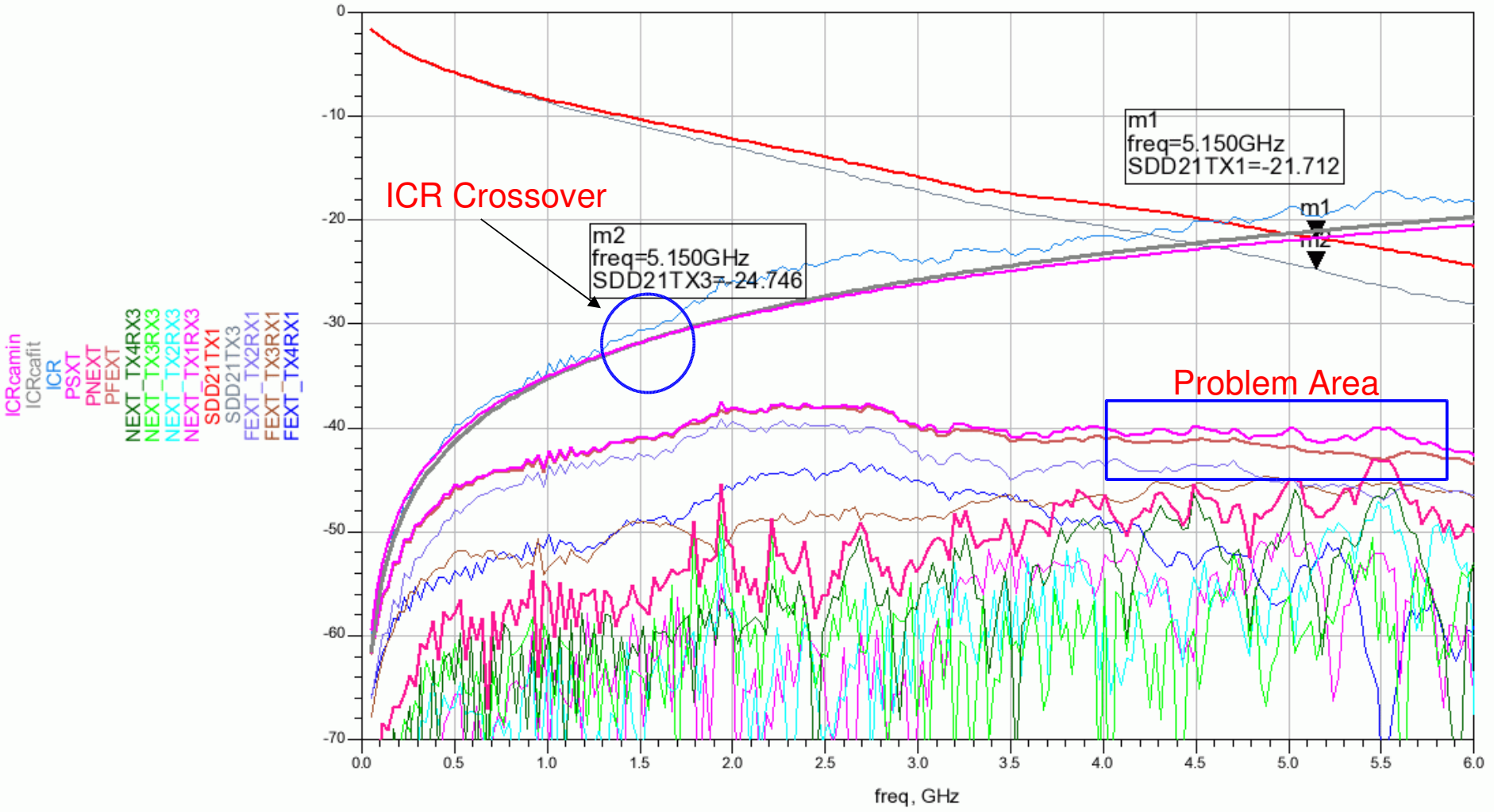


FEXT and ILD Analysis from Diminico_01_0708



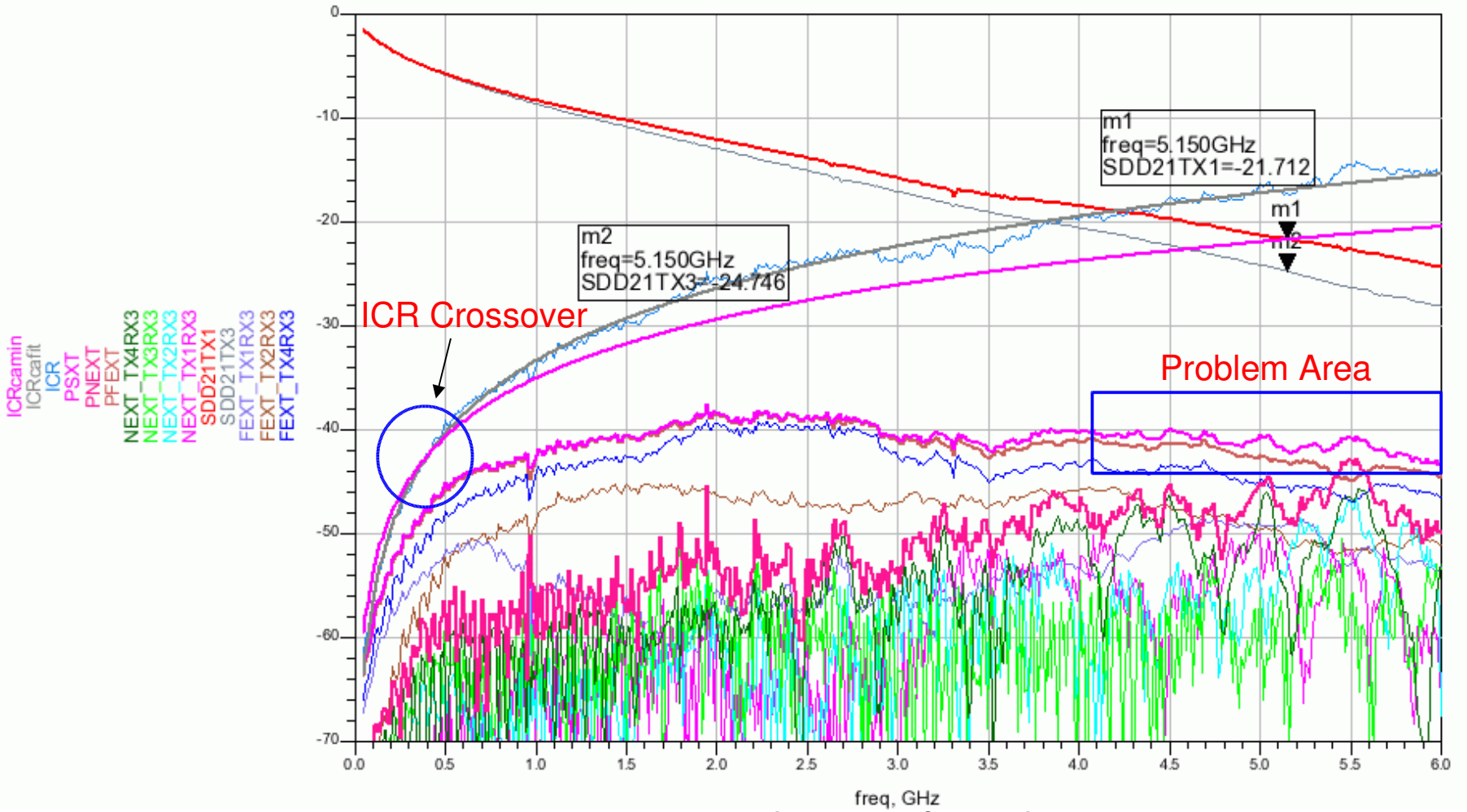
FEXT and ILD on Low Loss Cable Pair

- **Including 3 FEXT disturber on RX1**
  - **Used 4 NEXT disturber on RX3 instead since RX1 is one signal pair further away**



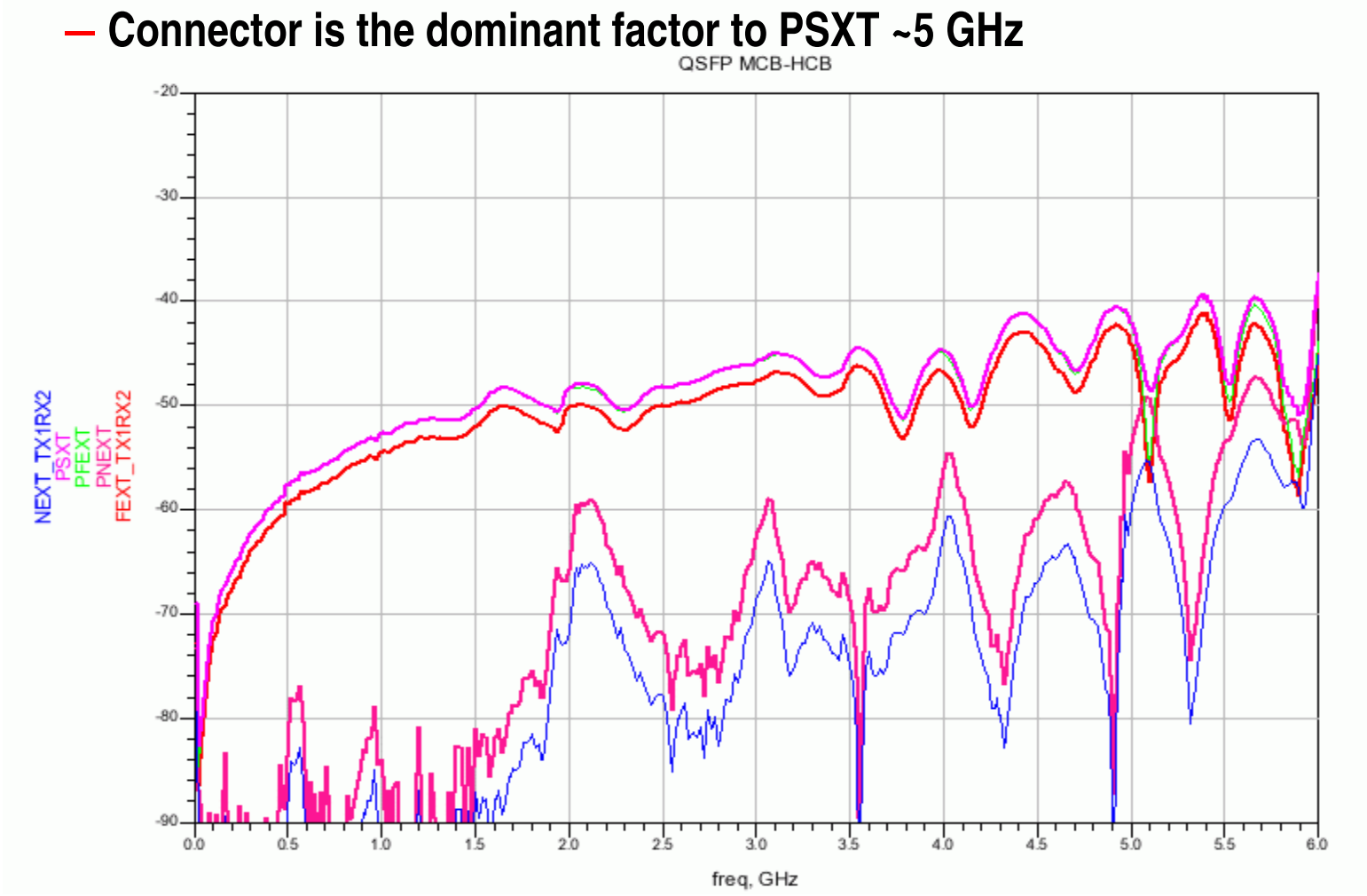
FEXT and ILD on High Loss Cable Pair

- **Including 4 NEXT disturber and 3 FEXT disturber on RX3**



QSFP MCB-HCB FEXT-NEXT

- PNEXT assumed to be 4x TX1RX2 NEXT
- PFEXT 2 dB higher than PFEXT for TX1RX2
- Connector is the dominant factor to PSXT ~5 GHz



Assumptions in Diminico_01_0708 Technical Analysis

- Insertion Loss, Return Loss, Crosstalk per data from Chris DiMinico
- Package models based on measured data
- Receiver architecture same as that used in KR group (802.3ap)
- MATLAB simulations
  - Pulse Response "Frequency-domain" Analysis, with MMSE optimization
- Performance evaluation based on detailed, worst-case error probabilities (not simple Gaussian assumption)
- On-chip impairments included
  - Clock jitter, Offsets, Front-end noise, Detailed analog circuit models, Detailed equalizer implementation penalties
- Worst-casing of ISI data patterns and crosstalk phase

Source: Vivek Telang, Broadcom

Lack of Commonality Between CL85 and CL86 is Alarming

- SR4 physical instantiation is the same as CR4 style 1 connector
- SR10 physical instantiation is the same CR10 connector
- Electrical level
  - CL85 electrical I/O level are 1200 mV
  - CL86 output 770 mV and max input 850 mV
  - CL85 electrical levels are 50% higher than CL86 and could potential damage the module!
- When CL85 and CL86 have same physical instantiation they should have the same return loss
- We should either make the electrical level for CL85 and 86 identical or define hardware key
  - The logical and the green choice is to use CL86 electrical levels as hardware key forces removes the option of Cu and optics plug and play that SFP+ offers.

Option Moving Forward

- **Do nothing**
  - **Would result in cable or host passing but link failing!**
- **Spin off clause 85 into a new project**
- **Delay revision 2.2 by at least one meeting cycle in order to close the copper budget as many of the baseline assumption must be verified**
  - **Expect 5 m reach**