802.3ba CR4/10, SR4/SR10 loss budgets

Marco Mazzini, Mark Gustlin, Lin Shen, Gary Nicholl, Pirooz Tooyserkani - Cisco

John D’Ambrosia – Force10 Networks

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Supporters

Joel Goergen – Force10 Networks
Scott Kipp - Brocade
Shashi Patel – Brocade
Jaya Bandyopadhyay – Juniper Networks
Jeffery Maki - Juniper Networks
Petar Pepeljugoski - IBM Research
Dan Dove – HP
David Law - 3com
Shimon Muller - Sun

Tom Palkert – Xilinx, Luxtera
Jerry Pepper – Ixia
Thananya Baldwin – Ixia
Larry Green – Ixia
George Noh - Vitesse
Brad Booth - AMCC
Matt Brown - AMCC
Ryan Latchman – Gennum
Frank Chang – Vitesse
Mike Dudek - Independent
Matt Traverso - Opnext

Overview

- The CR4/CR10 PCB loss allowances are not sufficient for future PCB board designs, and do not support 4” of standard PCB trace
- Clause 86A and 85 are not consistent in their PCB loss budgets.
  See dawe_05_0509 for comparison based on D2.0
- We need to allow for integration of multi-port PHYs, stacked connectors, and reasonably priced PCB materials (included lead free considerations)
- We need loss budget for reflections, stubs and other impairments

CR4/10 channel definition

The 40GBASE-CR4 and 100GBASE-CR10 channel is defined between the transmitter (TP0) and receiver blocks (TP5) to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss as illustrated in Figure 85–2. Annex 85A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. Two mated connector pairs have been included in the cable assembly specifications defined in 85.10.

Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0-TP1 and TP4-TP5 respectively are provided informatively in Annex 85A.

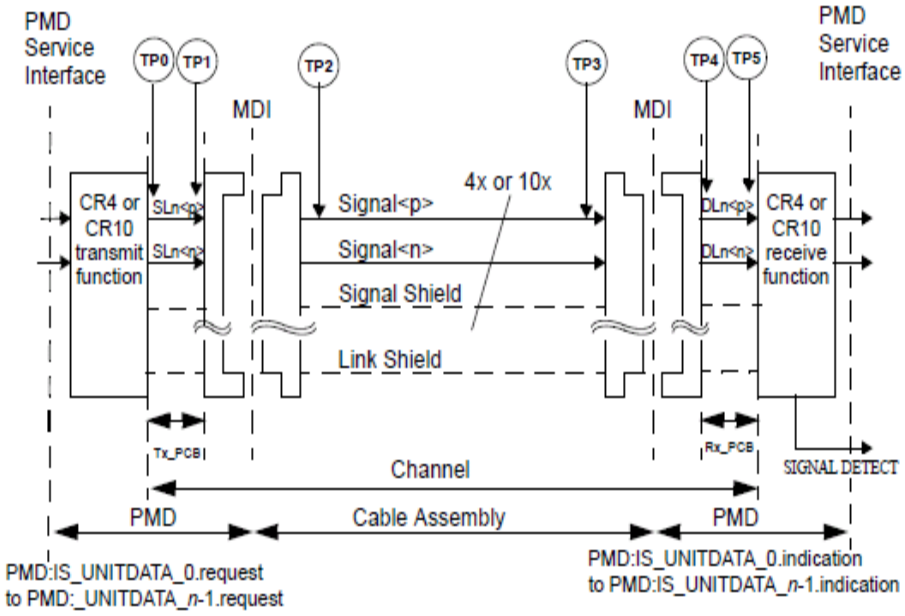


Figure 85–2—40GBASE-CR4 and 100GBASE-CR10 link (half link is illustrated)

NOTE—The source lanes (SL), signals SLn<p> and SLn<n>, are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DLn<p> and DLn<n>, are the positive and negative sides of the receivers differential signal pairs for lane n (n = 0, 1, 2, 3 or n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9).

85A.5 Channel insertion loss

The maximum channel insertion loss is determined using Equation (85A-3) where f is expressed in MHz.

$$IL_{Ch}(f) \le IL_{Chmax}(f) = IL_{Camax}(f) + IL_{PCBmax}(f) \quad \text{dB} \qquad (85A\text{-}3)$$

for 50 MHz $\le f \le$ 5156.25 MHz.

where

$IL_{PCBmax}(f)$ The sum of the transmit PCB loss and the receive PCB loss depicted in Figure 85–2.

$IL_{Camax}(f)$ The maximum cable assembly insertion loss determined using Equation (85–51).

The maximum channel insertion loss with a cable assembly of 0.5 m between TP1 and TP4 is determined using Equation (85A-4) where f is expressed in MHz.

$$IL_{Ch}(f) \le IL_{Chmax}(f) = 0.05 \times IL_{Camax}(f) + IL_{PCBmax}(f) \text{ dB} \qquad (85A\text{-}4)$$

for 50 MHz $\le f \le$ 5156.25 MHz.

where

$IL_{PCBmax}(f)$ The sum of the transmit PCB loss and the receive PCB loss.

$IL_{Camax}(f)$ The maximum cable assembly insertion loss determined using Equation (85–51).

CR4-10 PCB loss (draft 2.1)

85A.4 Transmiter and receiver differential printed circuit board trace loss

The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5) are determined using Equation (85A-1) where f is expressed in Hz and the coefficients b_1 through b_4 are given below.

$$IL_{PCB}(f) \le IL_{PCBmax}(f) = (0.2032) \times [20 \times \log_{10}(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3)] \text{ dB} \qquad (85A\text{-}1)$$

for 50 MHz $\le f \le$ 6000 MHz.

where

b_1	2×10^{-5}
b_2	1.1×10^{-10}
b_3	3.2×10^{-20}
b_4	-1.2×10^{-30}
e	≈ 2.71828

4.74dB max loss
Specified for total of
TP0-TP1 and TP4-TP5
(2.37dB TP0-TP1 or TP4-TP5
If split evenly)

The minimum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the maximum insertion loss between TP0-TP1 and TP4-TP5) are determined using Equation (85A-2) where f is expressed in Hz and the coefficients b_1 through b_4 are given below.

$$IL_{PCB}(f) \le IL_{PCBmin}(f) = (0.103) \times [20 \times \log_{10}(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3)] \text{ dB} \qquad (85A\text{-}2)$$

for 50 MHz $\le f \le$ 6000 MHz.

where

b_1	2×10^{-5}
b_2	1.1×10^{-10}
b_3	3.2×10^{-20}
b_4	-1.2×10^{-30}
e	≈ 2.71828

2.4dB min loss
Specified for total of
TP0-TP1 and TP4-TP5
(1.2dB TP0-TP1 or TP4-TP5
If split evenly)

CR4-10 cable assembly

85.10.2 Cable assembly insertion loss

The insertion loss of each pair of the 40GBASE-CR4 and 100GBASE-CR10 cable assembly shall meet the values determined using Equation (85–40) where f is expressed in MHz.

$$ILca(f) \le ILcamax\ (f) = ((0.192749 \times \sqrt{f}) + (0.001494 \times f)) \text{ dB} \qquad (85\text{–}40)$$

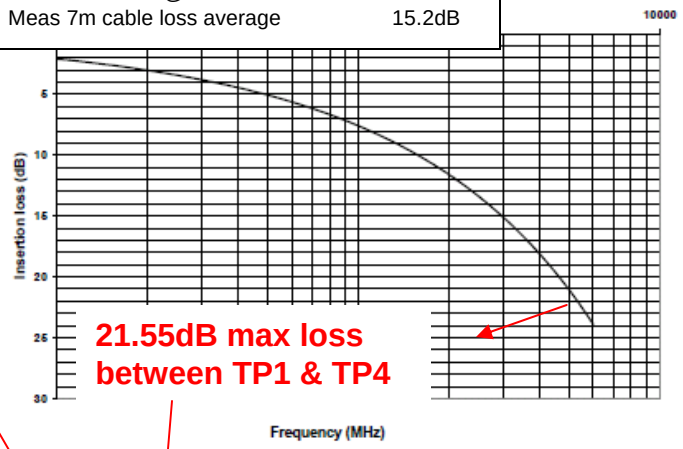
for 50 MHz $\le f \le$ 6000 MHz. This includes the insertion loss of the differential cabling pairs and the assembly connectors.

where

$IL_{ca}(f)$	The cable assembly insertion loss.
$IL_{Camax}(f)$	The maximum cable assembly insertion loss.

The maximum cable assembly insertion loss is illustrated in Figure 85–4.

Cable loss dB/m	2
Total cable loss @ 10m	21
Meas 7m cable loss average	15.2dB



21.55dB max loss
between TP1 & TP4

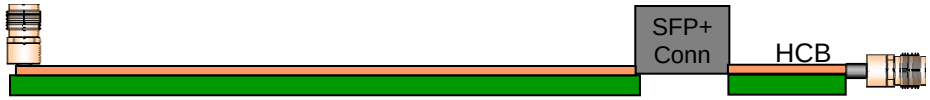
Max channel loss = 26.3dB

CR4/10 Measured PCB loss

- With FR4-6 material (or equivalent), Cisco estimates a PCB loss of around 0.8dB/inch, as measured over Cisco Ref card (CRC, for SFP+ testing)

- Lead-free materials further limits the PCB material choices

CRC S-Param	Total Loss	Connector + HCB loss	PCB loss	Loss/Inch
Measured 8"	6.93	1.04	5.89	0.74
Measured 6"	5.68	1.04	4.64	0.77
Measured 4"	3.85	1.04	2.81	0.70
Measured 2"	2.44	1.04	1.40	0.70
Measured Cal 8"			6.44	0.81
Measured Cal 2"			1.4	0.70



CRC channel

Cal channel

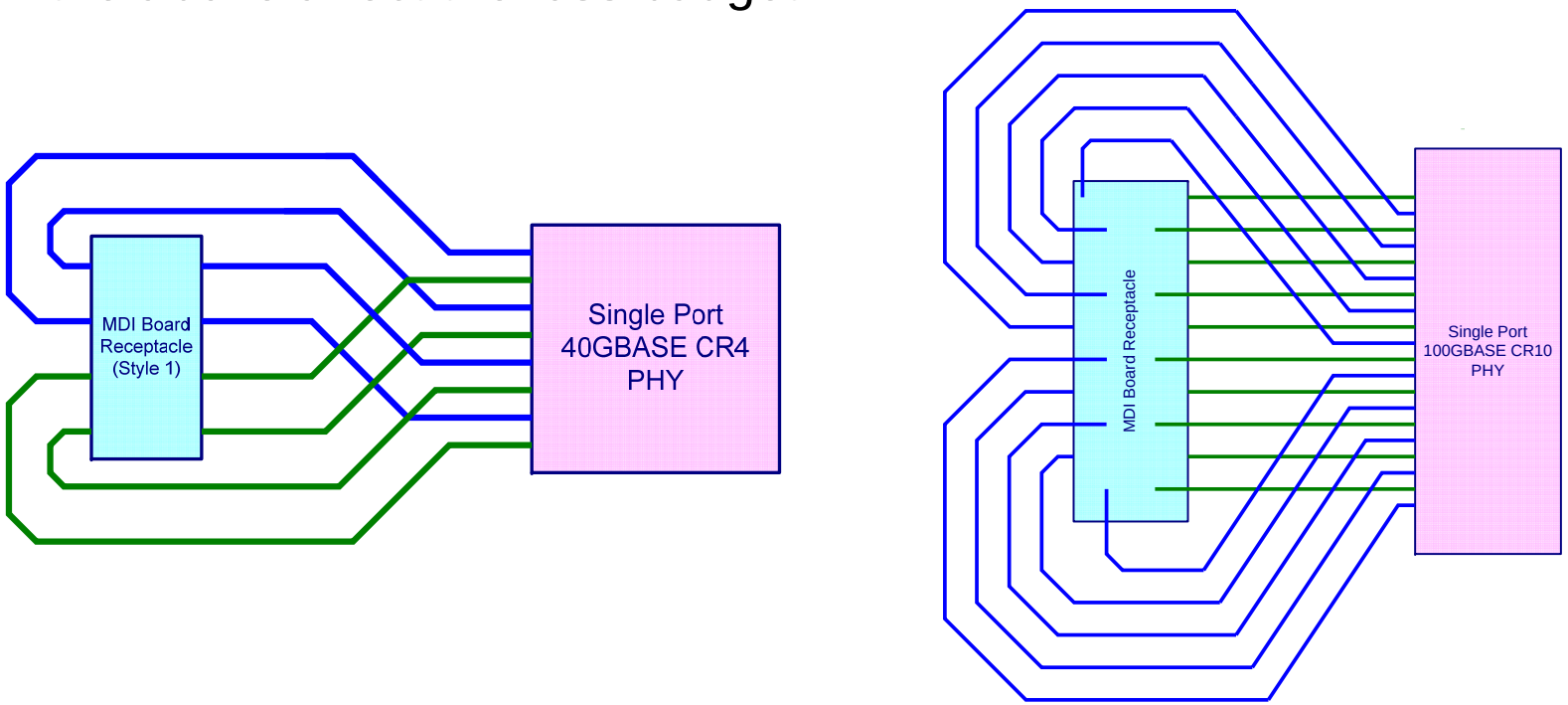
- **Current 802.3ba draft 2.1 limits PCB designs to be from 1.5” minimum to 3” maximum, with FR4-6 material or equivalent: this is not in line with the 8” (4” per side) requirement in 85A.4.**

- Note: CRC uses 4.25 mil traces, 8.5 mil spacing, DK = 3.8

Channel Layout Example

- Taking into account future multi-port designs:
  - PCB impedance variation (+/-10%),
  - Routing layer used (this leads to stubs),
  - Connector pin field design
  - Reflections/resonances between individual components
  - Many discrete components are not shown these constrain the PHY placements

All the above affect the loss budget



Proposal is to allocate a total of 5dB max loss for PCB and Host connector (3.5dB for PCB, 0.87dB for connector, 0.63dB for other impairments).

Budget Tradeoffs

To allocate this budget, a trade off between CR4/10 cable and PCB loss can be considered.

We do not foresee a significant reduction of copper connections by moving the target maximum CR4/CR10 cable distance from 10 to 7m.
(the same feedback was already given to the SFF-8431 working group to define maximum direct attach cable length).

If this can be applied to CR4/10 802.3ba, then a 7m cable would allow such PCB loss to keep the same max channel loss.

Considering a cable assembly loss reduction of 6dB from 10 to 7m (2dB/m), then this loss would become:

21.55dB – (3*2dB) = 15.55dB → assuming 16.3dB

Max channel loss (10m) = 26.3dB in the draft 2.1

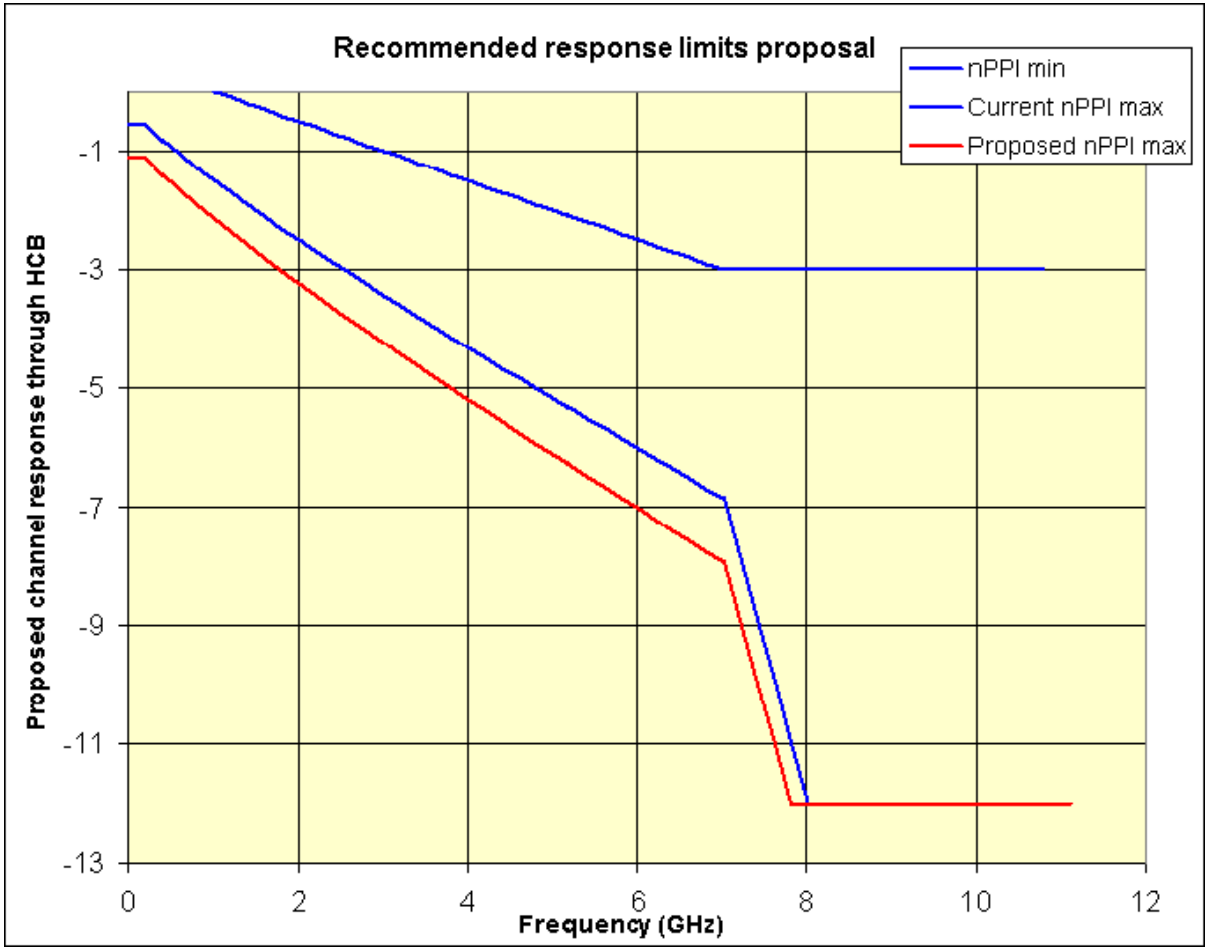
Proposed would give Max channel loss (7m) = 16.3 + 5*2 = 26.3dB

Annex 86A

- Eq 86A-20 specifies the maximum insertion loss for the Parallel Physical Interface's channel (PCB) and the HCB, between the PMA IC (TP0 or TP5) and TP1 or TP4
  - Observation: 5.3dB
- Page 424 Line 36: The recommended maximum loss of the host channel (PCB only) at 5.15625 GHz is 3.5 dB.
  - Observation: 5.3dB – 3.5dB = 1.8dB for HCB + connector
- Equation 83A-7 specifies 1.26dB for HCB trace only
  - Observation: 1.8dB – 1.26 dB = 0.54dB for connector only
    - Cisco connector measurement: 1.04dB
- However, specifications for HCB, MCB, and mated HCB/ MCB :
  - HCB: 1.26dB nominal
  - MCB: 0.67dB
  - Mated HCB / MCB: 2 to 2.8dB
  - Connector loss and deviations from nominal = 2.8 – 1.26 – 0.67 = 0.87dB
  - For comparison, SFP+ connector loss max 0.58 dB

- Proposal is to allocate a total of 5dB max loss for PCB and Host connector (3.5dB for PCB, 0.87dB for connector, 0.63dB for other impairments).
  - Eq 86A-20 will need to be revisited to use 0.87dB (increase of 0.33dB for connector) and 0.63dB for other impairments.
  - Eq 86A-20 should reflect 3.5dB (Host trace) + 0.87dB (connector) + 1.26dB (HCB trace) + 0.63dB (impairments) = 6.26dB at 5.15625 GHz

Proposed 86A Channel



86A.6 Recommended electrical channel

A recommended maximum attenuation template for the Parallel Physical Interface's channel (PCB) and the HCB, between the PMA IC (TP0 or TP5) and TP1 or TP4, is illustrated in Figure 86A–11, along with a recommended minimum attenuation intended to control the effect of reflections. It is recommended that

$$
\begin{aligned}
20\times\log_{10}(|SDD21|) \;&\geq -1.11 && 0.01 \leq f \leq 0.2 \\
&\geq -0.6029 - 0.8097\times\sqrt{f} - 0.7397\times f && 0.2 \leq f \leq 7 \\
&\geq 28.31 - 5.16\times f && 7 \leq f \leq 7.81 \\
&\geq -12 && 7.81 \leq f \leq 11.1
\end{aligned}
\qquad (86A\text{–}20)
$$

SR4/10 Loss

- We want to have compatible PCB trace requirements for the non-retimed optical interface application, so use the related values in 85A.4 (Transmitter and receiver differential printed circuit board trace loss) and 86A.6 (Recommended electrical channel for Parallel Physical interface).
- This will enable a single host design that is able to drive CR4 and SR4 in small form factors for high density port switches. We believe current PPI host electrical output specifications at TP1a can be met for a maximum PCB + connector loss of 5dB.

	SFF-8431	IEEE 802.3ba	SFF-8431 Cisco measuments at B (equivalent to TP1a): 5" CRC (around 5dB total loss)		
Parameter	**TX host B requirements (= TP1a)**	**Values into Draft 2.1 Table 86a for nPPI**	130nm structure TX host Phy	90nm structure TX host Phy	65nm structure TX host Phy
Common-mode AC output voltage (max.)	15mV rms	15mV rms	6mV rms	6.7mV rms	6.3mV rms
J2 jitter output	n.s.	0.18	n.m.	n.m.	n.m.
J9 jitter output	n.s.	0.26	n.m.	n.m.	n.m.
DJ (Dual-Dirac PRBS9 @1E-12)	n.s.	n.s.	0.11 UI	0.105 UI	0.12 UI
DDJ (PRBS9)	0.1 UI	n.s.	0.087 UI	0.079 UI	0.085 UI
DDPWS (PRBS9)	0.055 UI	0.07 UI	0.047 UI	0.043 UI	0.049 UI
DCD	n.s.	n.s.	0.006 UI	0.003 UI	0.007 UI
Total Jitter	0.28 UI	n.s.	0.23 UI	0.22 UI	0.23 UI
Uncorrelated Jitter	0.0023 UI	n.s.	0.0012 UI	0.0011 UI	0.0013 UI
QSQ	50 V/V	45 V/V	> 50	> 50	> 50
Eye Mask coordinates: X1, X2, Y1, Y2 (Hit ratio 5x10-5)	0.11, 0.31 UI / 95, 350 mV	0.12, 0.33 UI / 95, 350 mV	Compliant to SFF-8431 eye mask	Compliant to SFF-8431 eye mask	Compliant to SFF-8431 eye mask

Above are reported some SFF-8431 compliance measurements over 5” CRC (total PCB + host connector loss of ~5dB). These values are achieved considering different TX host drivers of different vendors and gate structures. Highlighted in green are the common SFF-8431 802.3ba parameters. This is what industry can produce now in terms of TX host drivers. Proposal for modifications is 6.26dB.

Summary

- We believe that the CR4/CR10 PCB loss allowances are not sufficient for future PCB board designs
  - PCB trace budgets for non-retimed optical interface applications and copper applications should be equivalent
  - Additional loss needed for trace lengths supporting integrated multi-port designs

- Proposed Changes
  - Change the reach objective for CR4/10 to 7m (from 10m) to allow for more loss to be assigned to the PCB, keeping constant the channel loss budget (26.3dB)
  - Change clause 85A.4 from 4.74dB total loss for tx / rx host boards to 5dB per side for the PCB + connector + impairments budget
  - Change clause 86A.6 to 5dB per side for the PCB + connector + impairments. Note that this is a change in a recommendation since the PCB budget is a recommendation, and this channel is jitter limited.
  - Change Eq 86A-20 to reflect 3.5dB (Host trace) + 0.87dB (connector) + 1.26dB (HCB trace) + 0.63dB (impairments) = 6.26dB at 5.15625 GHZ