# Bit Matrix Implementation for 40GE and 100GE Block Muxing

Zeng Li, Min Ye, and WB Jiang

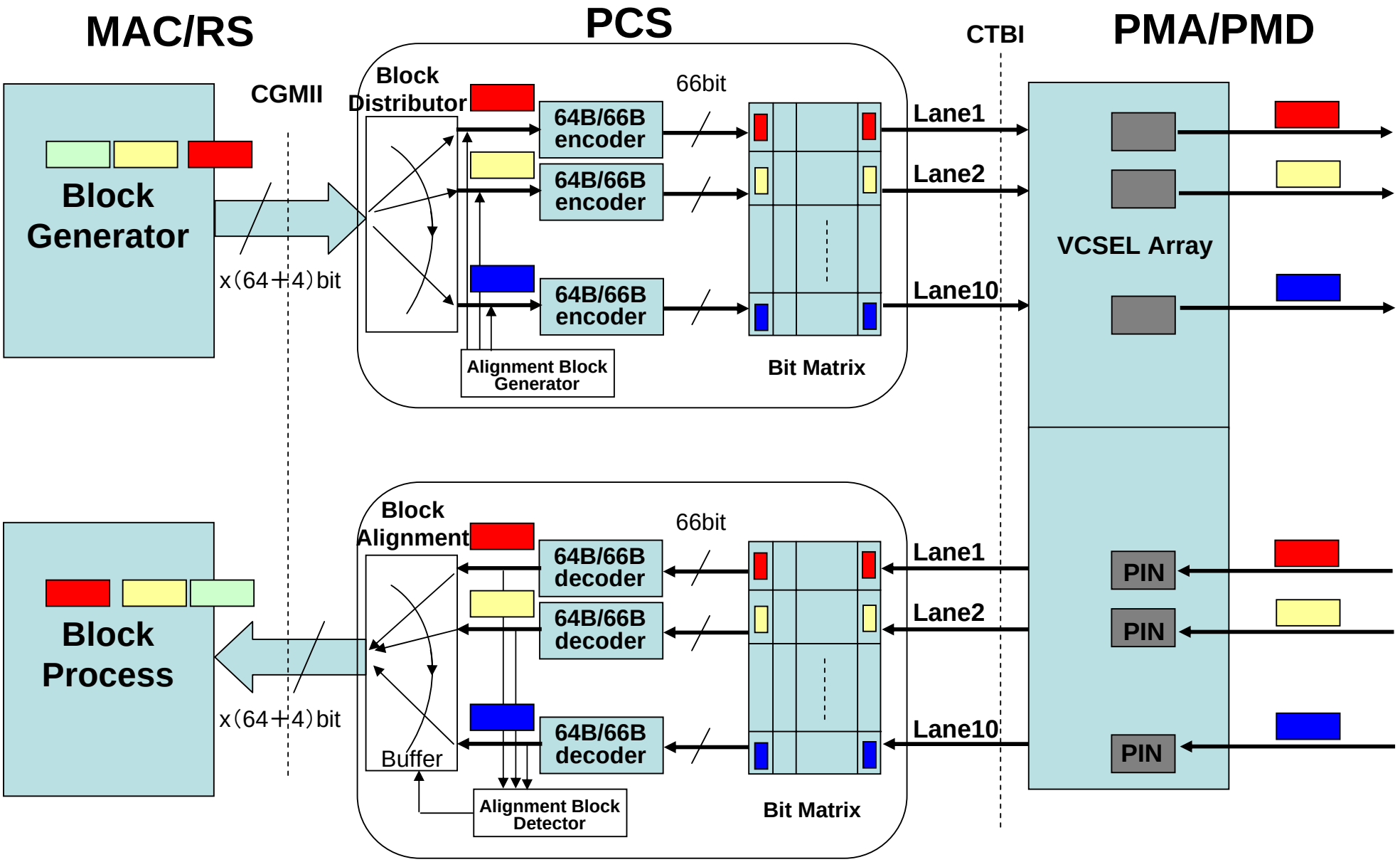
HUAWEI TECHNOLOGIES Co., Ltd.

IEEE 802.3ba Task Force, 2008

# Outline

- **High Speed Ethernet (40GE and 100GE) PBL Model**
- **Bit Matrix Implementation for PBL**
- **PBL Applications with Bit Matrix**

# PBL Model Overview



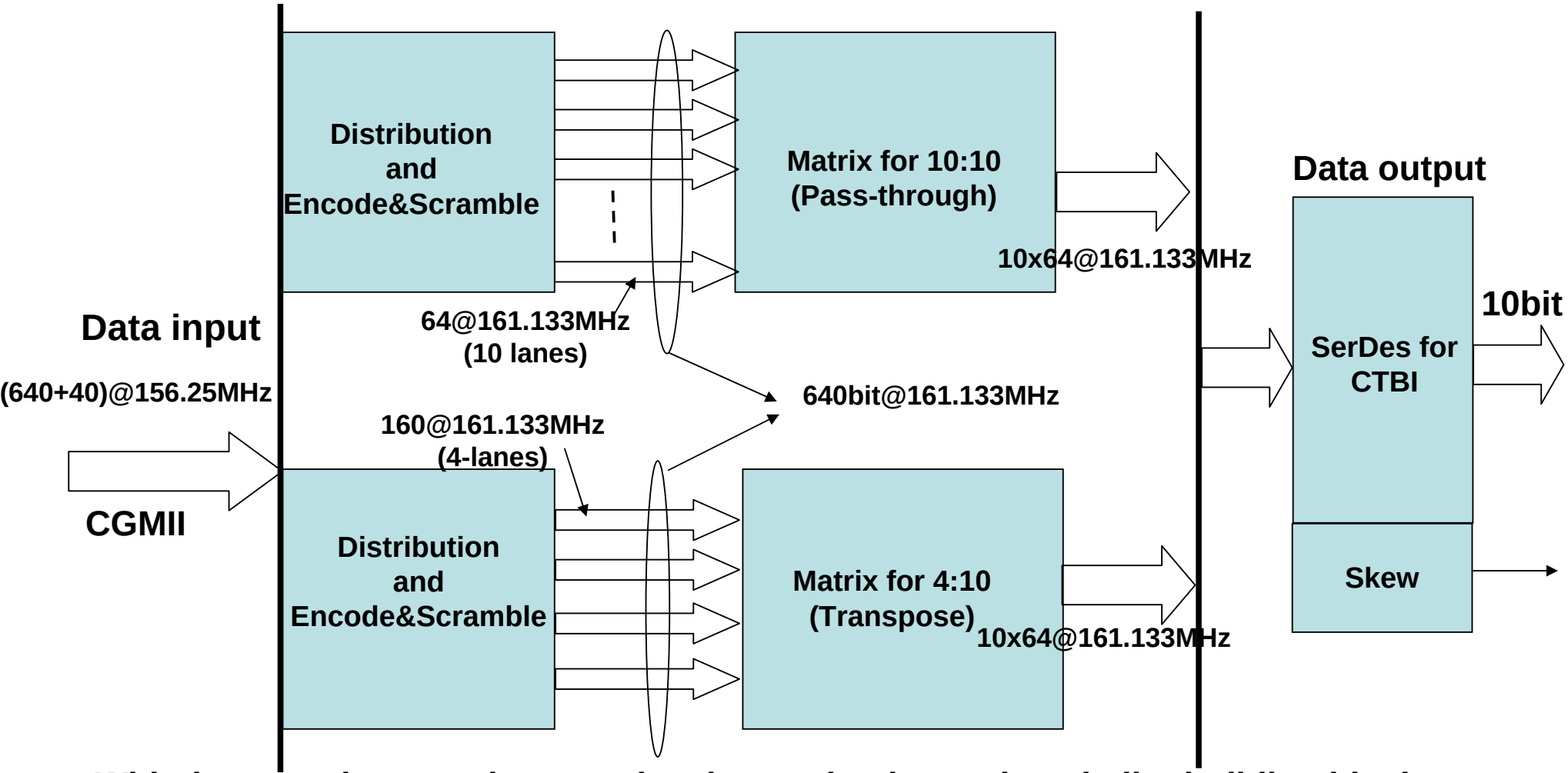
# PBL Model Overview

- Receive data from MAC layer and generate 64bit Blocks
- Transmit the Blocks through CGMII bus
- Distribute to multi-lanes based on Blocks with alignment words inserted to each lane following the distributor
- Encode the Blocks within each lane (64B/66B encoding & scrambling)
- Bit matrix will adapt CTBI to different physical lanes
- Keep Block format in every physical Lane (Block interleave to the Multi-lanes)

# Bit Matrix Introduction

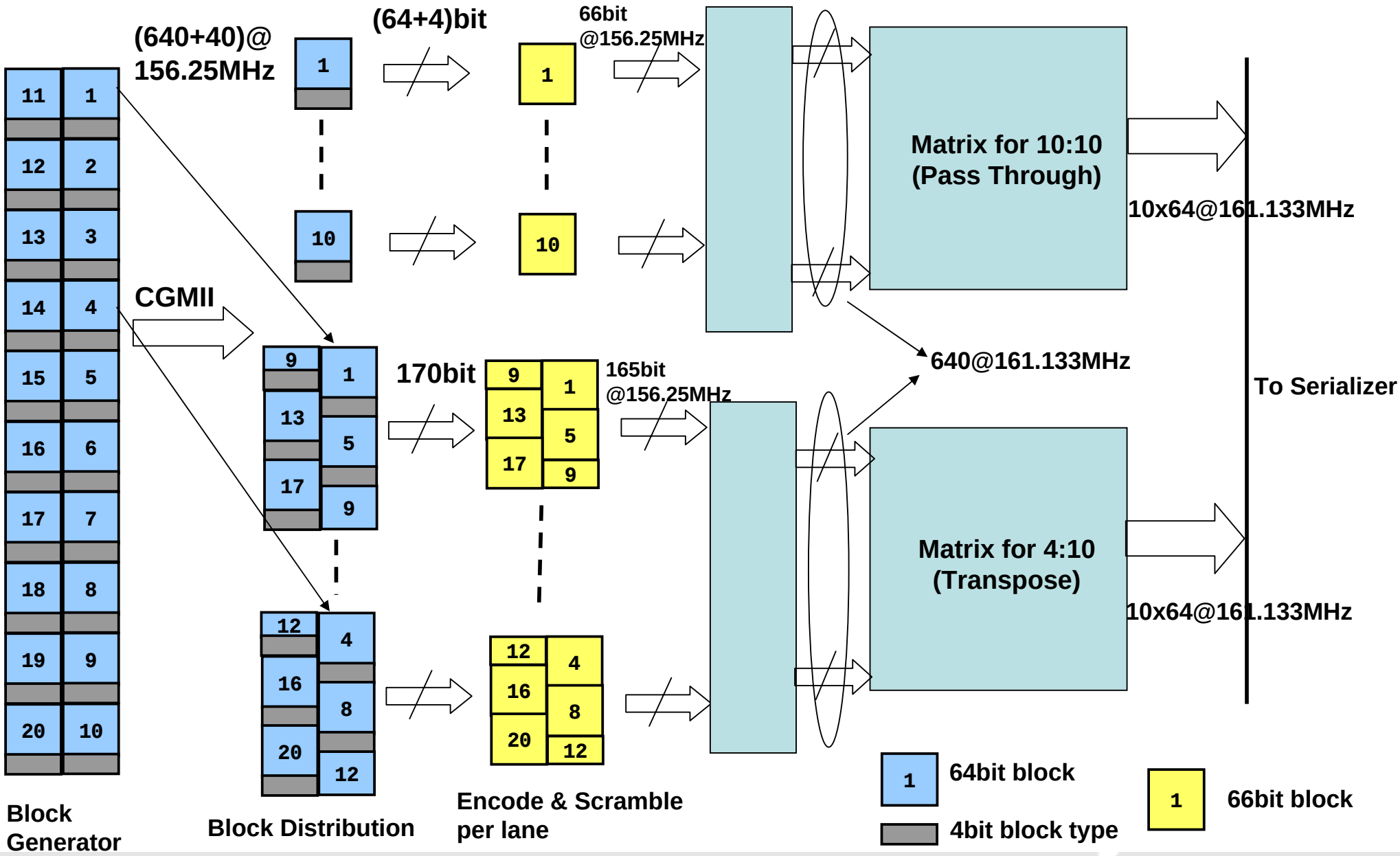
- **Bit Matrix is used for keeping Blocks running in PHY lanes**
- **Bit Matrix has two modes:**
  - Pass-through
  - Transpose
- **Bit Matrix can be implemented with Memory**

# Bit Matrix Implementations – Two Modes

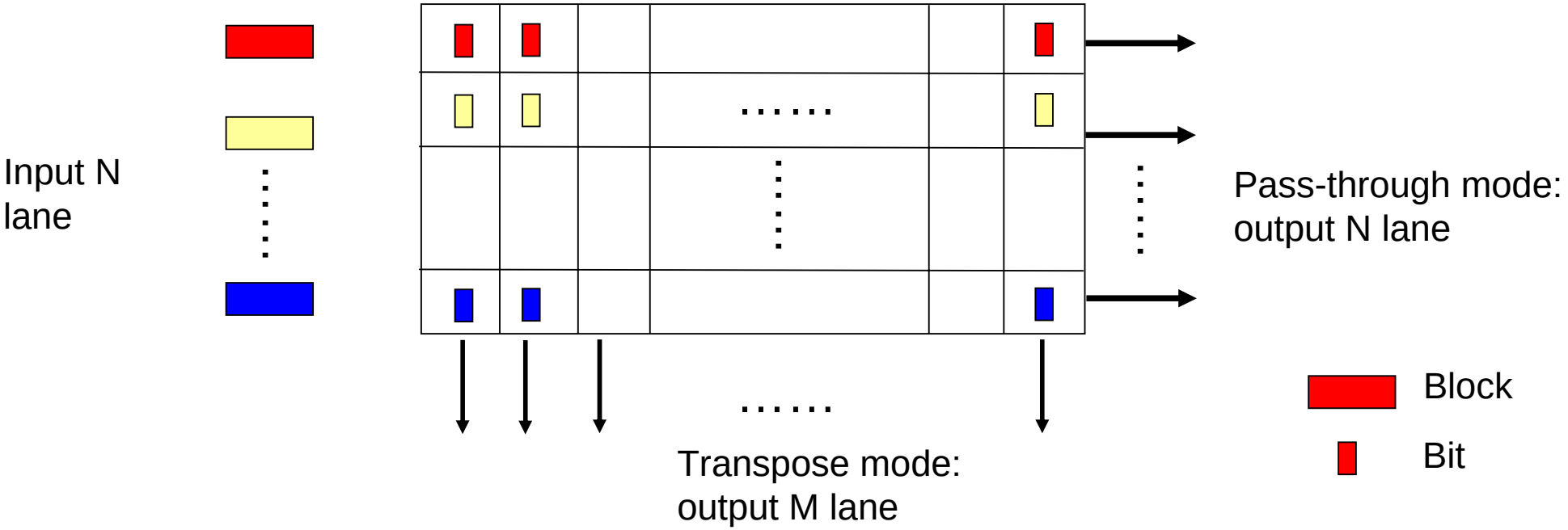



- With the same input and output data buses, implementing similar building blocks may share development resource for lower R&D cost
- Bit matrix is a configurable memory to support either a 10x10 or a 4x10 optical module.

# Bit Matrix Implementations – Two Modes



# Bit Matrix Details

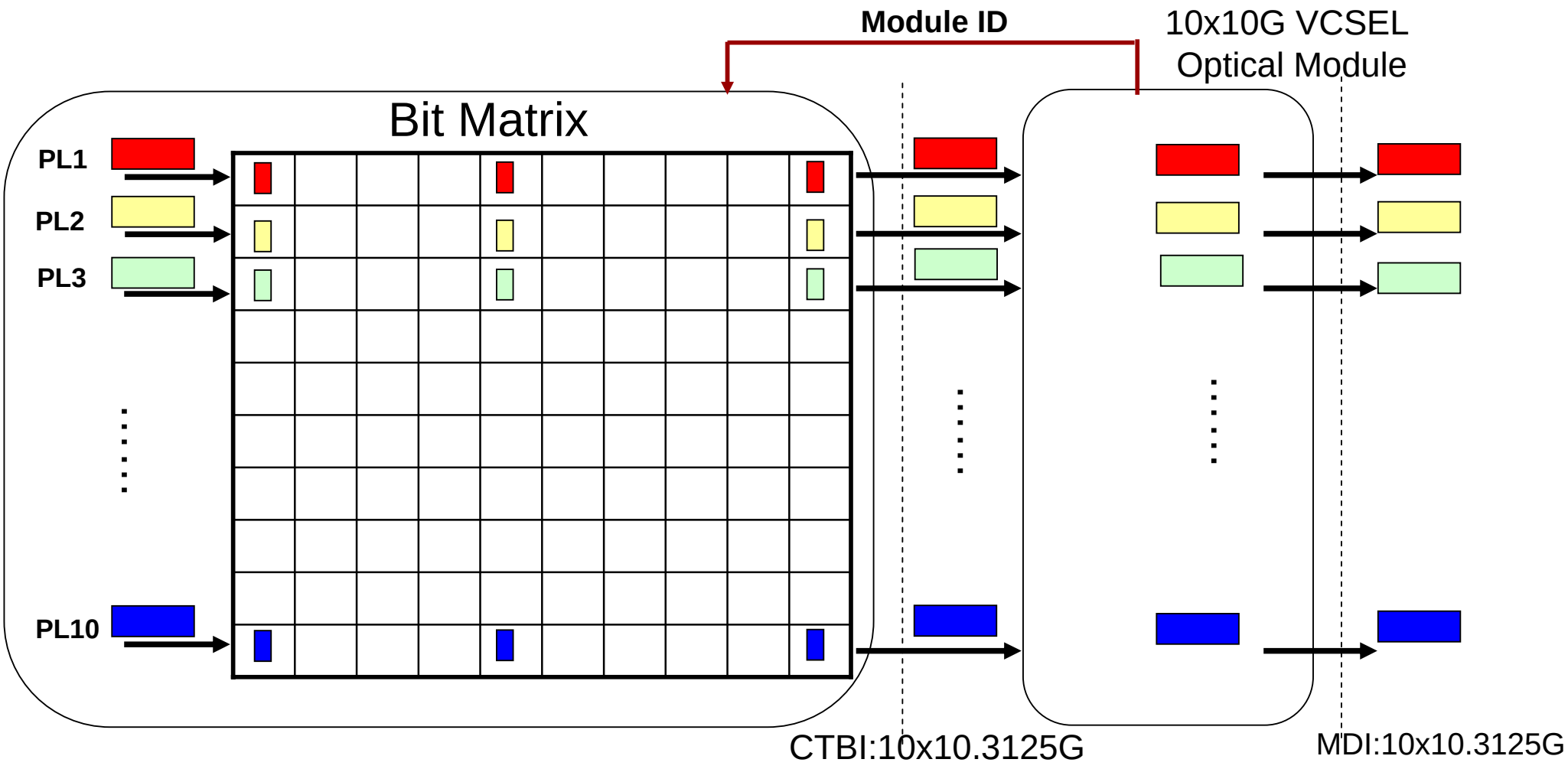



**•Bit Matrix is a (n x m) memory, n is the # of distributed physical lanes (optical module channel count); m is the # of CTBI signal (m=10)**

**•When connected to a 10x10G optical module, 10-lane data will pass through bit by bit, and physical lanes keep block running in order**

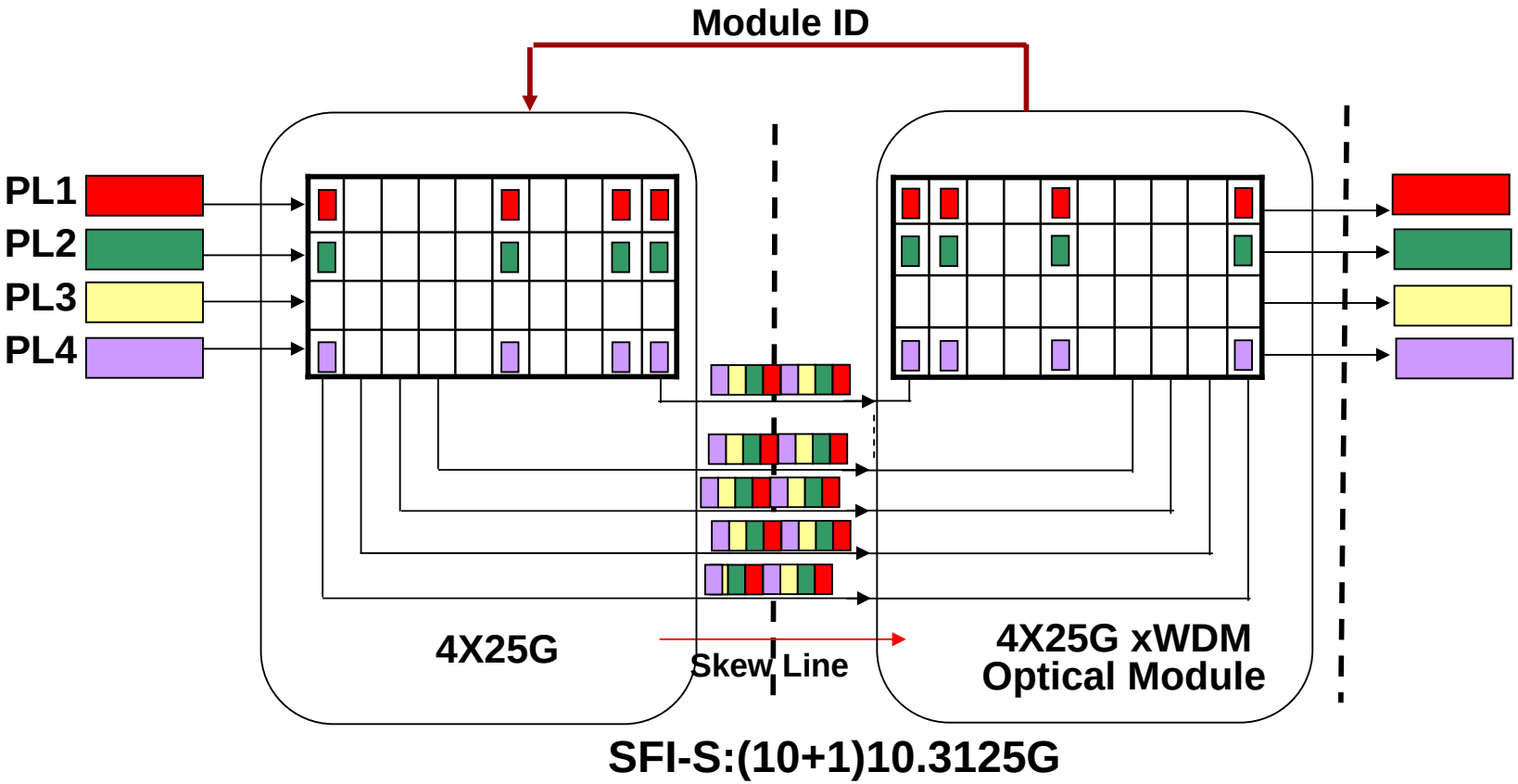
**•When connected to a 4x25G optical module, 4-lane data will be transposed to adapt to the 10bit CTBI interface. In the optical module, anti-transpose matrix will recover the blocks for running in each physical lane.**

# Bit Matrix Pass-through (10:10) Mode



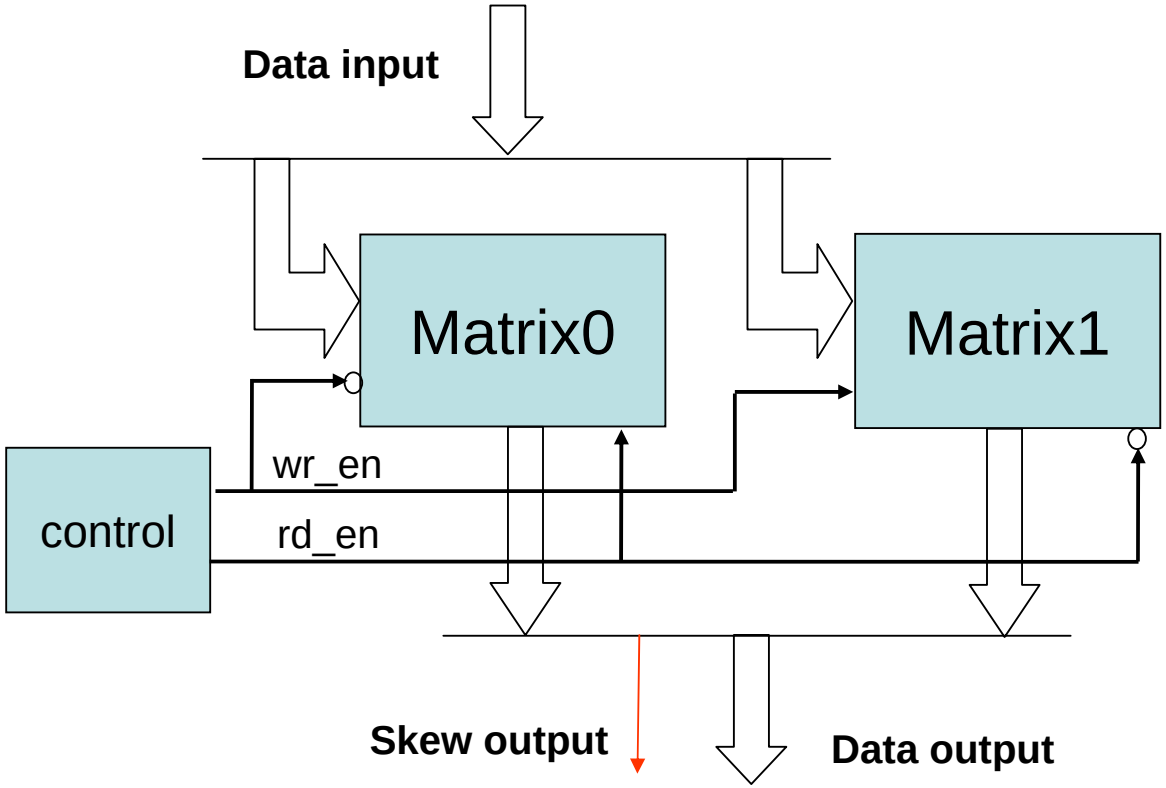

- **Optical module ID instructs PCS to configure the pass-through mode**
- **10x10 bit matrix will be deployed**
- **It will adapt to CTBI and keep block running in all 10 lanes (Block muxing in PHY lanes)**
- **No gearbox (bit matrix) in the VCSEL optical module, skew line idle (not needed)**

# Bit Matrix Transpose (4:10) Mode



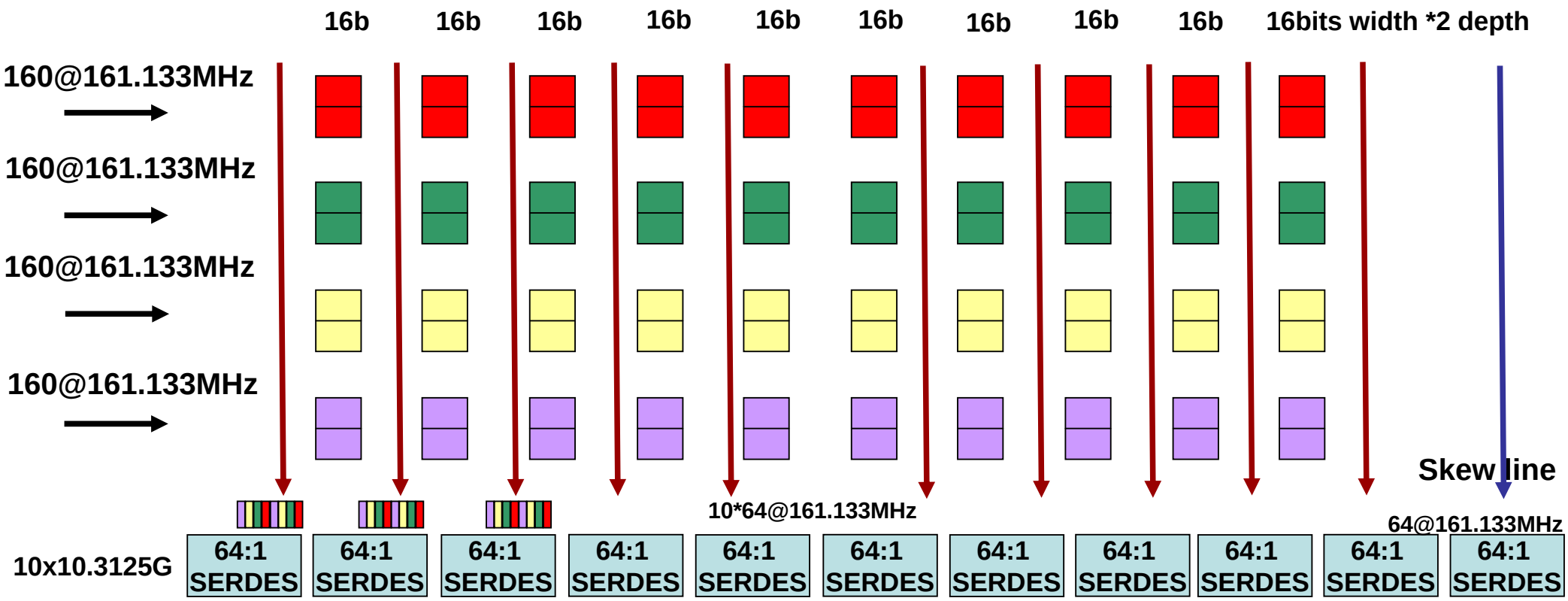

- For a 4x25G optical module, the module ID instructs PCS to configure transpose mode, adapt to 10bit electrical interface.
- Blocks are distributed to 4 Physical Lanes
- The anti-transpose Matrix (gearbox) is needed in the 4x25G optical module to recover block data (keep blocks running in all four optical lanes)

# Transpose Matrix Implementation




- **Use two matrixes with “ping-pong” operation to implement transpose function**
- **Use wr_en and rd_en to control two matrixes’ read and write**
  - When writing data into Matrix0(wr_en is available to Matrix0), data is read from Matrix1
  - When writing data into Matrix1(wr_en is available to Matrix1), data is read from Matrix0

# Transpose Matrix Implementation with Memory

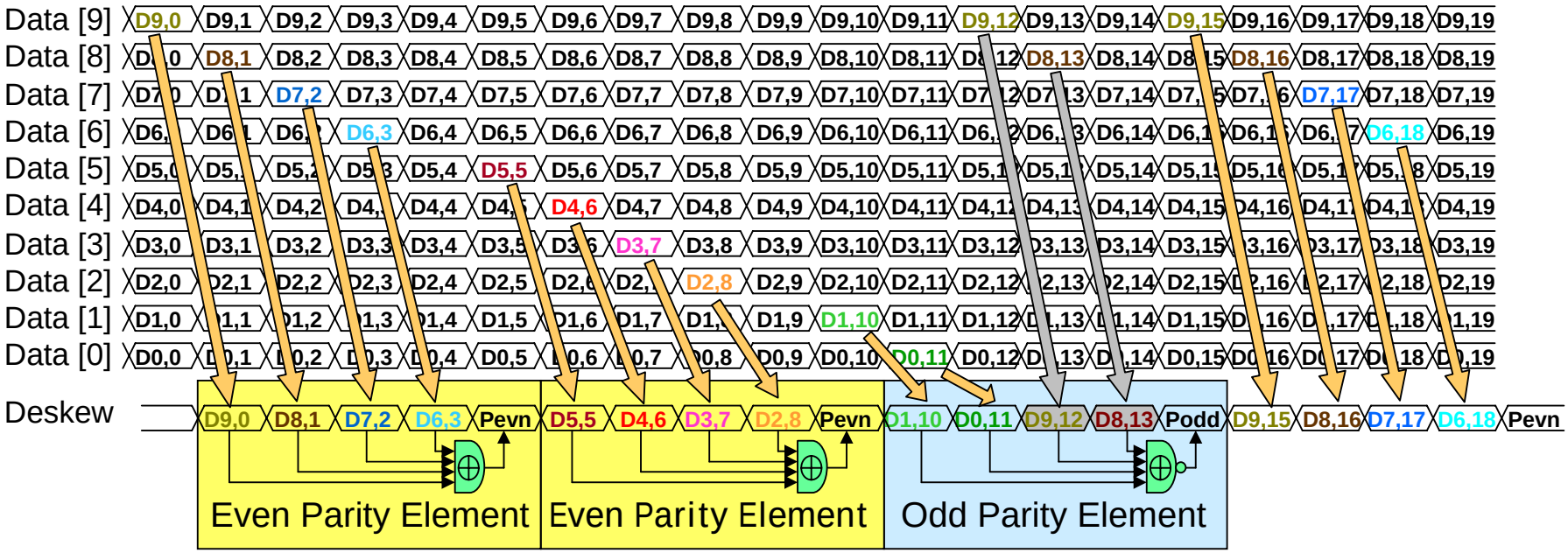



- In each lane, 160bits of data is written to 10 RAMs. Every RAM is 16-bit wide * 2-bit deep.
- Data are read by column. In each column, 64bits are read from 4 RAMs in order, and serialized by SERDES

# Transpose Matrix Implementation with Memory

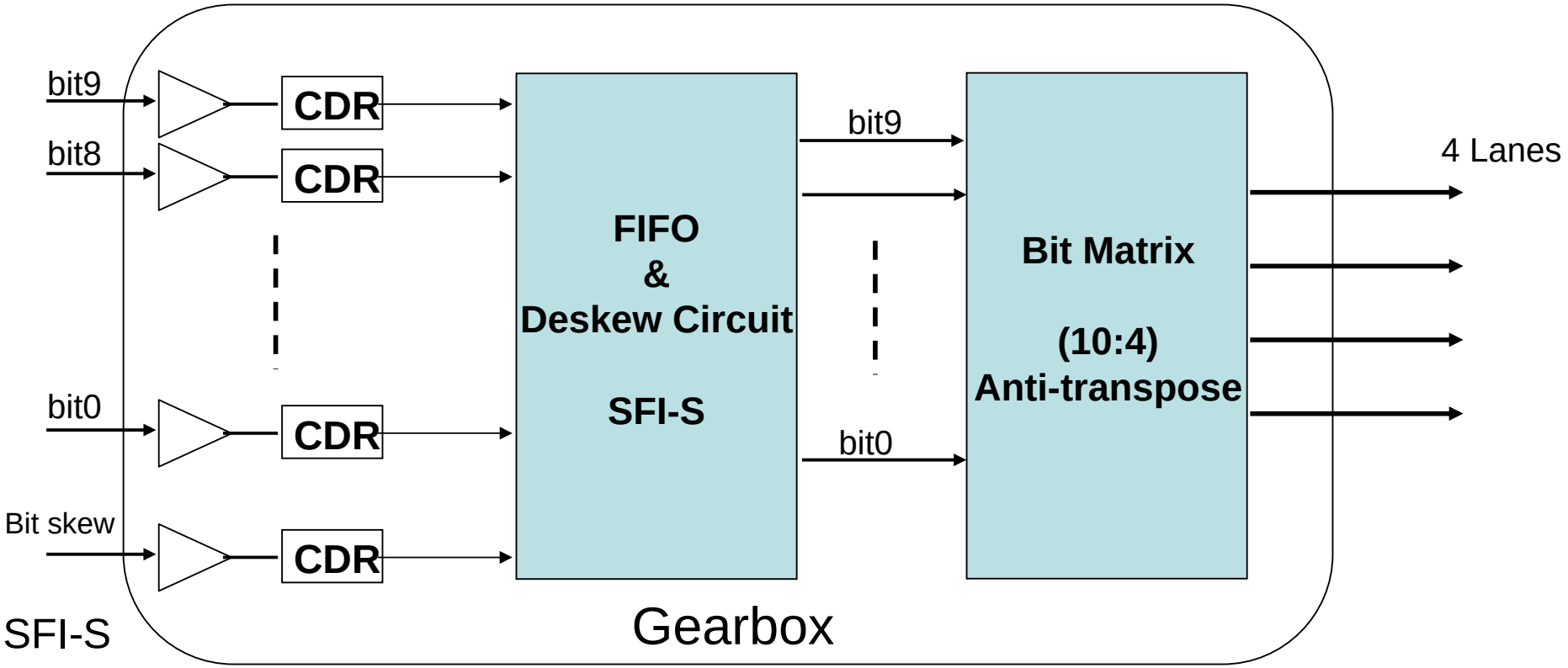
- **There are 40 RAMs in a sub-Matrix, and 80RAMs in total by “ping-pong” matrixes**
- **Skew line is introduced for bit alignment.**
- **Resource needed for the matrix (when input data is 640bits@161.133MHz)**
  - Bit Matrix RAM: 16 bits *2 *40 *2 = 2560 bits
  - Skew line generator: Logic resource implementation per even-parity element and odd-parity element – Next page

# Skew Line Implementation per SFI-S



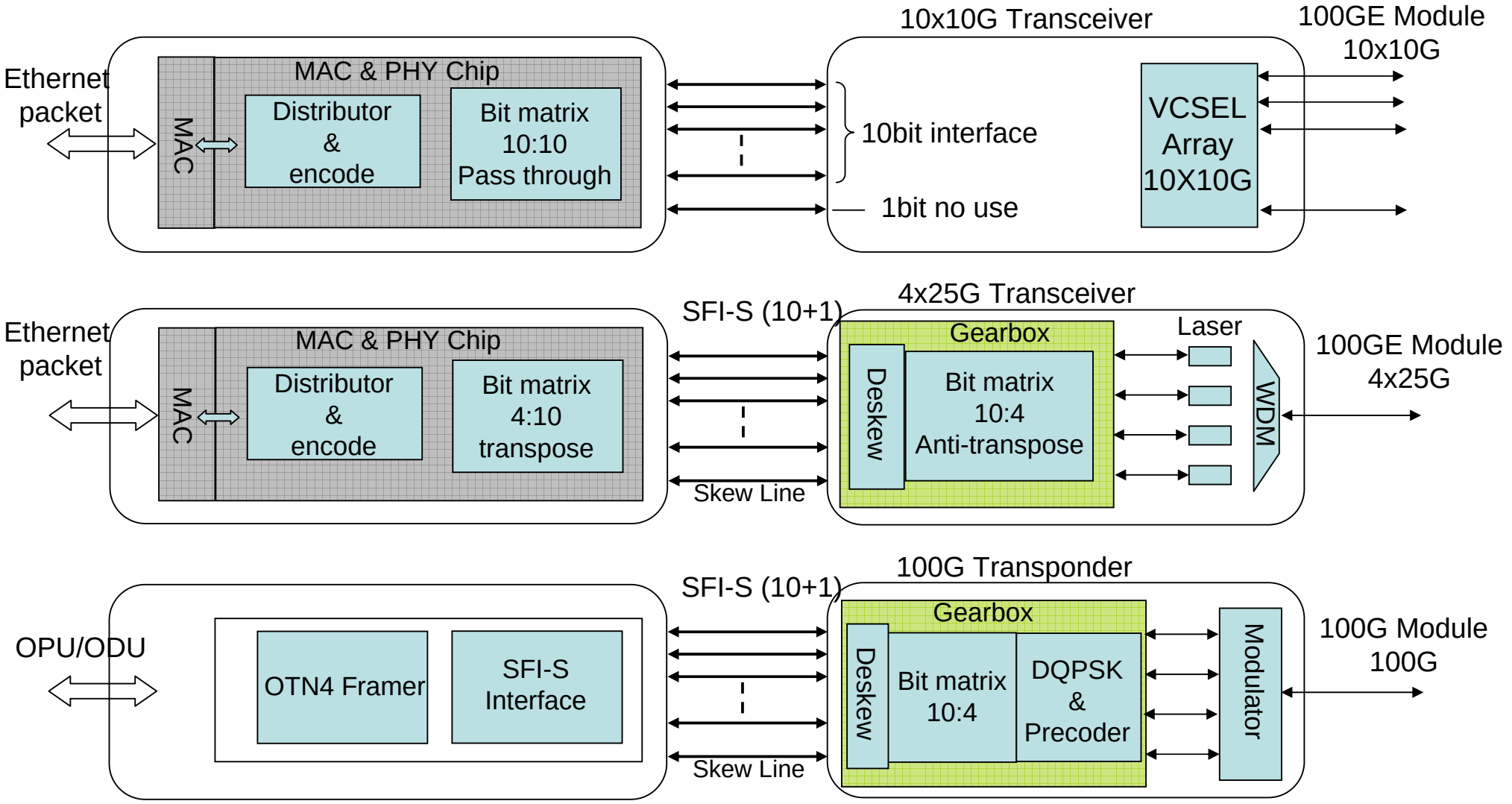

- **Skew line to keep bit alignment in the module**
- **In the optical module, anti-transpose bit matrix recovers blocks from aligned bits**
- **Skew line adopts SFI-S protocol defined by OIF (oif2007.304.01)**

# Anti-Transpose Matrix in 4x25G xWDM Optical Module




- **SFI-S-like inteterface is used as a common electrical interface for optical modules**
- **The aligned bits are recovered in blocks in the physical lanes by anti-transpose bit matrix method**
- **Implementation is the similar to the PCS, but reversing the rows and columns**
  - 2.56k memory
  - 10x10G (161.133MHz bus) Serdes with CTBI
  - 4x25G (161.133MHz bus) Serdes with 4x25G xWDM PMD

# Common Optical Module Interface for Ethernet & OTN



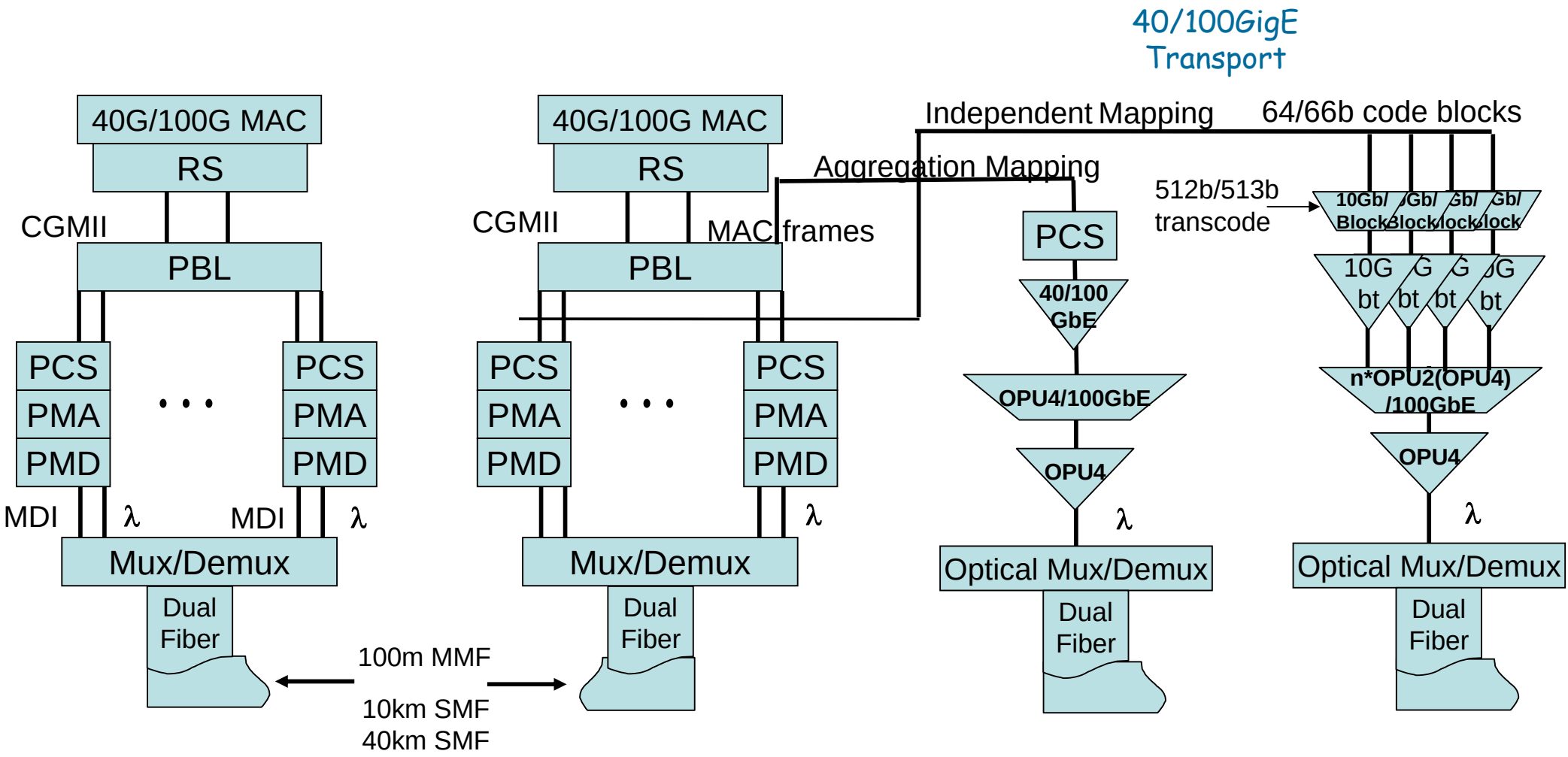

- **SFI-S is introduced as a common interface for the 100G optical module**
- **Similar chip design due to similar function blocks may be shared**

# Conclusions of Bit Matrix Method

- **Bit matrix method provides a solution to keeping data blocks running in the physical lanes**
- **Bit matrix adapts to different optical modules with the same electrical interface**
  - Support both 10x10G and 4x25G modules
  - Select operation mode (pass-through or transpose) by diagnosing module type
- **SFI-S is introduced to interface between PHY and optical modules**
  - SFI-S is defined by OIF
  - Skew line keeps the bits aligned in transpose mode
  - SFI-S allows common interfaces for both 100GE and ODU-4 optical modules

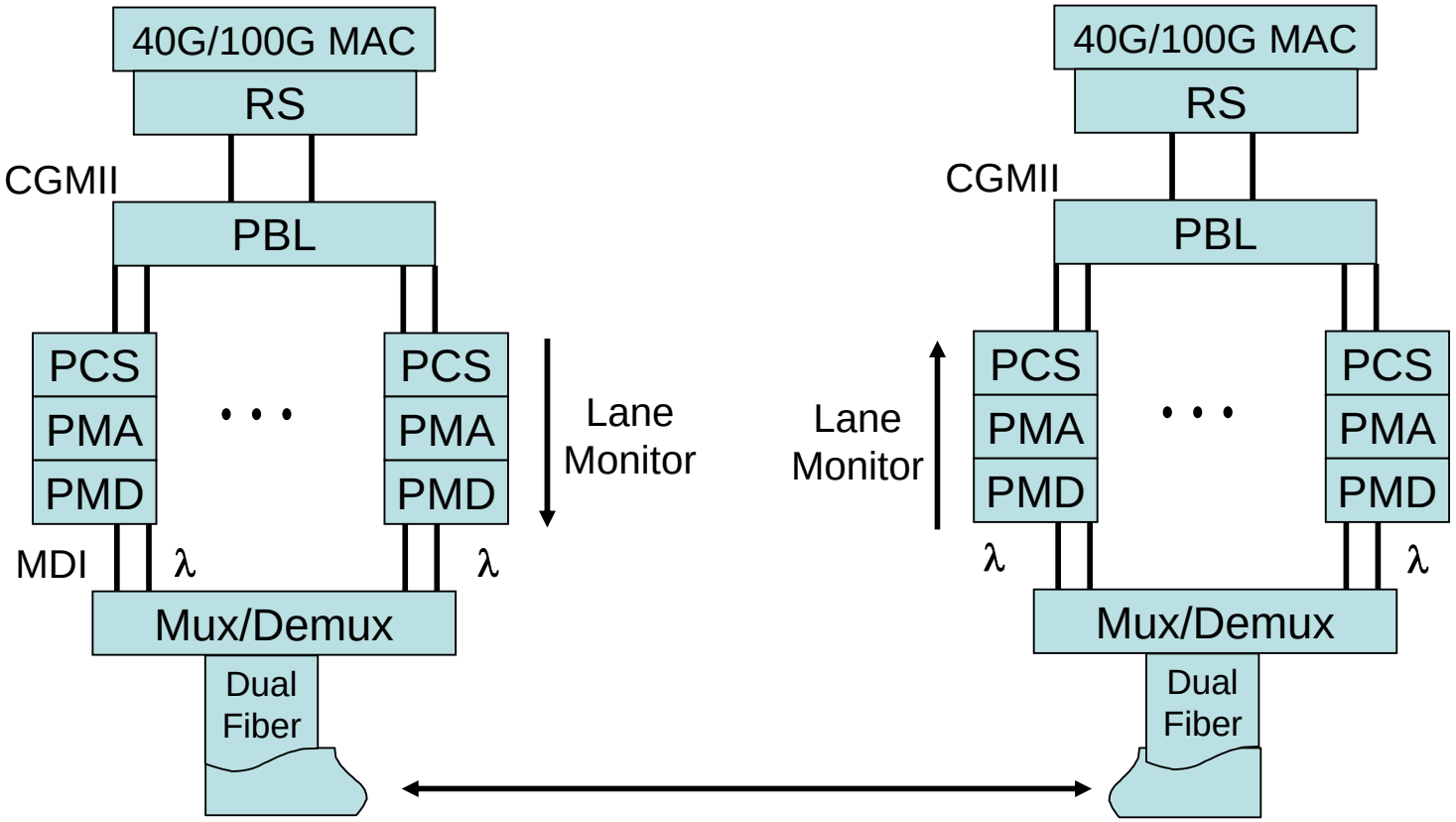
# Appendix – PBL Applications

# PBL Application– Flexible OTN Mapping



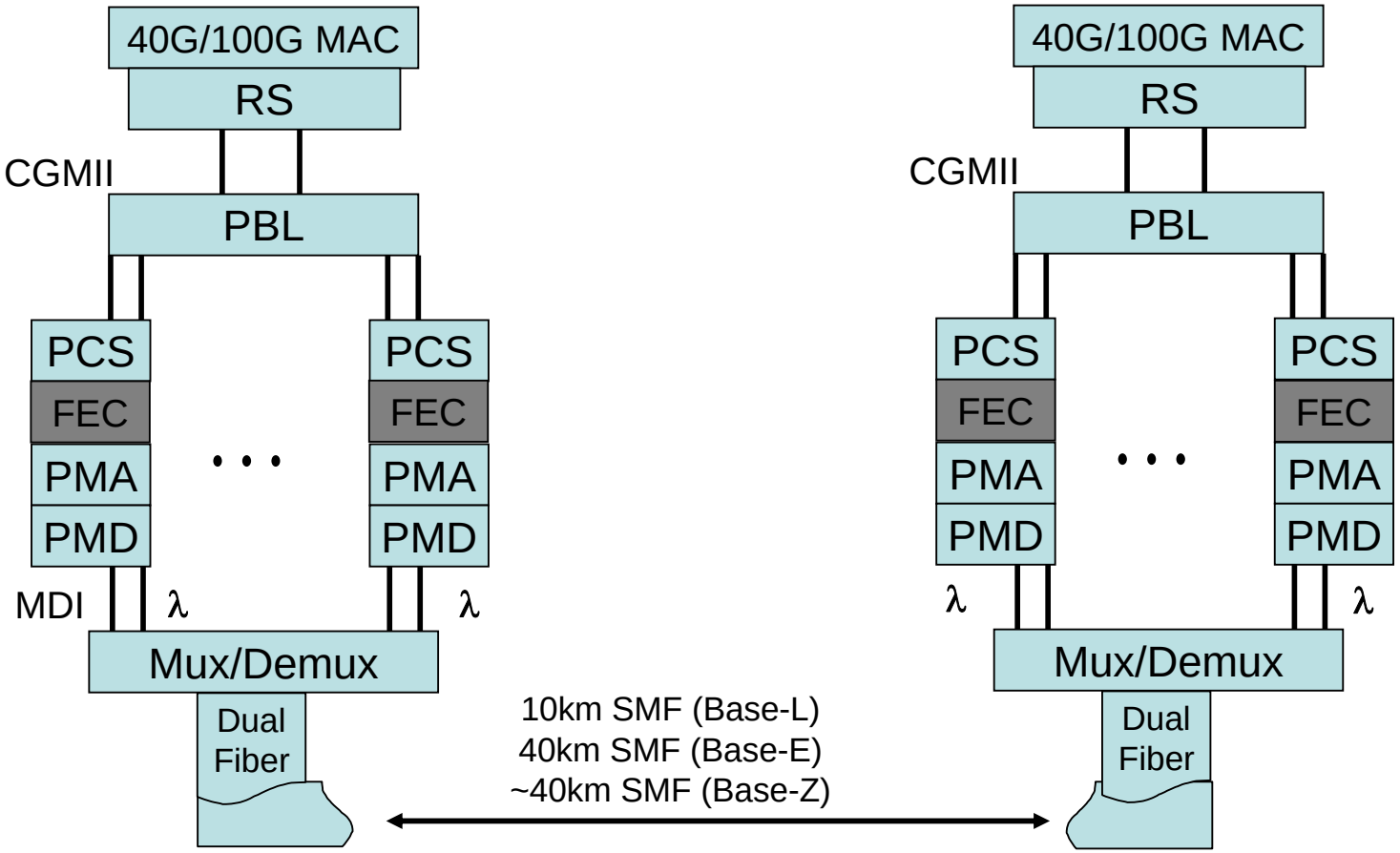

- **PBL supports both Aggregation and Independent Mapping into OTN**
- **Blocks in an independent lane allows for mapping into OTN by transcode**

# PBL Application – PHY Management




- **PBL distributes blocks to each lane (block muxing), which is similar to traditional Ethernet format good for management and maintenance**

# PBL Application – FEC Support




**•PBL distributes blocks to each lane (block muxing) and support FEC function for applications not only in backplane but also in transport over extended distances**

# PBL with Bit Matrix

- **Physical Lane Bundling (PBL) with block muxing retains tradition Ethernet technology**
  - **Beneficial to many applications**
    - **OTN mapping**
    - **PHY management**
    - **FEC**
- **PBL with Bit-Matrix**
  - **Provide a common electrical interface solution to accommodating both 10x10G and 4x25G optical modules**
  - **Allow a single 100G optical module design for both 100GE and ODU-4**

Thank You