HSE OTN Support

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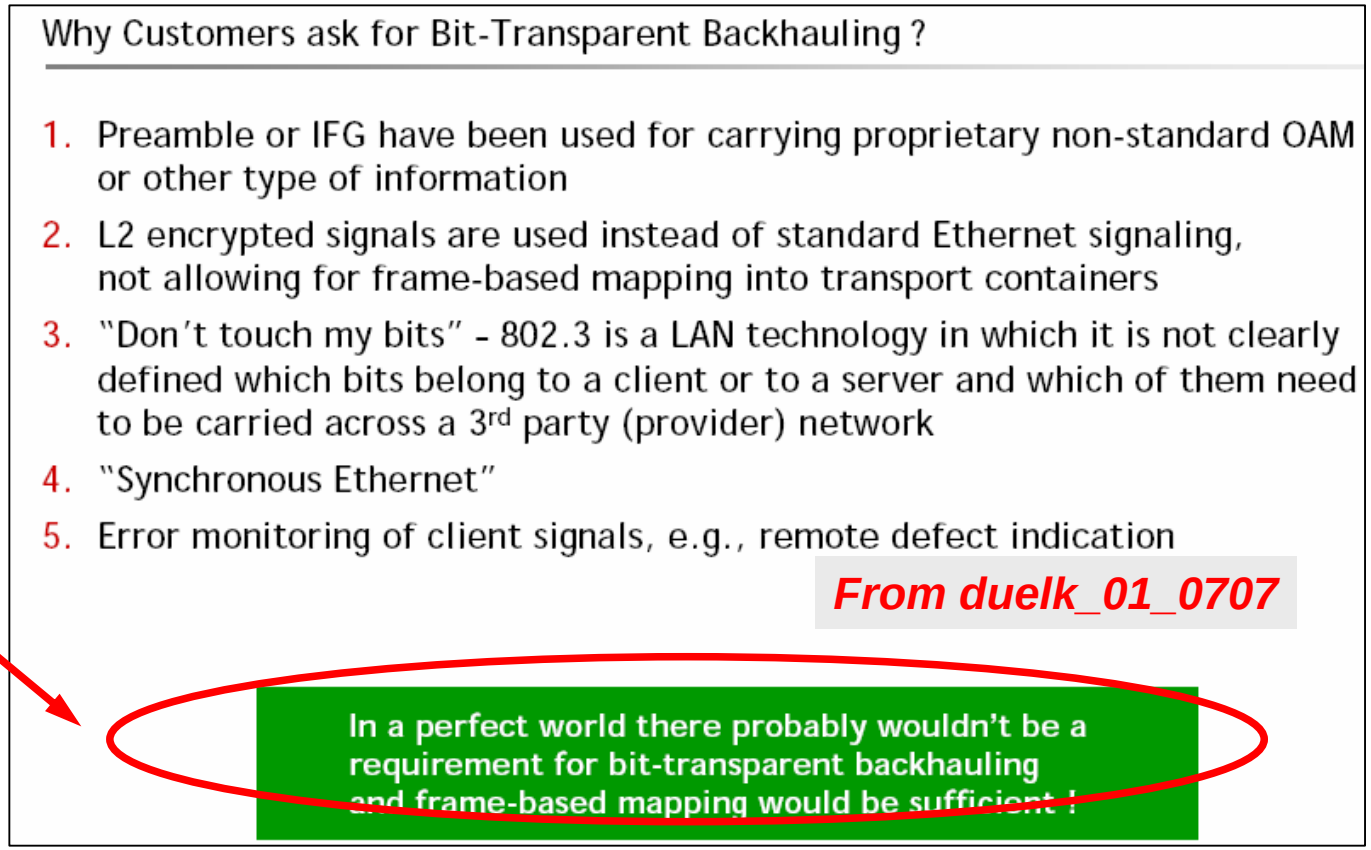
Content

- **Bit transparency requirement**
- **Skew accumulation issue**
- **Lane independent transport & 2x skew tolerance**

Transparency Requirement Addressed by duelk_01_0707

- **Ethernet service transparency options over OTN**
  - Bit transparency, PCS codeword transparency, MAC Frame transparency
- **OTN as a Service Layer should provide various levels of transparency for Ethernet over OTN, especially the Bit Transparency**

In a real world, different private applications will be required, bit transparency should be ensured both in IEEE and ITU-T



Bit Transparency Requirement for 40GE/100GE

- **Bit transparency requirement for 40GE/100GE has been discussed both in IEEE and ITU-T. ODUk-Xv or ODU4 (possible ODU3e for 40GE) will meet the Bit Transparency requirement for 40GE/100GE!**

- **Transcoding will provide PCS Codeword Transparency of 40GE over standard ODU3 right now.**

Difference between 40 GbE and 100 GbE (Provider Perspective)

40 Gigabit Ethernet

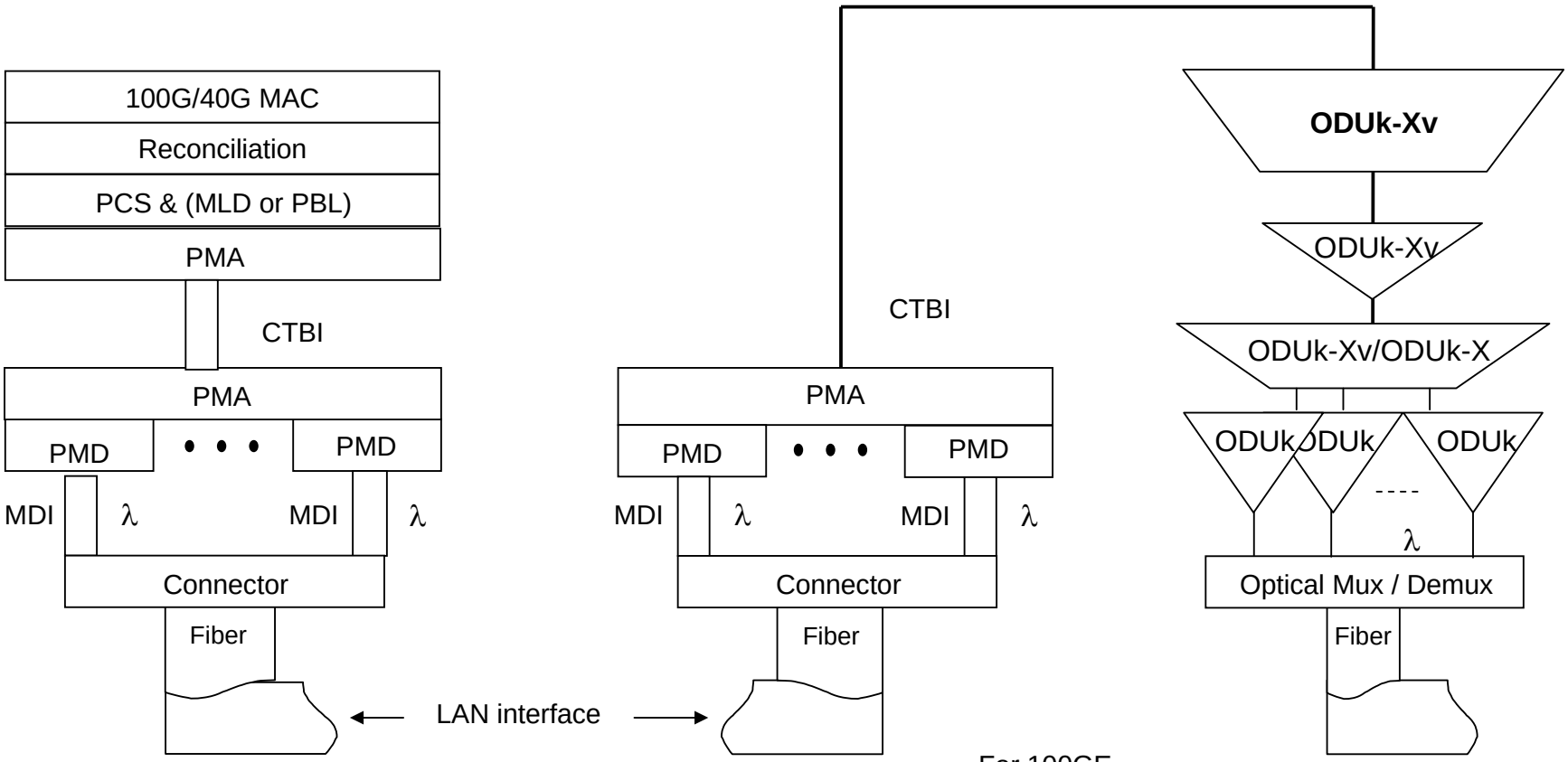
- 40G transport networks have been on the market for six years now
- 40G (OTU3) transport equipment is shipping today in growing volumes
- By 2010 there will be large installed OTU3 WDM infrastructure in most provider networks
- Bit-transparent backhauling of 40 GbE clients will be required with existing OPU3 payload rates !

100 Gigabit Ethernet

- No existing 100G transport network
- ITU-T SG15 decided in June 2007 to extend G.709 to the next higher rate
- ITU-T SG15 is monitoring the HSSG/TF activities and will define an ODU4 rate that is sufficiently large for bit-transparent backhauling of 100 GbE

From duelk_01_0707

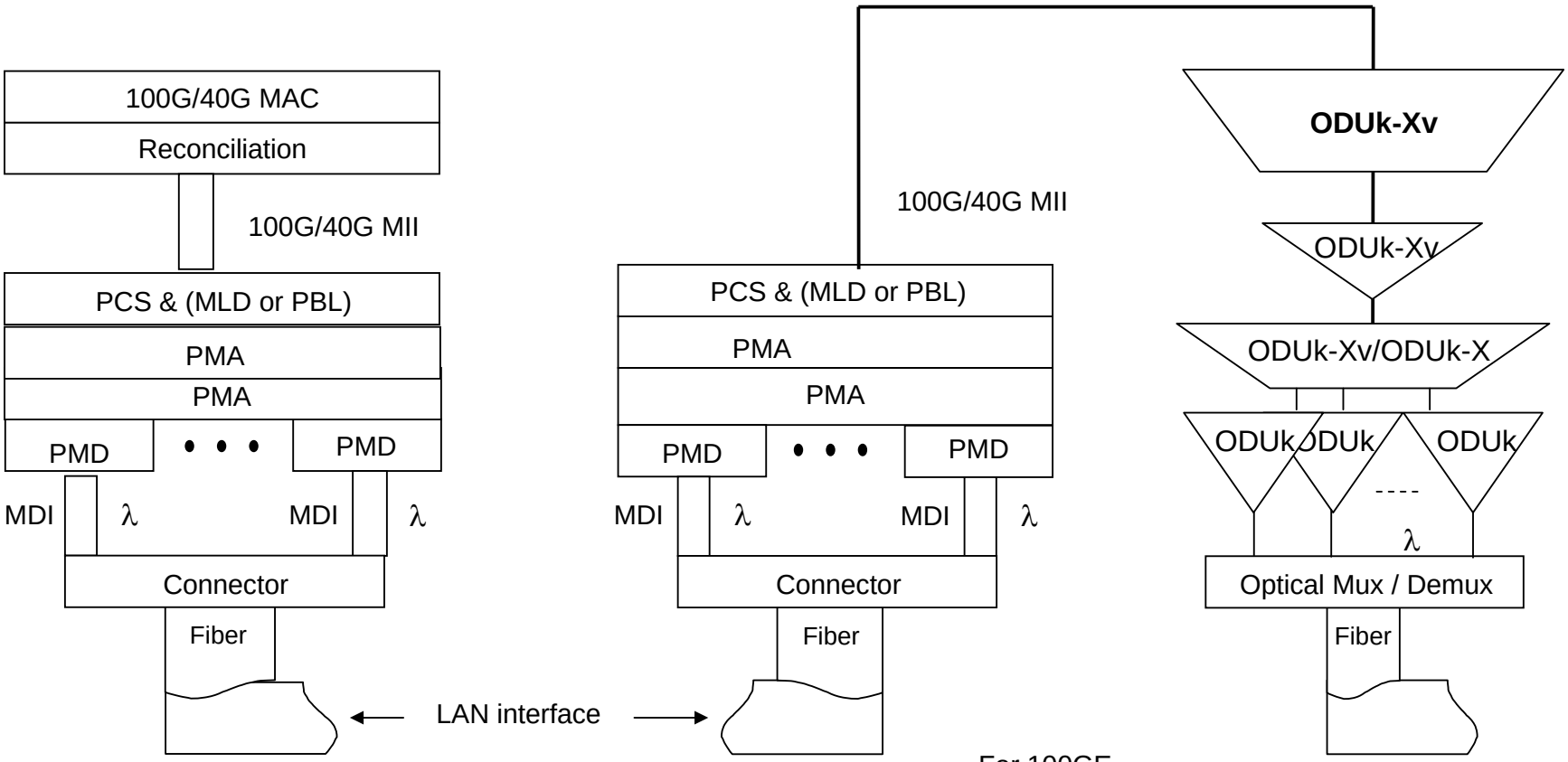
Bit Transparent Mapping of 100GE&40GE



For 100GE
- k=2, X=11(ODU2-11v)
- k=3, X=3 (ODU3-3v)
- ODU4

For 40GE
- k=2, X=5 (ODU2-5v)
- ODU3e

PCS Transparent Mapping of 100GE&40GE



For 100GE
- k=2, X=11(ODU2-11v)
- k=3, X=3 (ODU3-3v)
- ODU4

For 40GE
- k=2, X=5 (ODU2-5v)
- ODU3e

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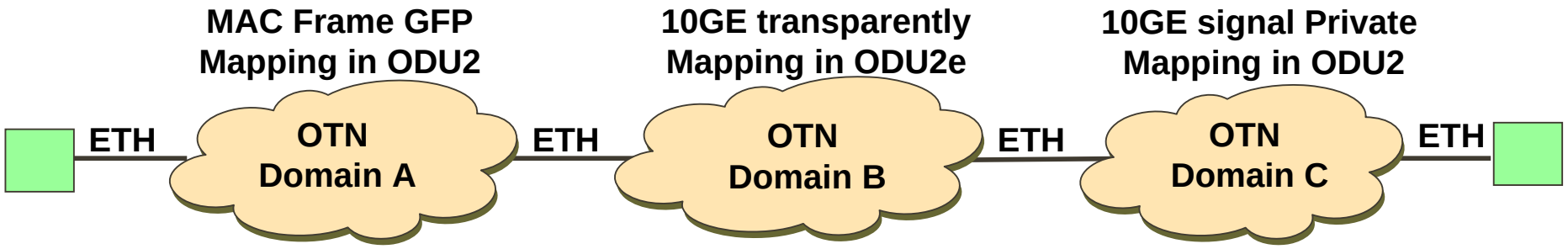
Understand the History: Local 10GE over OTN Interconnect

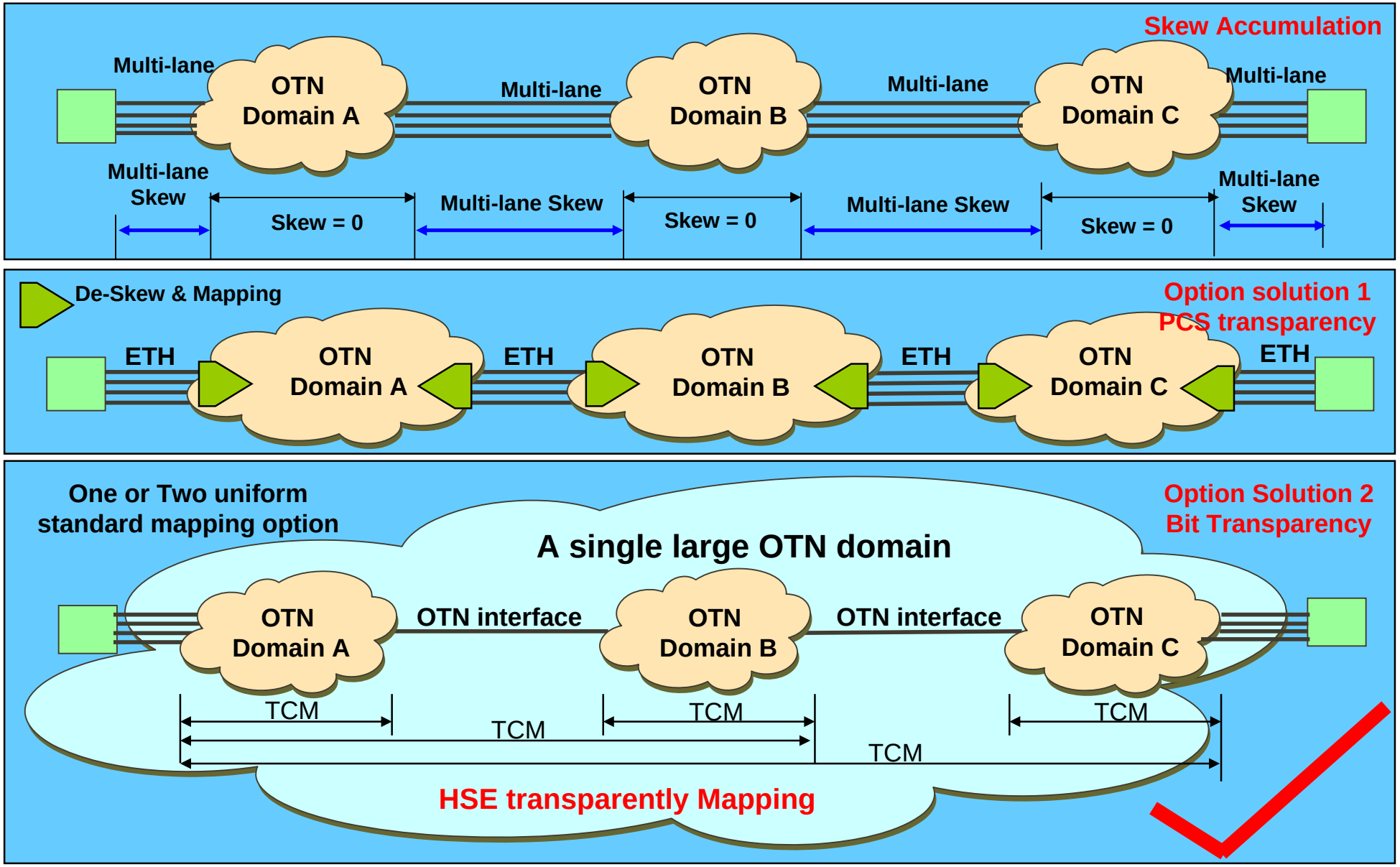
- **There have been too many options (standard or non-standard) to map 10GE LAN signal for transporting over OTN in ODU2/ODU2e. Different vendors/ transport service providers use different approaches to carrying 10GE LAN signals. 10GE LAN interface has been the most common interface for multi-OTN domain interconnections.**
  - Multiple mapping, de-mapping & re-mapping operations → High complexity for an OTN service interface line card
  - Not end-to-end solution → No end-to-end Monitoring for such long distance transport service. Each domain manages and operates its own section of a service link.
- **"Appropriate Support for OTN" objective should consider to reduce this type of inconvenience.**
- **Are we expecting any such situation in HSE (40G/100G)?**



Multi-Lane Data Traversing Multiple OTN Domains

- **Multi-lane interface for multiple OTN domain interconnections**
  - Multi-lane PHY Lane-to-Lane skew compensation is required, otherwise, the multi-lane link Lane-to-Lane skew will accumulate:
    - Increase OTN line card complexity due to mapping and de-mapping of 40GE/100GE.
    - De-skew requirement at the mapping side introduces special de-skew logic and buffer
    - 64/66b codeword based de-skew requires 64/66b Block sync process, thus it is required to run sync state machine.
  - Not end-to-end Bit Transparency
    - Multiple OTN domain architecture cannot support end-to-end bit agnostic transparency as de-skewed and re-generated HSE signal will not be the original signal any more.
- **OTN NNI Interface for multiple OTN domains interconnection**
  - 40GE/100GE is considering to "provide appropriate support for OTN”．
  - Multi-domains as a large OTN network may support end-to-end transport service.
  - Standard mapping for HSE to be transported over OTN will be supported.

Multi-Lane Data Traversing Multiple OTN Domains



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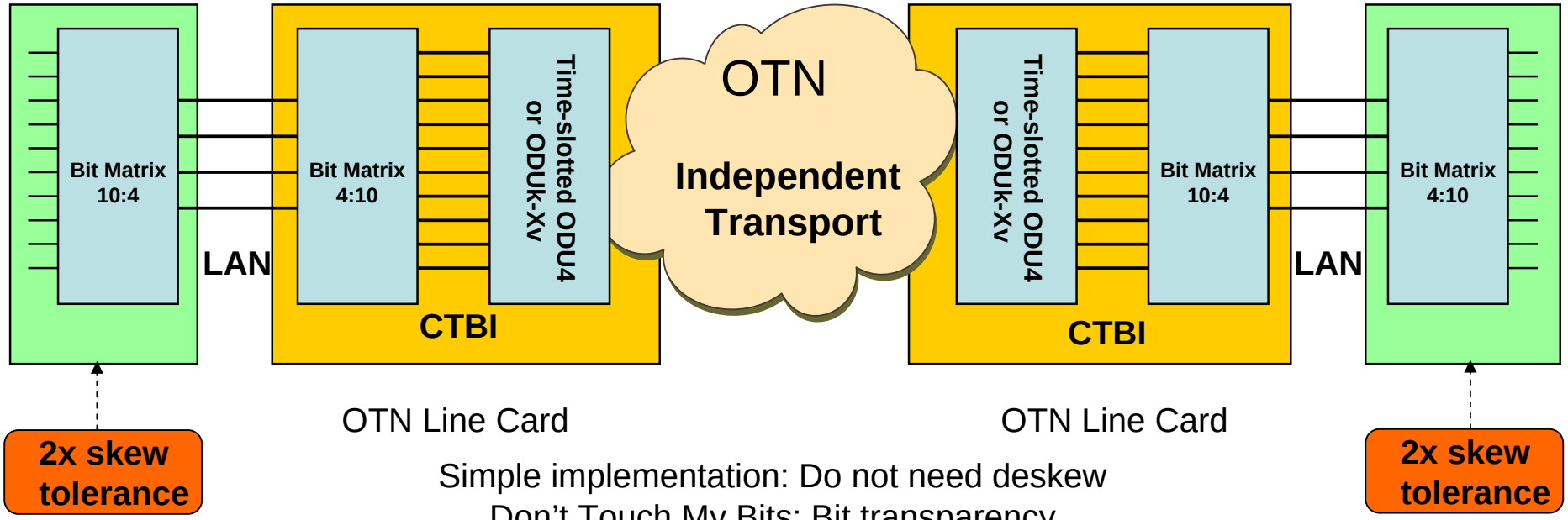
Bit Transparency and Lane-Independent Transport

- **Considerations of Bit Transparency lead to lane-independent transport mode at CTBI interface for 100GE and 40GE**
  - **Simple Implementation and low complexity (cost)**

- **Option to handle skew accumulation over HSE LAN**
  - **2X Skew tolerance**
  - **Use OTN link for OTN inter-domain interconnection**

Independent Transport for PBL



Simple implementation: Do not need deskew
Don't Touch My Bits: Bit transparency

Need 2x skew tolerance on receive side

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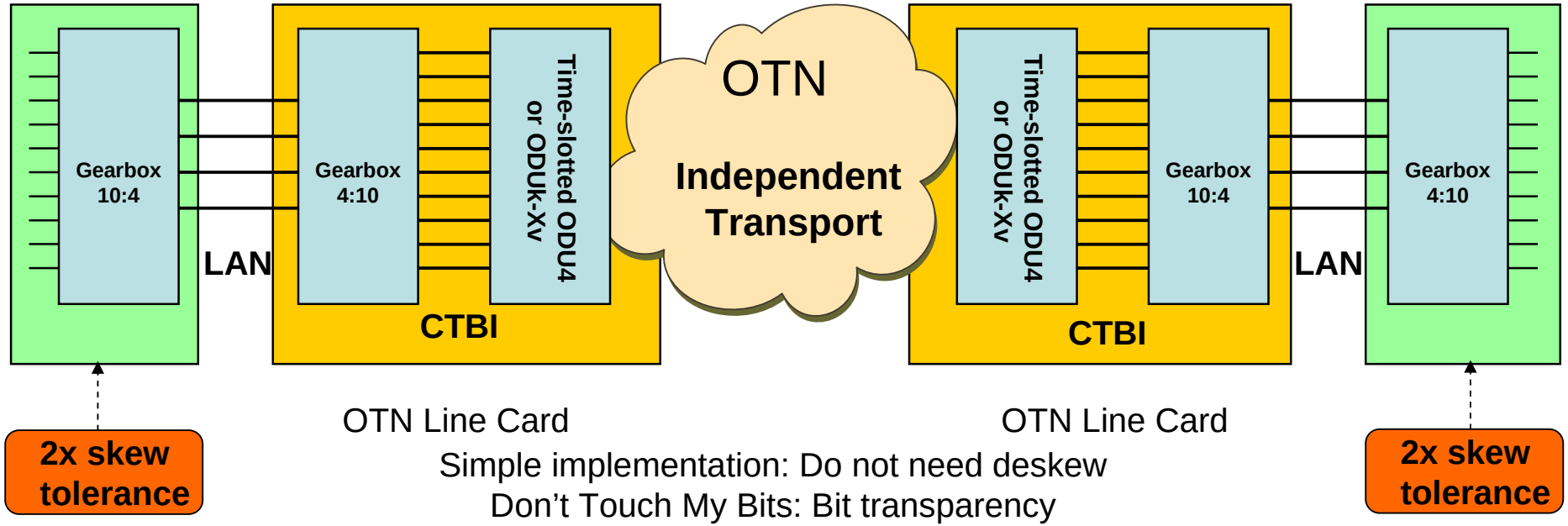
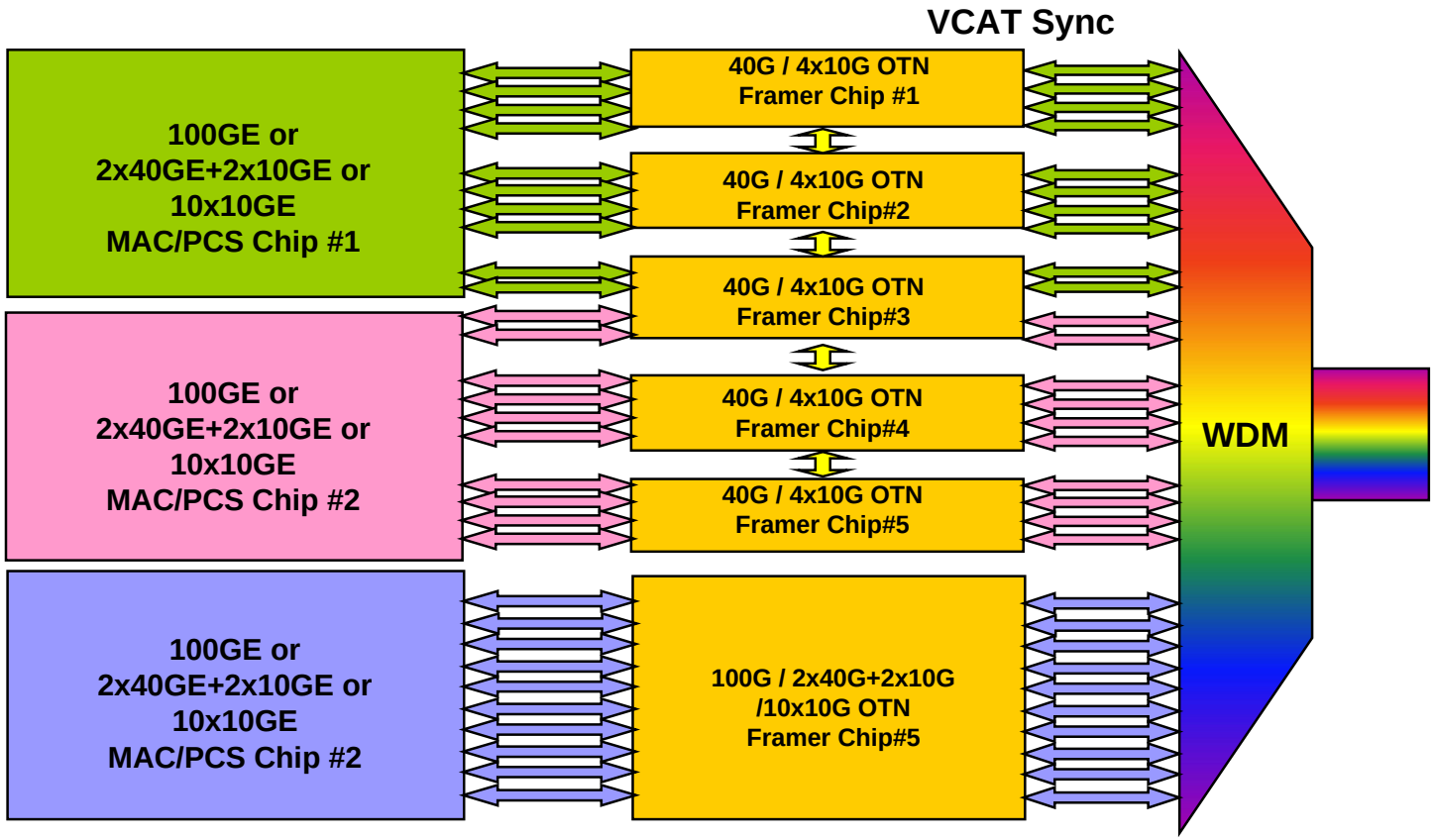
- **No need to deskew the LAN lanes at OTN ingress; No need to recover 64B/66B for each lane in the OTN node; 10 timeslots for 10 CTBI bit-streams, The same method for serial 100GE (10 timeslots for 10 CTBI); Bit transparency transport;**
- **Skew introduced by OTN domain will be compensated by VCAT or ODU4**

Independent Transport for MLD



- **No need to deskew the LAN virtual lanes at OTN ingress; No need to recover 64B/66B from each virtual lane in the OTN node; 10 timeslots for 10 CTBI bit-streams, The same method for serial 100GE (10 timeslots for 10 CTBI); Bit transparency transport;**
- **Skew introduced by OTN domain will be compensated by VCAT or ODU4**

Lane-Independent, Common OTN for 100&40&10GE



- Single MAC/PCS definition/chip design for 100GE, 40GE, and 10GE should be considered.
- "Lane-Independent model" enables OTN system to provide comparable Implementation of 100GE&40GE&10GE transport service over a common platform, thus reducing complexity.
- Enable low cost Multi-chip FPGA etc. using programmable chip for early implementation to support 100GE, 40GE and 10GE over OTN.

LAN Interface Skew Tolerance: 1x *vs*. 2x

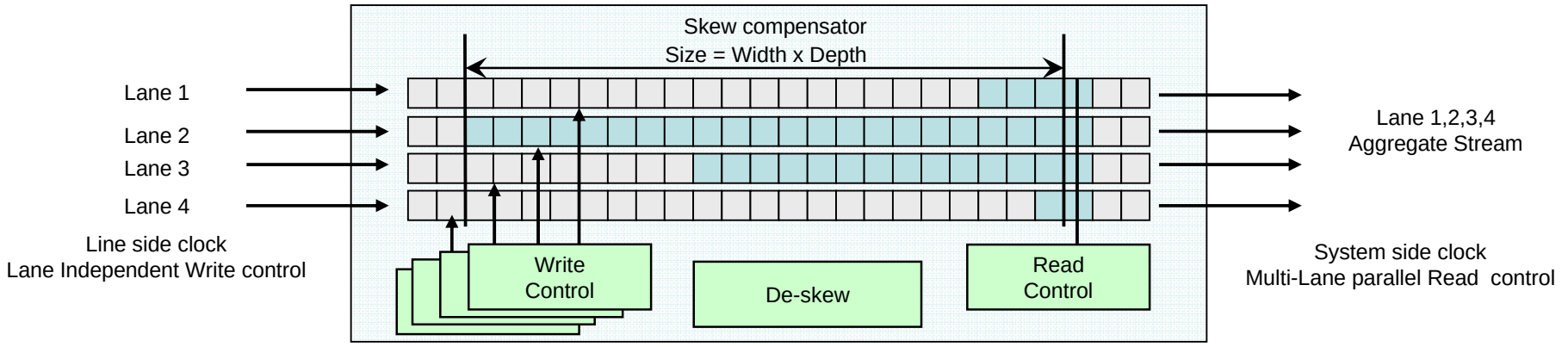
	PMD type	1x Skew (Per Lane)	1x Buffer Size (Per Lane)	2x Buffer Size (Per Lane)
40GE 4x10G MMF 100m	4 ribbon fiber, 850nm	1.94ns (#1) 20 UI	20 Bits	2x20 Bits
100GE 10x10G MMF 100m	10 ribbon fiber, 850nm		20 Bits	2x20 Bits
40GE 4x10G MMF 100m	4 ribbon fiber, 850nm	<<10ns (#2) 100 UI	100 Bits	2x100 Bits
100GE 10x10G MMF 100m	10 ribbon fiber, 850nm		100 Bits	2x100 Bits
100GE 4x25G SMF 40km	IEEE LX4 CWDM (1275.7, 1300.2, 1324.7, 1349.2nm)	151.4 UI (#3)	152 Bits	2x152 Bits
	ITU-T CWDM near 1310nm (1291,1311,1331,1351 nm)	151.6 UI (#4)	152 Bits	2x152 Bits
	ITU-T DWDM 400G Grid Near 1310nm (1308-1316 nm)	9.1 UI (#5)	12 Bits	2x12 Bits

Note: The Total Link Skew Compensation Buffer RAM Size Requirement = Lane # x PerLaneSkewUI

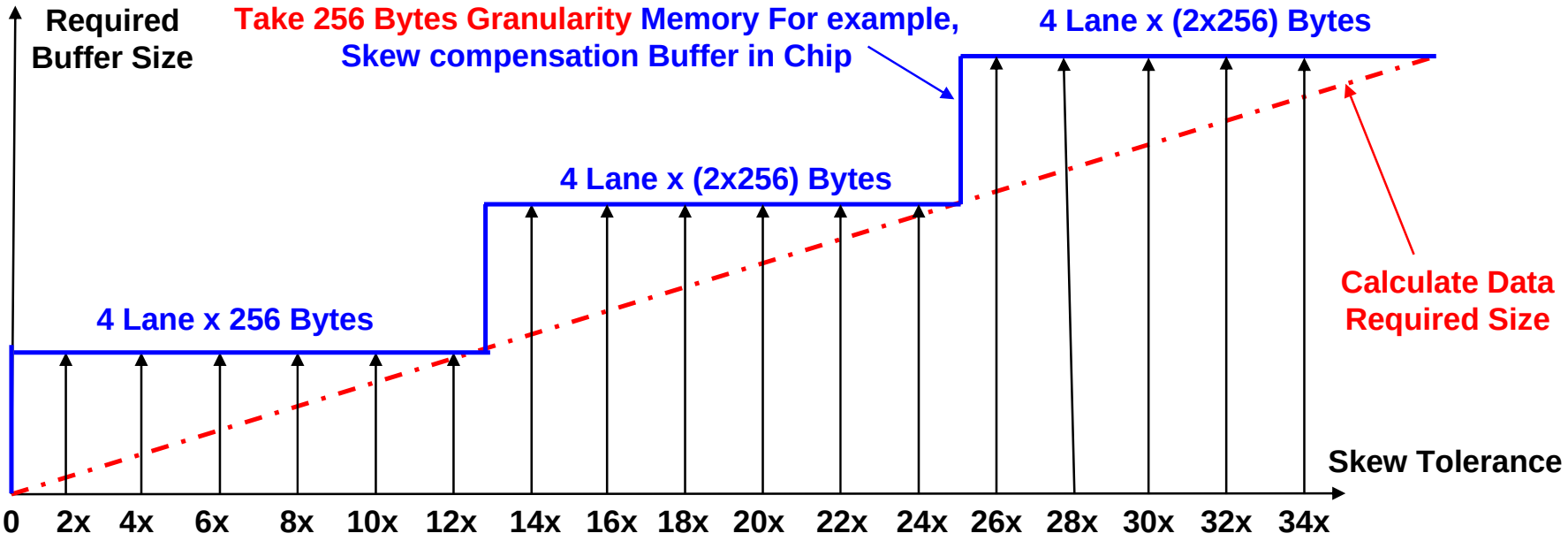
(#1)(#2) MMF Ref: nishimura_01_0906, nishimura_01_1106. The Experimental Result is 5.8ns@300m, or 1.94ns@100m; In nishimura_01_1106, the max skew is <<30ns@300m, while 30ns is the limit of a ribbon fiber skew. Here we assume that 5.8ns@300m is more reasonable.
(#3)(#4)(#5)SMF Ref: anslow_02_1107.pdf, anslow_03_1107.xls. The spreadsheet includes the above three WDM options. The values (#3), (#4),(#5) are obtained based the spreadsheet.

Worst Case 2x Buffer Size Example (4x25G)

- **Max 2x Buffer RAM Size per Lane ➔ (2x152=304bit ~ 320bit) ~ 40 Bytes**
  - **If a compensation module Digital Logic clock is 312.50 MHz (80bit x312.5MHz=25G)**
    - **The Buffer width is 10byte, and a 40 bytes buffer should have a depth of 4.**
  - **If a compensation module Digital Logic clock is 156.25 MHz (160bit x156.25MHz=25G)**
    - **The Buffer width is 20byte, and a 40 bytes buffer should have a depth of 2.**
- **At the multi-lane HSE receiver side, the multi-lane skew compensator will normally have a de-skew buffer far greater than what we have calculated here**
  - **Memories in field are normally organized in terms of fixed sizes (256/2k/128k/2M Bytes)**
  - **A 4-lane de-skew buffer will easily exceed the small depth requirement of 2, 3 or even 4.**



Skew Tolerance and Compensator Buffer Size



- **Worst case 2x Skew Tolerance ~2x152UI ~ 320 UI = 40 Bytes**
- **Take 256 bytes Memory Granularity for example, single Granularity Per lane will have a 12x Skew Tolerance . This Skew Tolerance will double when the memory block number increases.**

Summary and Proposals

✓OTN link may be used for OTN Multi-domain interconnections

✓Propose to include both Lane-Independent and Lane-Aggregate transport models to meeting different requirements for multi-lane HSE over OTN

✓Lane Independent Transport is bit transparency oriented, and is simpler to implement than Lane-aggregate Transport

✓Propose to support at least 2x skew tolerance at the HSE multi-lane receiver side

Thank You