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NANOPHOTONIC INTEGRATED CIRCUITS

Test Points and Elect. Interfaces

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3/18/08

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Agenda:

- 10G ethernet TP and electrical I/F overview
- 1G Ethernet TP and electrical I/F overview
- SFF-8431 TP and electrical I/F overview
- Recommendations for 802.3ba

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Supporters

- Gourgen Oganessyan: Quellan
- Jay Neer: Molex
- John Petrilla: Avago
- Mike Dudek: JDSU
- Rich Mellitz: Intel
- Matt Brown: AMCC

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10GBASE-R/W Test Points

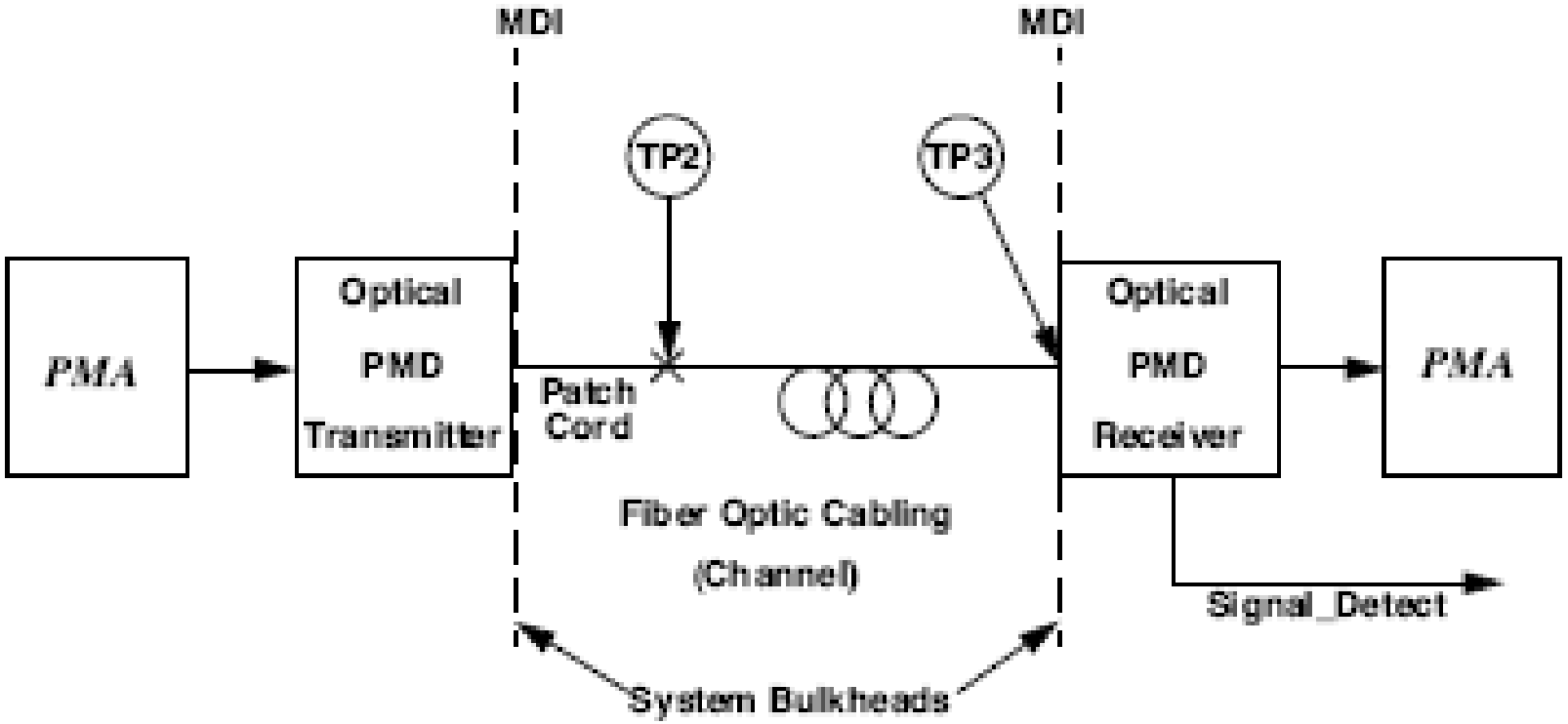

Figure 52–2—Block diagram

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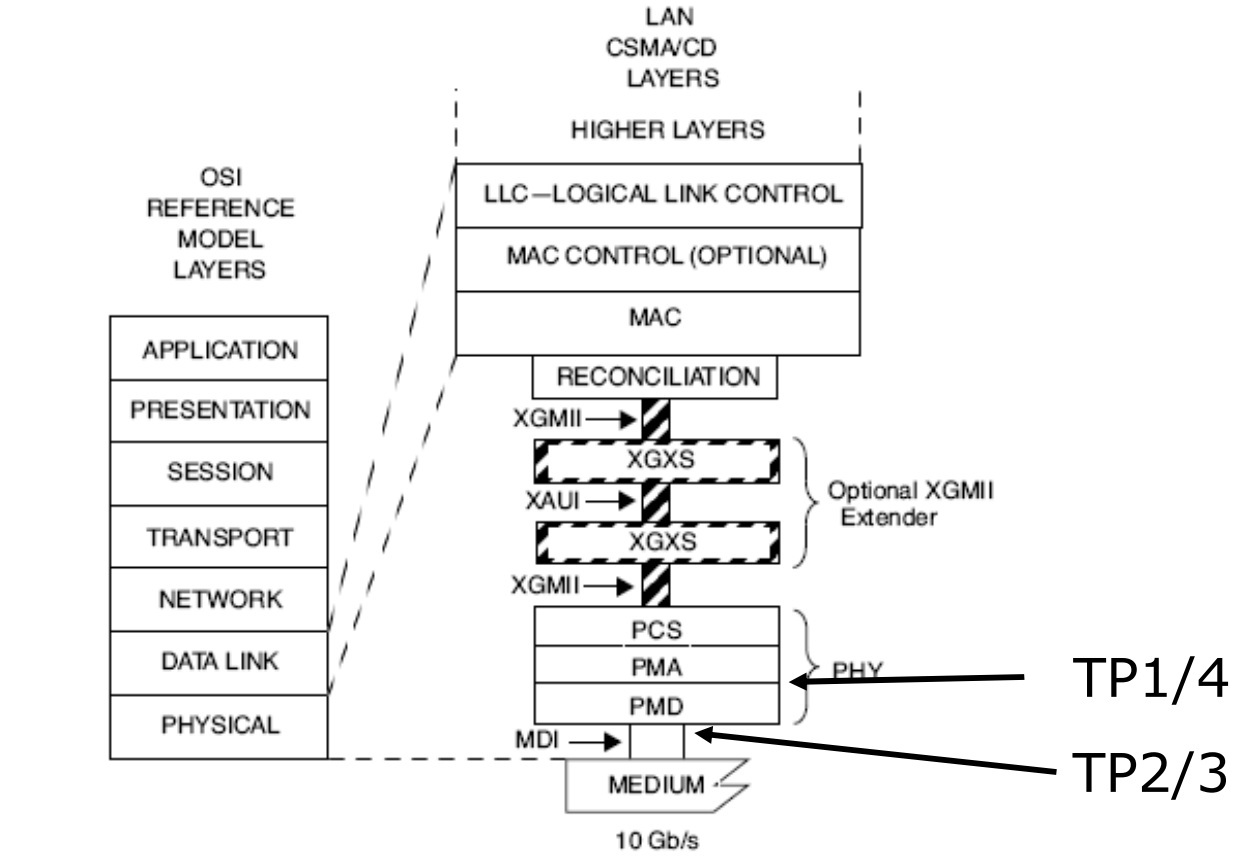
XAUI is not defined at TP1



MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XAUI = 10 GIGABIT ATTACHMENT UNIT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XGXS = XGMII EXTENDER SUBLAYER

Figure 47–1—XAUI and XGXS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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10GBASE-CX4 Test Points

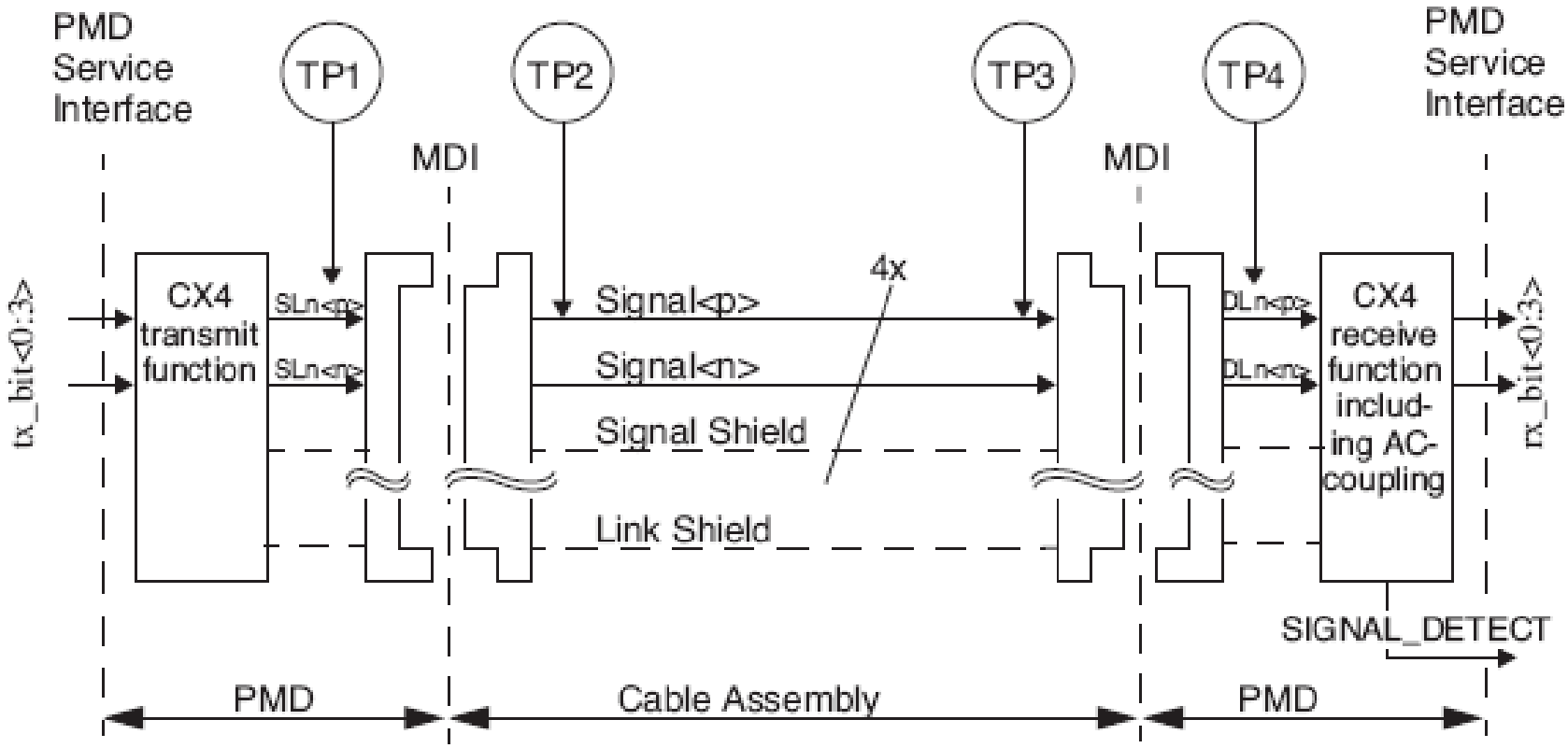

Figure 54–2—10GBASE-CX4 link (half link is shown)

1000BASE-x overview

- Overview
- Architecture
- Example
- Compliance points
- Channel types
- Channel assumptions

1000BASE-X test points

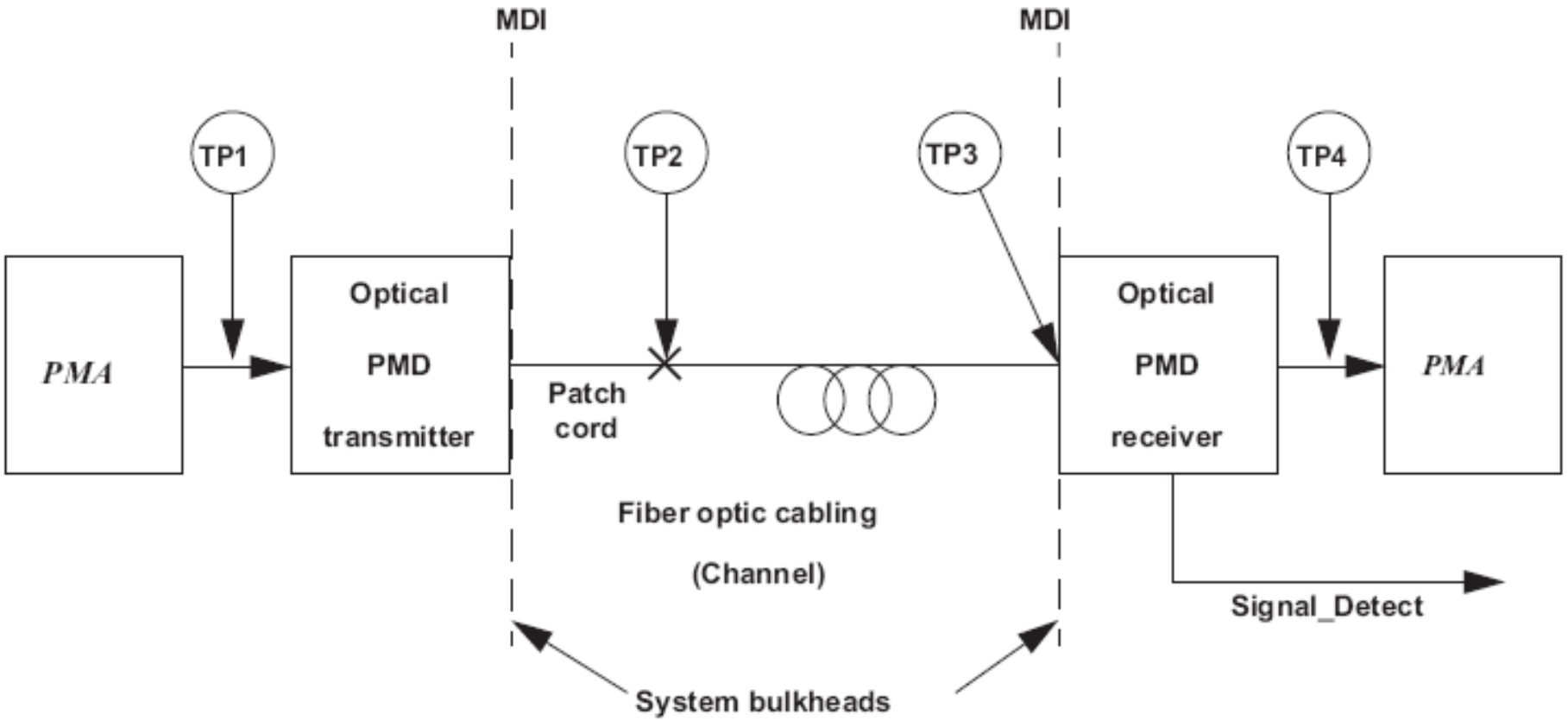

Figure 59–2—1000BASE-X block diagram

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1GE TP jitter recommendations

Table 59–9—1000BASE-LX10 jitter budget on MMF (informative)

	Total jitter		*W*	
Reference point	UI	ps	UI	ps
TP1	0.240	192	0.100	80
TP1 to TP2	0.284	227	0.100	80
TP2	0.431	345	0.200	160
TP2 to TP3	0.170	136	0.050	40
TP3	0.510	408	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4	0.749	599	0.462	370

Table 59–10—1000BASE-LX10 and 1000BASE-BX10 jitter budget on SMF (informative)

	Total jitter		*W*	
Reference point	UI	ps	UI	ps
TP1	0.240	192	0.100	80
TP1 to TP2	0.334	267	0.150	120
TP2	0.481	385	0.250	200
TP2 to TP3	0.119	95	0	0
TP3	0.510	408	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4	0.749	599	0.462	370

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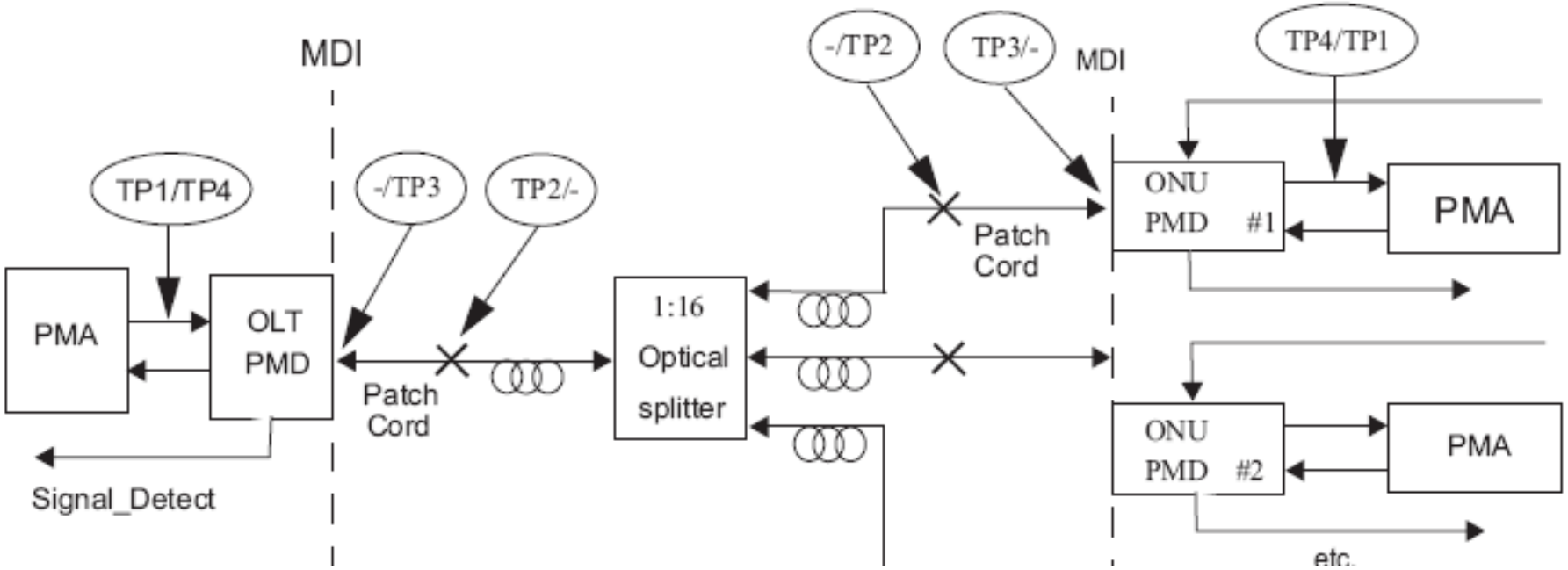
1G EPON test points



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EPON Test Point jitter specs

Table 60–10—1000BASE-PX10 and 1000BASE-PX20 downstream jitter budget (informative)

	Total jitter		Deterministic jitter	
Reference point	UI	ps	UI	ps
TP1	0.24	192	0.10	80
TP1 to TP2	0.191	153	0.15	120
TP2	0.431	345	0.25	200
TP2 to TP3	0.009	7	0	0
TP3	0.44	352	0.25	200
TP3 to TP4	0.309	247	0.212	170
TP4	0.749	599	0.462	370

SFF-8431 overview

- SFF-8431 is being defined by the Small Form Factor 8431 group. It is primarily defined for 8 and 10G optical (limiting and linear), and short reach copper.
  - Operates from 9.95G (SONET OC-192) to 11.1G (10G ethernet with G.709 FEC)

SFP+ electrical interface

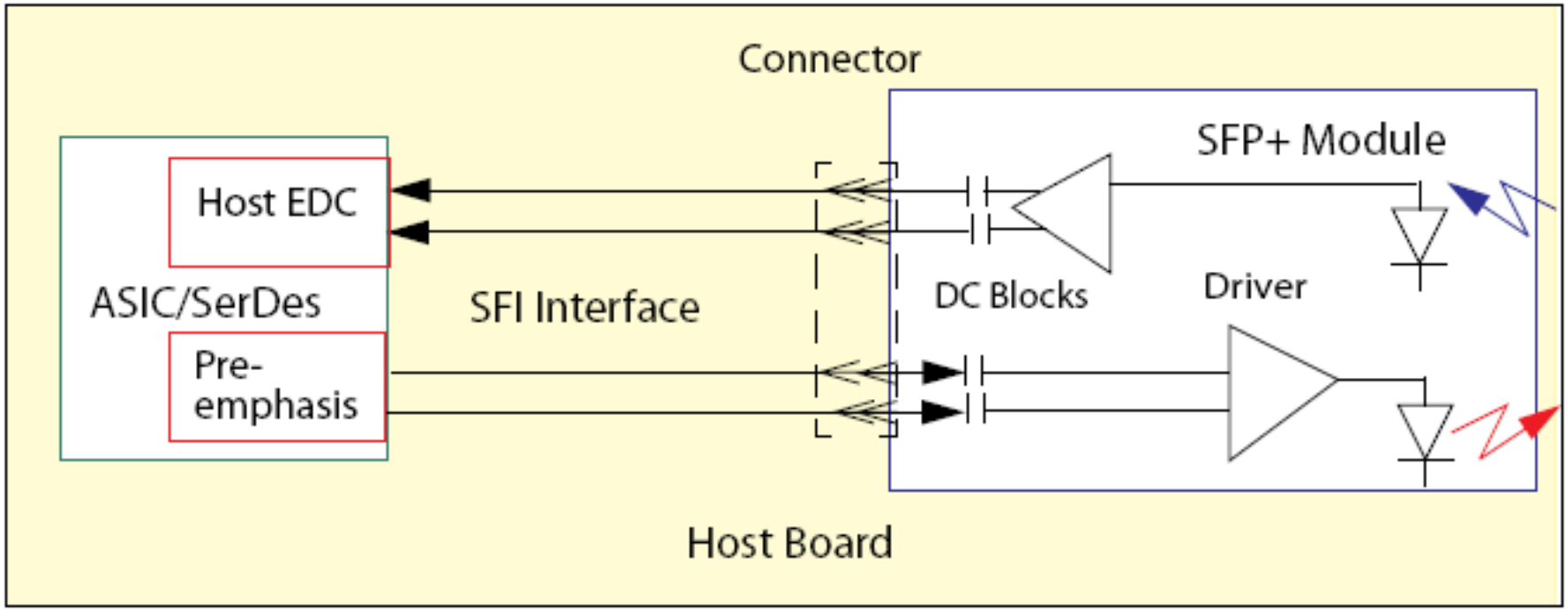

Figure 12 SFI Application Reference Model

SFP+ Host test board

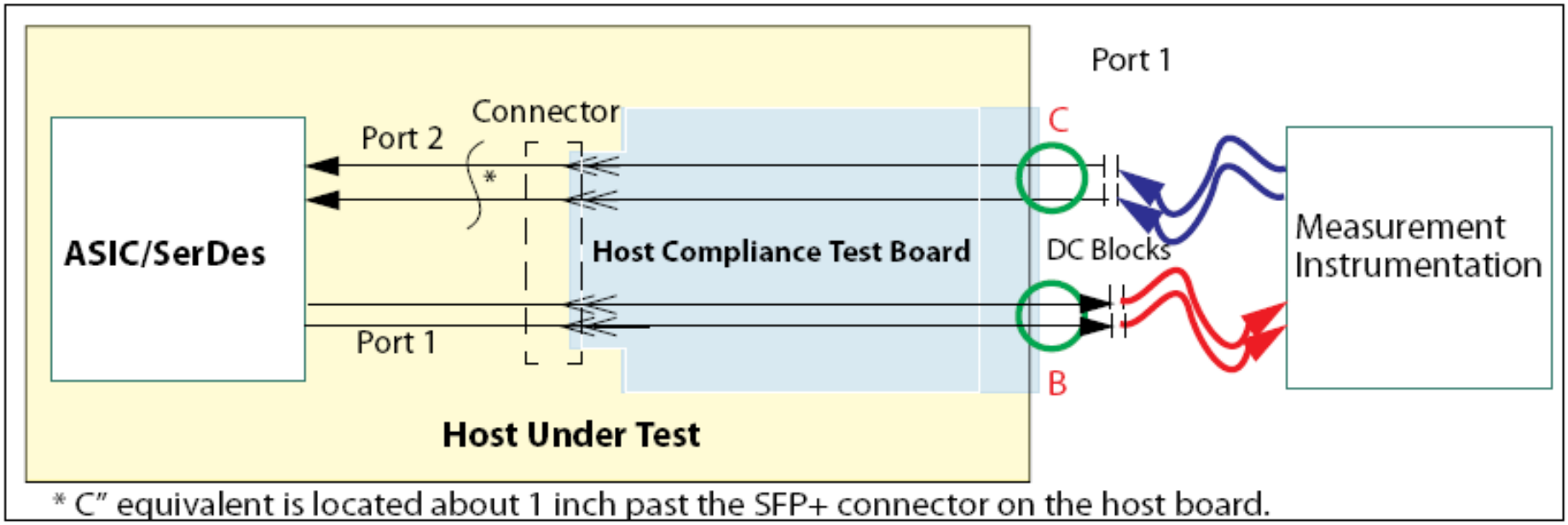

Figure 13 Host Compliance Test Board

SFP+ module test card

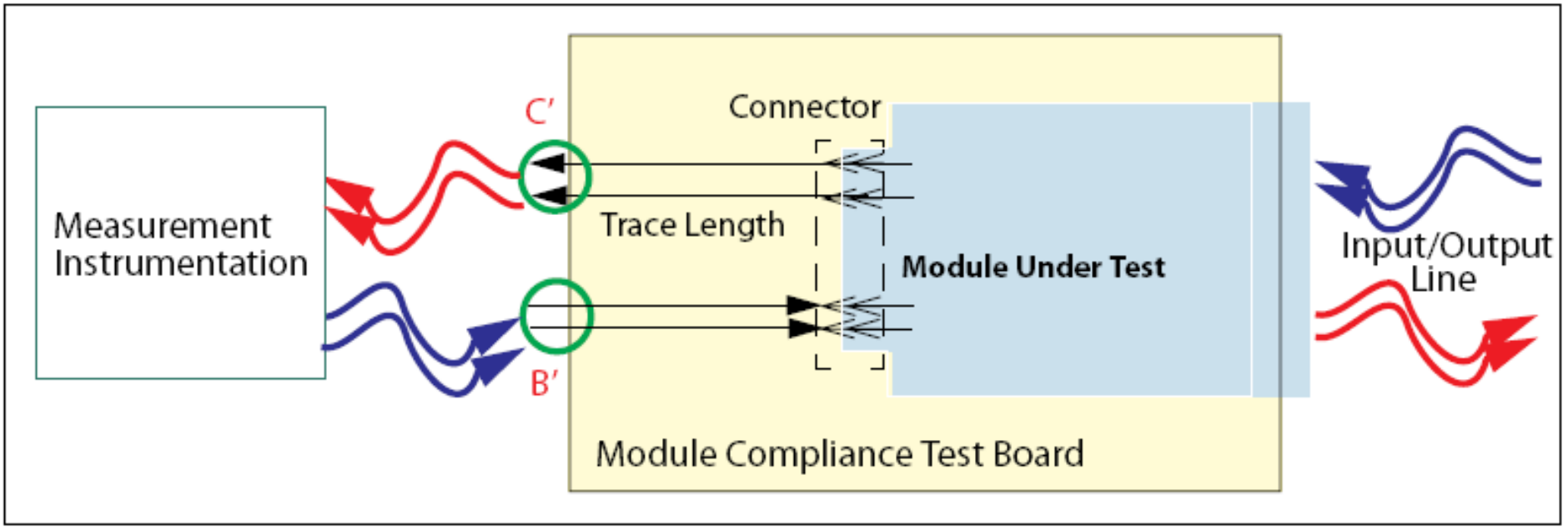

Figure 14 Module Compliance Test Board

Proposed SFP+ TX jitter specs

Table 13 SFP+ Host Transmitter Output Jitter and Eye Mask Specifications at B

Parameters- B	*Symbol*	*Conditions*	*Target Value*	*Max*	*Units*
Total Jitter	TJ	See 1, D.5		0.28	UI(p-p)
Data Dependent Jitter	DDJ	See D.3		0.1	UI(p-p)
Data Dependent Pulse Width Shrinkage	DDPWS			0.055	UI (p-p)
Uncorrelated Jitter	UJ	See D.4		0.023	UI (RMS)
Eye Mask	X1	See D.2 and Figure 19	0.14		UI
Eye Mask	X2		0.35		UI
Eye Mask	Y1		90		mV
Eye Mask	Y2		350		mV
1. The data pattern for the Total Jitter Measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64/66B data traffic.					

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Proposed SFP+ RX specs

- Note: D.5 describes the Dual Dirac model for jitter separation
- DJ is considered non-compensable

Table 20 SFP+ Limiting Module Receiver Output Jitter and Eye Mask Specifications at C'

Parameters - C'	*Symbol*	*Conditions*	*Min*	*Target*	*Max*	*Units*
Crosstalk source rise/fall time (20% to 80%)	Tr, Tf	See D.10.5		35		ps
Output Rise and Fall time (20% to 80%)	Tr, Tf	See 1	28			ps
Total Jitter	TJ	See 2, D.5			0.70	UI (p-p)
Deterministic Jitter	DJ	See D.5,			0.42	UI (p-p)
Eye Mask	X1	See D.2, D.10			0.35	UI
Eye Mask	Y1		150			mV
Eye Mask	Y2				425	mV

1. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1's and four 0's sequence in the PRBS 9 is an acceptable alternative.
2. The data pattern for the total jitter measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

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Conclusions

- 1000BASE-X, 1000BASE-PX, 10GBASE-CX4 provide either normative or informative jitter specifications at TP1. We should follow this model and specify jitter budgets at TP1 for 802.3ba PMDs.
- SFF-8431 provides the latest jitter budget for a TP1 specification. For the multi-lane/MM variants changes will be needed.
- 10GBASE-KR provides a good starting point for the jitter budget for a TP1/4 specification for the 40G copper variant
- Next generation XAUI (CAUI) should not be considered as a TP1 specification