40/100G Copper Feasibility-2

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PhyCore Technology

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Outline

Update of the previous contribution[1] with measured channel and crosstalk data[2,3,4]

1. **SNR and Noise Margin**
2. **Measured Data of Cable Assembly[2]**
3. **Signaling Selection by Salz SNR**
4. **Achievable Noise Margin with IC Implementation**
5. **Passive Module[5]**
6. **Summary**

[1] http://www.ieee802.org/3/hssg/public/nov07/takatori_02_1107.pdf
[2] http://www.ieee802.org/3/ba/public/jan08/diminico_01_0108.pdf
[3] http://grouper.ieee.org/groups/802/3/ba/public/tools/ghiaisi_c1_1207.pdf
[4] http://grouper.ieee.org/groups/802/3/ba/public/tools/na_01_1207.pdf
[5] http://www.ieee802.org/3/hssg/public/nov07/ghiasi_02_1107.pdf

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SNR vs. EYE-Opening

Question: “Is BER OK when EYE is open?”

The answer depends on system impairments.

YES: Chip to chip I/O environment in which high SNR is guaranteed and deterministic ISI is much bigger impairment than random noise source.
→ EYE / LINK Budget

NO: When random (Gaussian) noise sources such as crosstalk, IC electronics noise, and random jitter are major impairments.
(Backplane, Long reach CEI, and Cable applications)
→ SNR / Noise Margin

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Noise Margin

The best method to characterize PHY QOS is "Noise Margin"

"Noise Margin" Definition

Noise Margin = [Achievable SNR] – $SNR_{required}$

$SNR_{required}$ is 17dB for 2PAM-NRZ

24dB for 4PAM (BER = 10-12).**

Target Margin: 3 ~ 6dB

"6dB in theory and 3dB with worst case conditions w IC implementation"

Achievable SNR is determined by Channel, Noise environment, Jitter, and IC Implementation.

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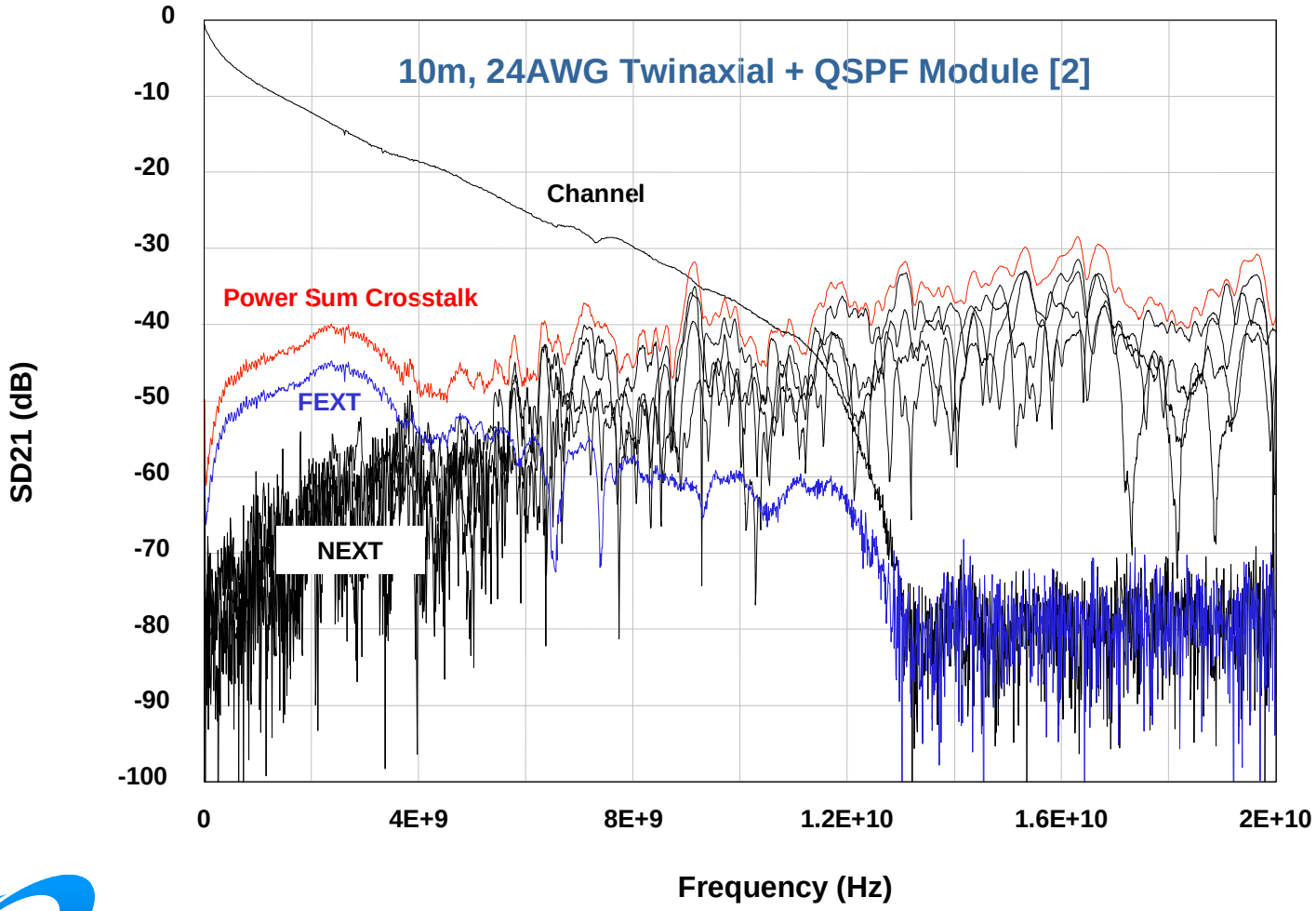
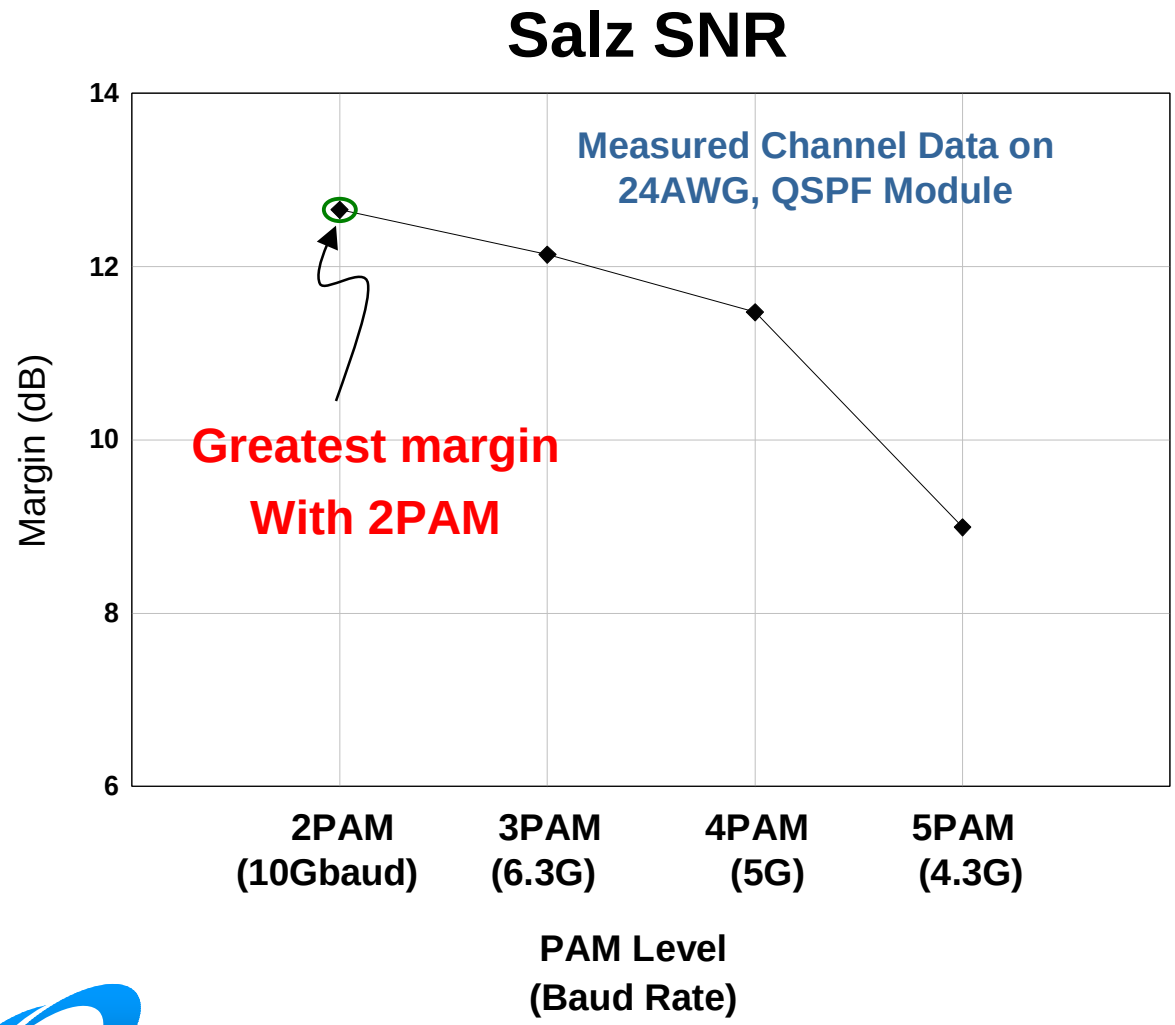
Channel IL and Crosstalk

Cable Assembly with QSFP



Signaling for 40G (4-lane)



2PAM is the best signaling for 40G, 4-lane system.

24AWG, 10m Cable

No coding gain

IC Noise, -140dBm/Hz

TX Power = 5dBm

With measured crosstalk

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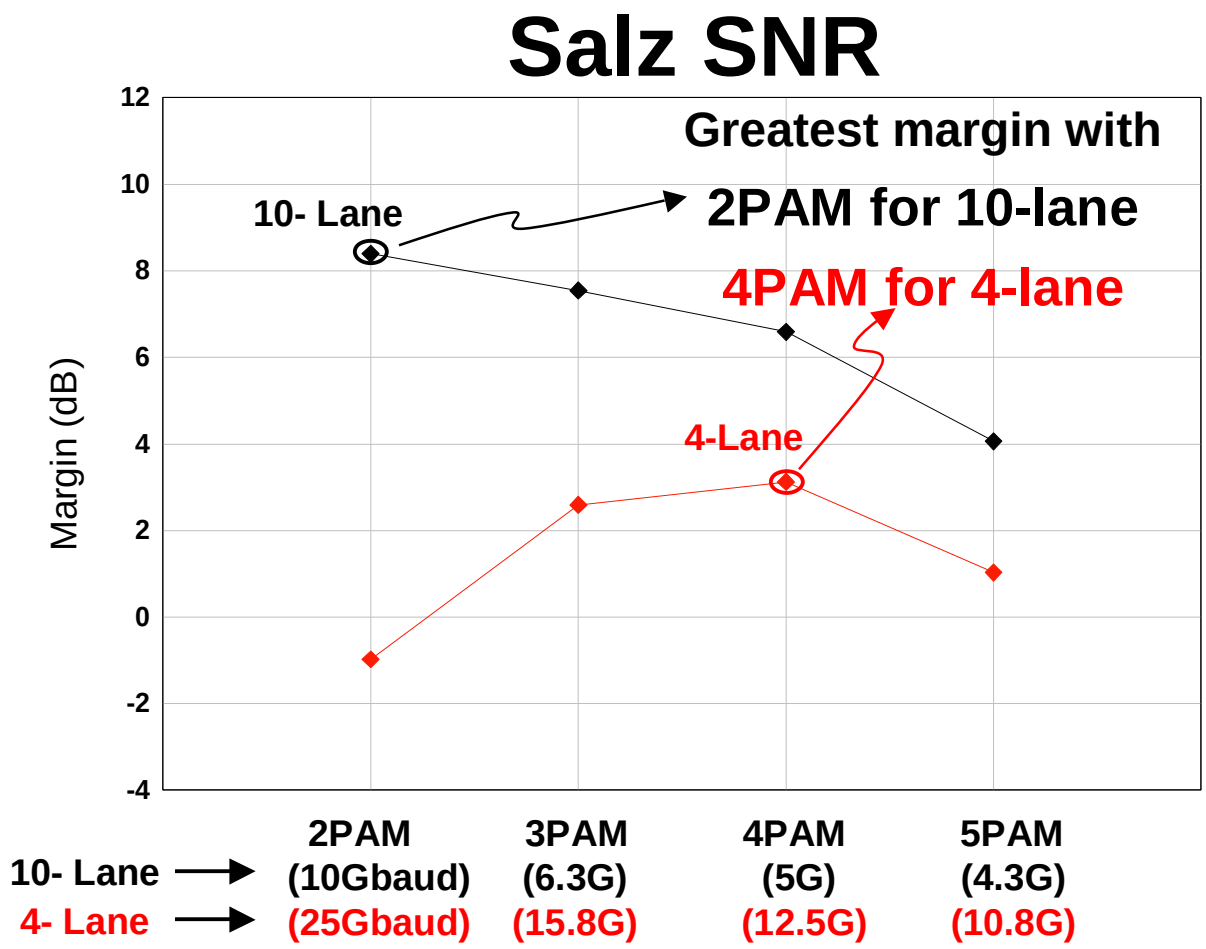
Signaling for 100G(4 & 10-lane)



2PAM is the best signaling for 100G, 10-lane system.

4PAM has advantage over 2PAM by 4dB for 4-lane system, however, margin is not enough.

24AWG, 10m Cable

No coding gain

IC Noise, -140dBm/Hz

TX Power = 5dBm

With measured crosstalk

Behavioral Time Domain Simulation

- How does BER relate to an EYE Diagram?
- Vertical EYE closure by ISI and Noise?
- Horizontal EYE closure by Jitter?
- How do we simulate random noise?
- What is the importance of sampling phase?

Some of these issues ignored and assumed to be ideal by Salz SNR are incorporated by the behavioral time domain simulation with key IC implementation impairments.

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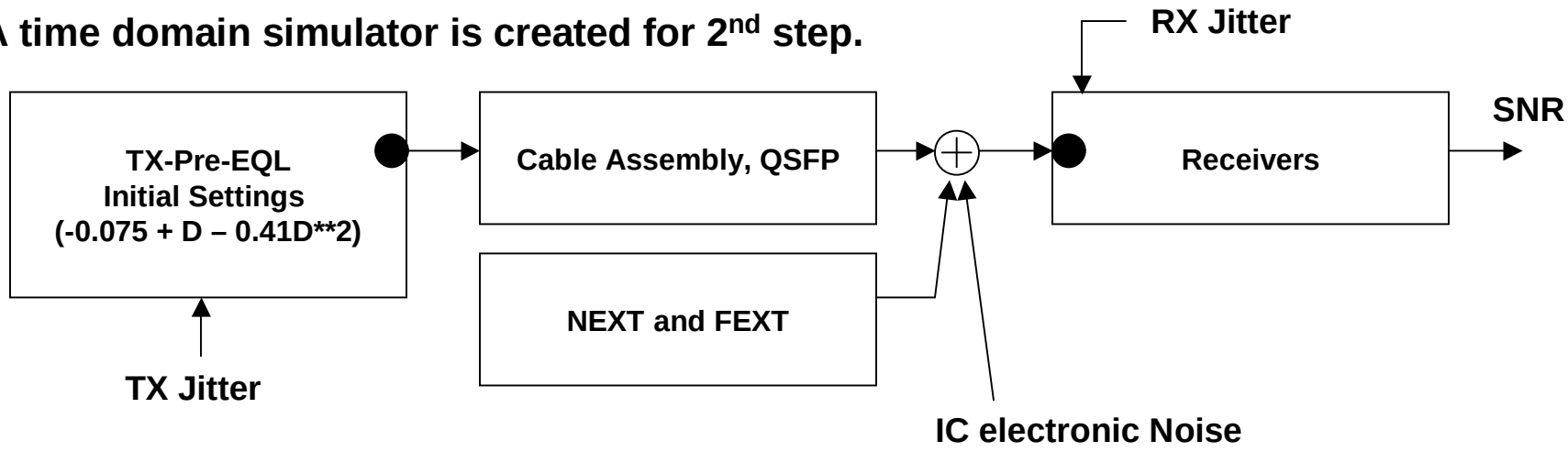
Behavioral Time Domain Simulation

A time domain simulator is created for 2nd step.



TX Jitter	**0.15UIpp jitter**
RX Jitter	**systematic timing recovery jitter**
IC Electronic Noise	**-140dBm/Hz**
FFE	**8 tap**
DFE	**8, 16, 32 tap**

Crosstalk Canceller added later as an option

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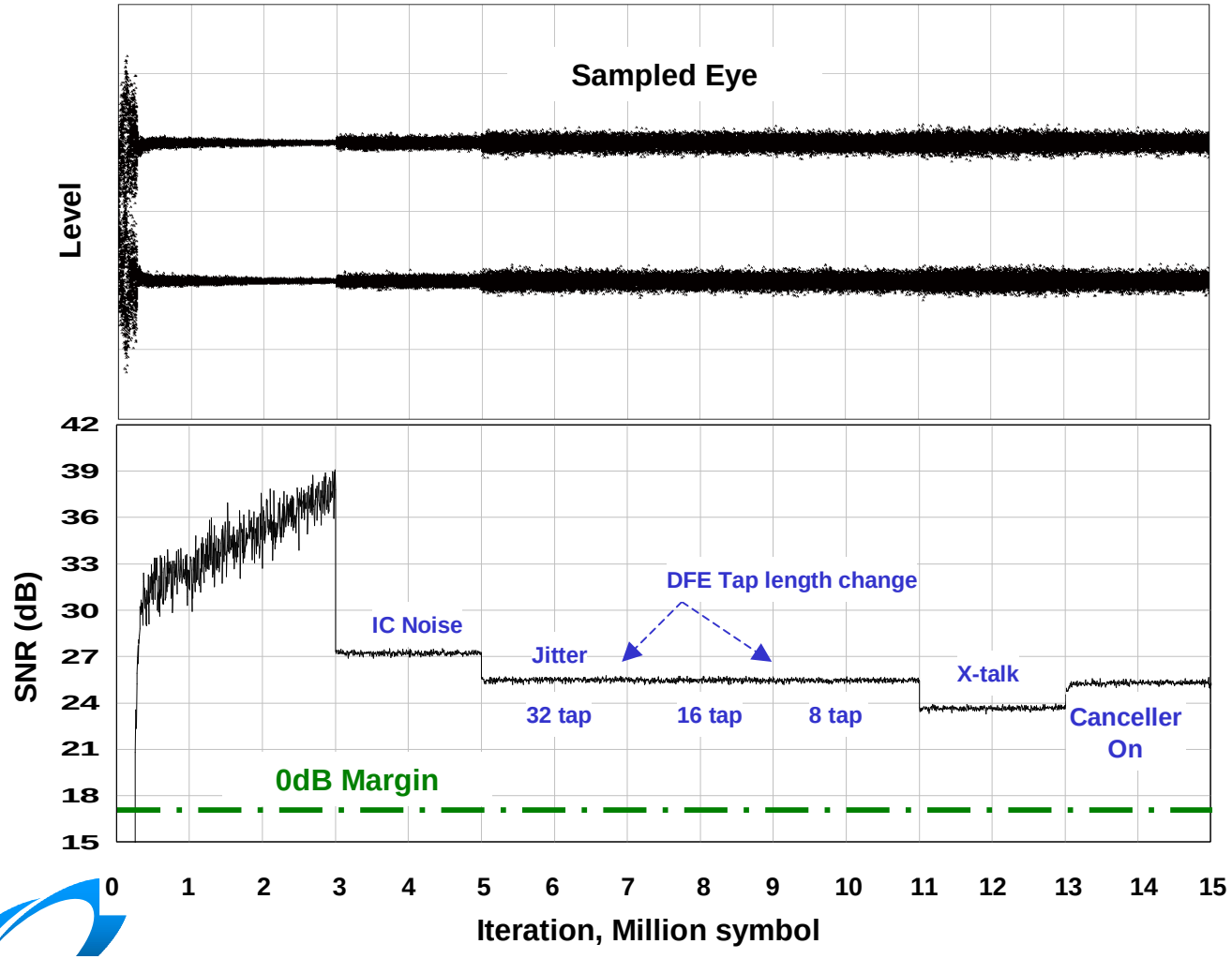
Result-1: 40G, 10G x 4-Lane

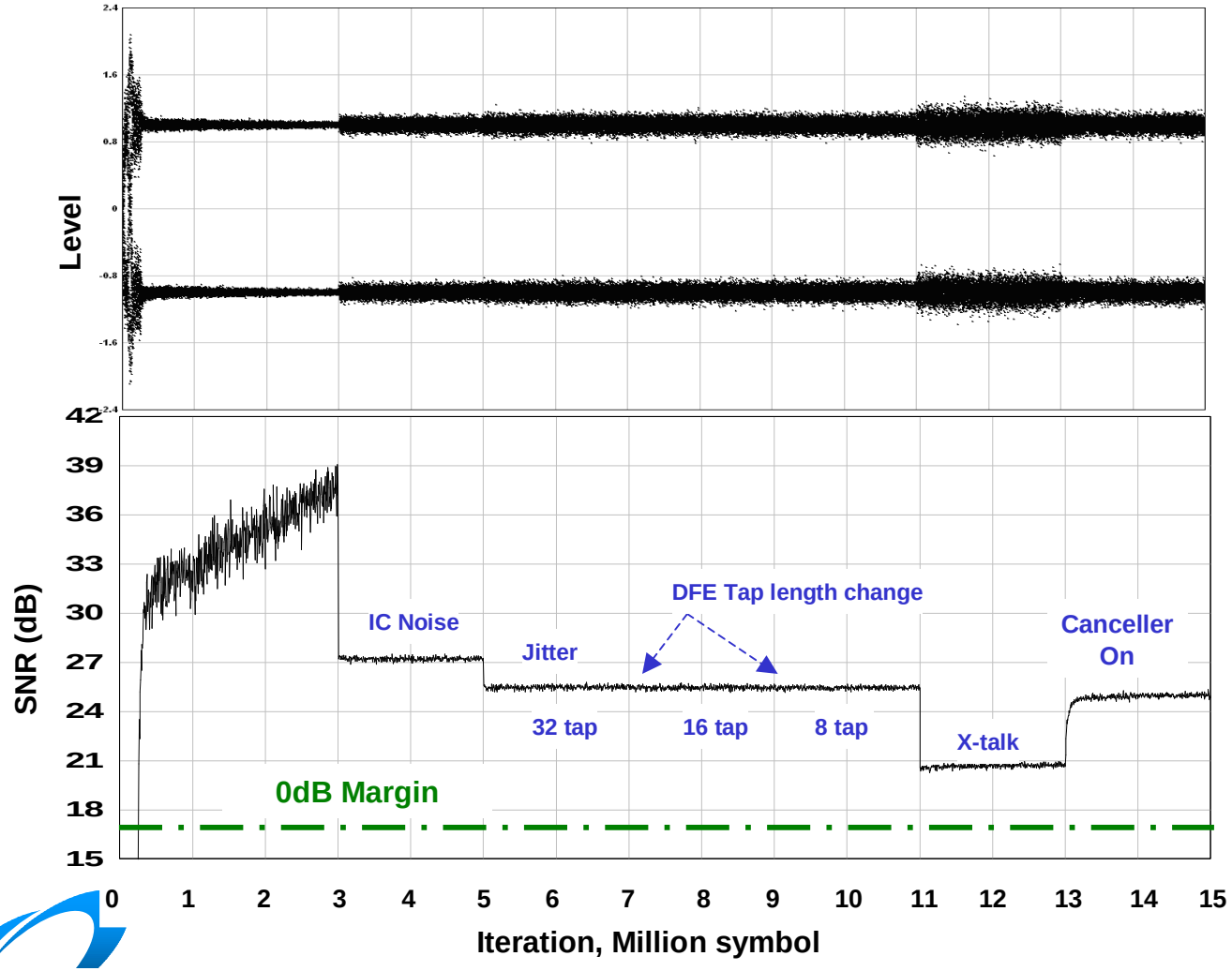


Noise Margin:

6.8dB
(w/o canceller)

8.4dB
(w canceller)

Result-2: 100G, 10G x 10-Lane



Noise Margin:

3.7dB

(w/o canceller)

8.1dB

(w canceller)

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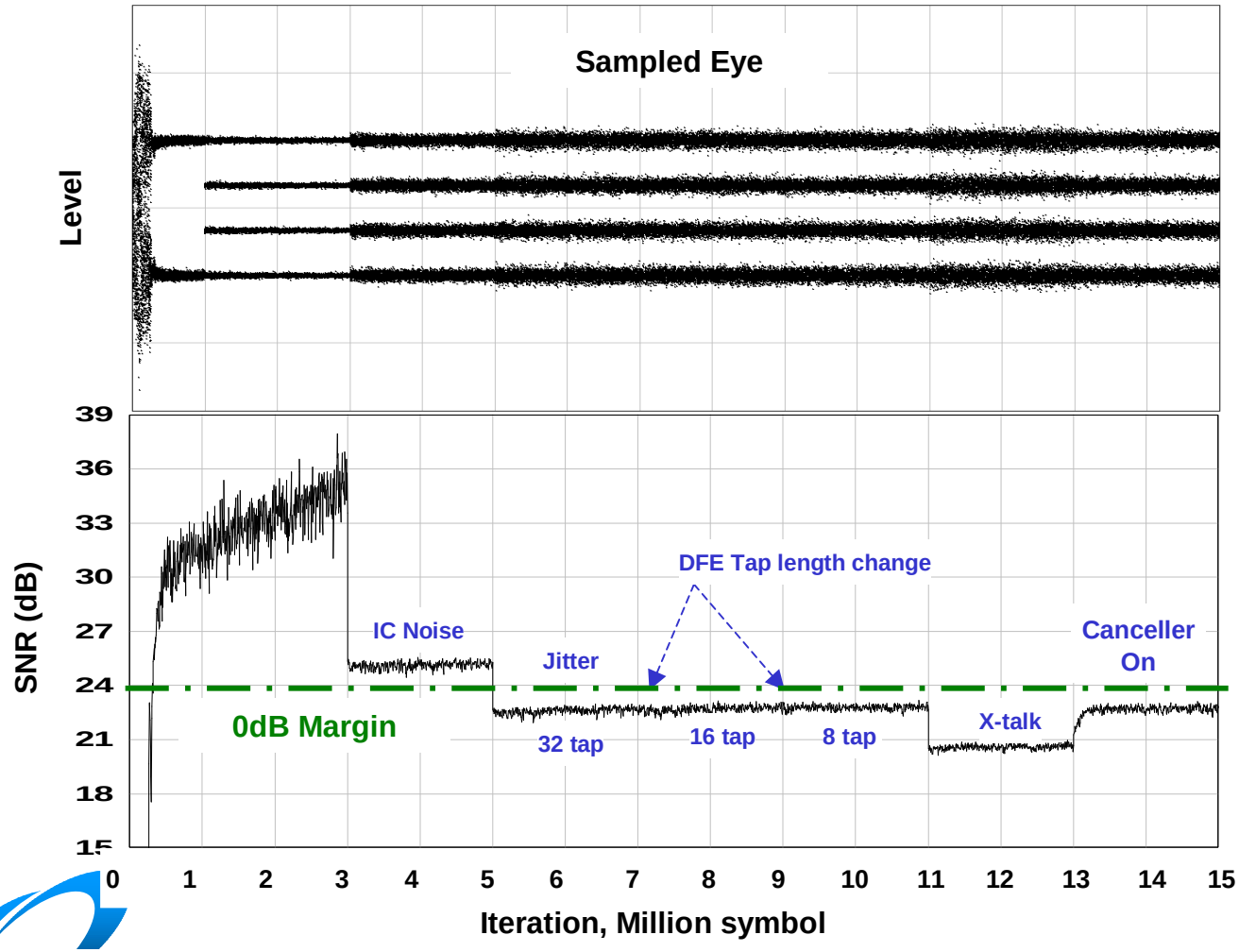
Result-3: 100G, 25G x 4-Lane



Noise Margin:

-3.3dB

(w/o canceller)

-1.2dB

(w canceller)

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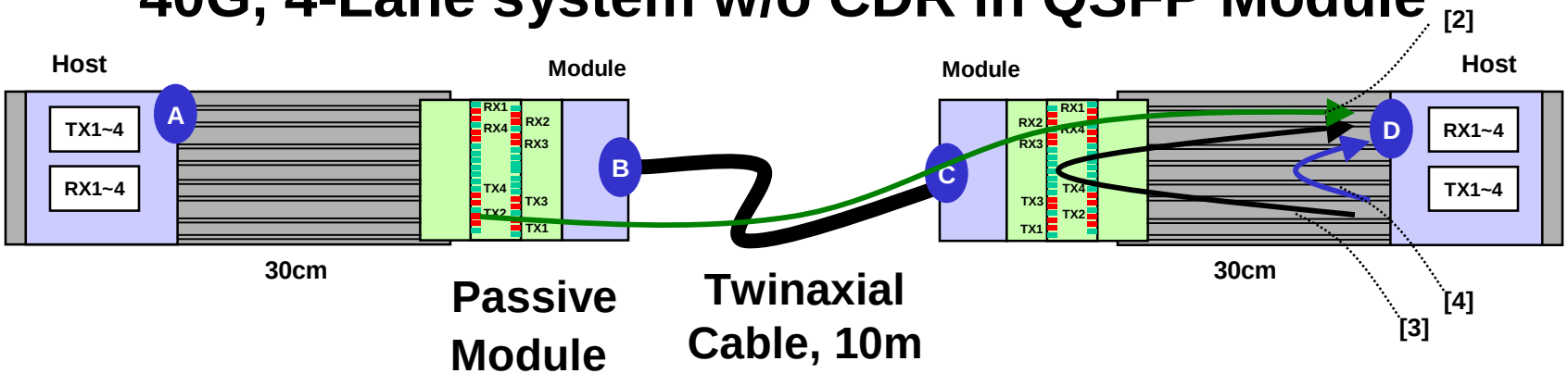
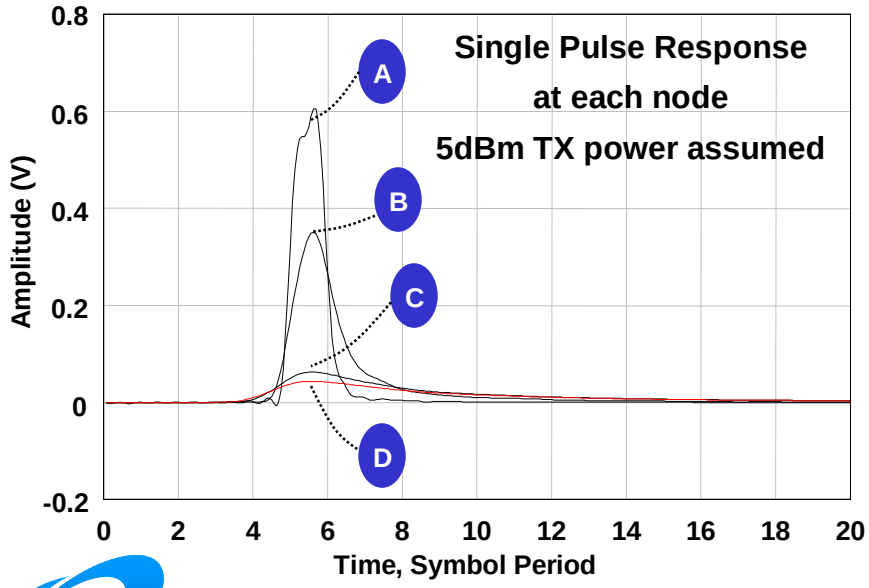
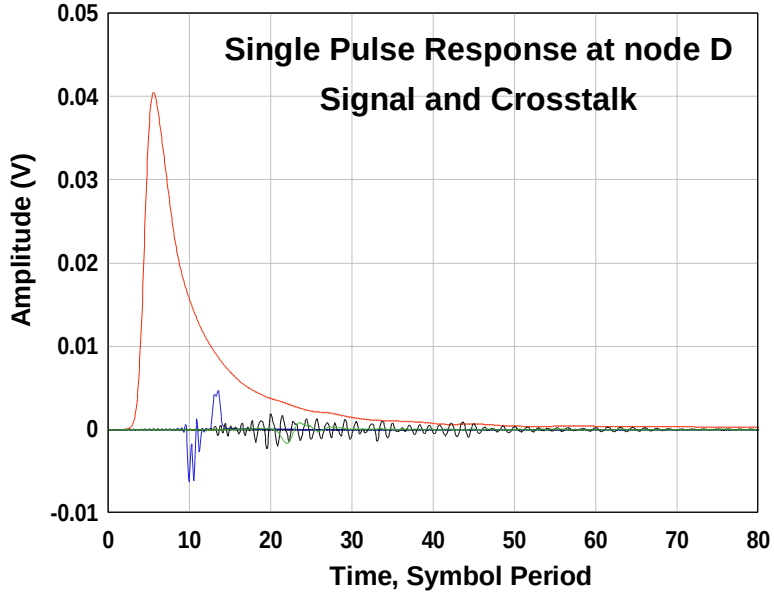
Passive Module

40G, 4-Lane system w/o CDR in QSFP Module







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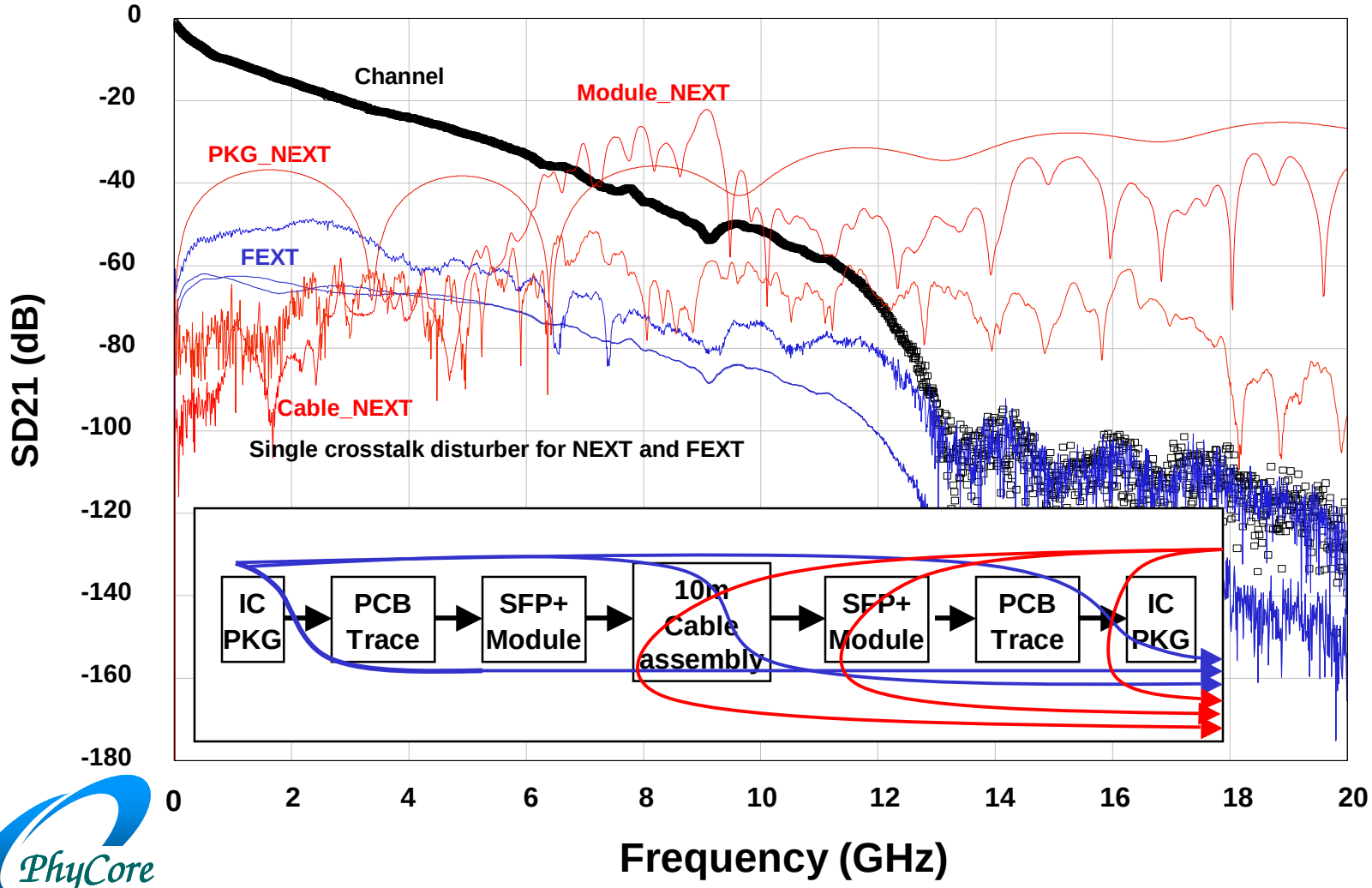
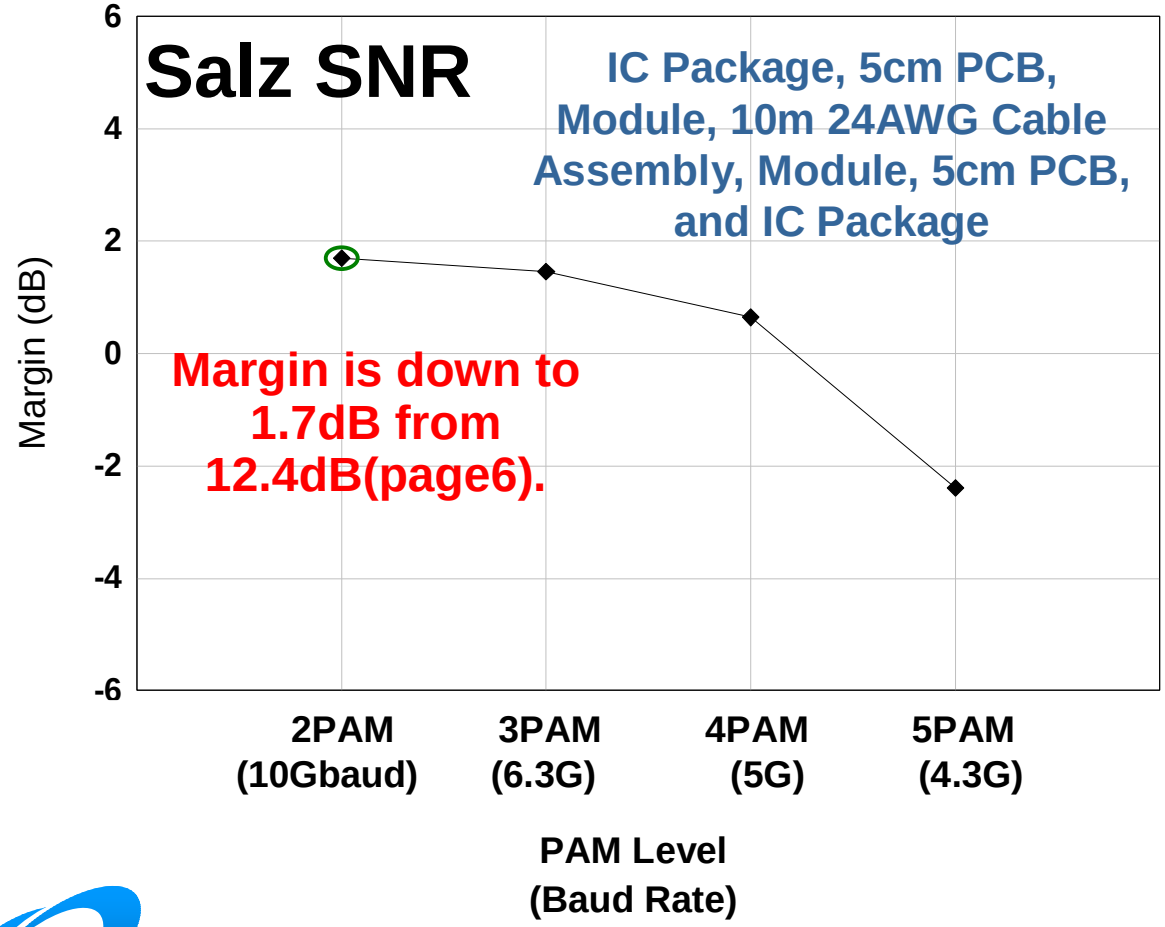
Channel IL and Crosstalk

IC Package, 5cm PCB, Module, 10m 24AWG Cable Assembly, Module, 5cm PCB, and IC Package



Noise Margin of Passive Module 40G (4-lane)



Margin degradation is more than 10dB with the additions of

-IC package,

-PCB trace,

-module.

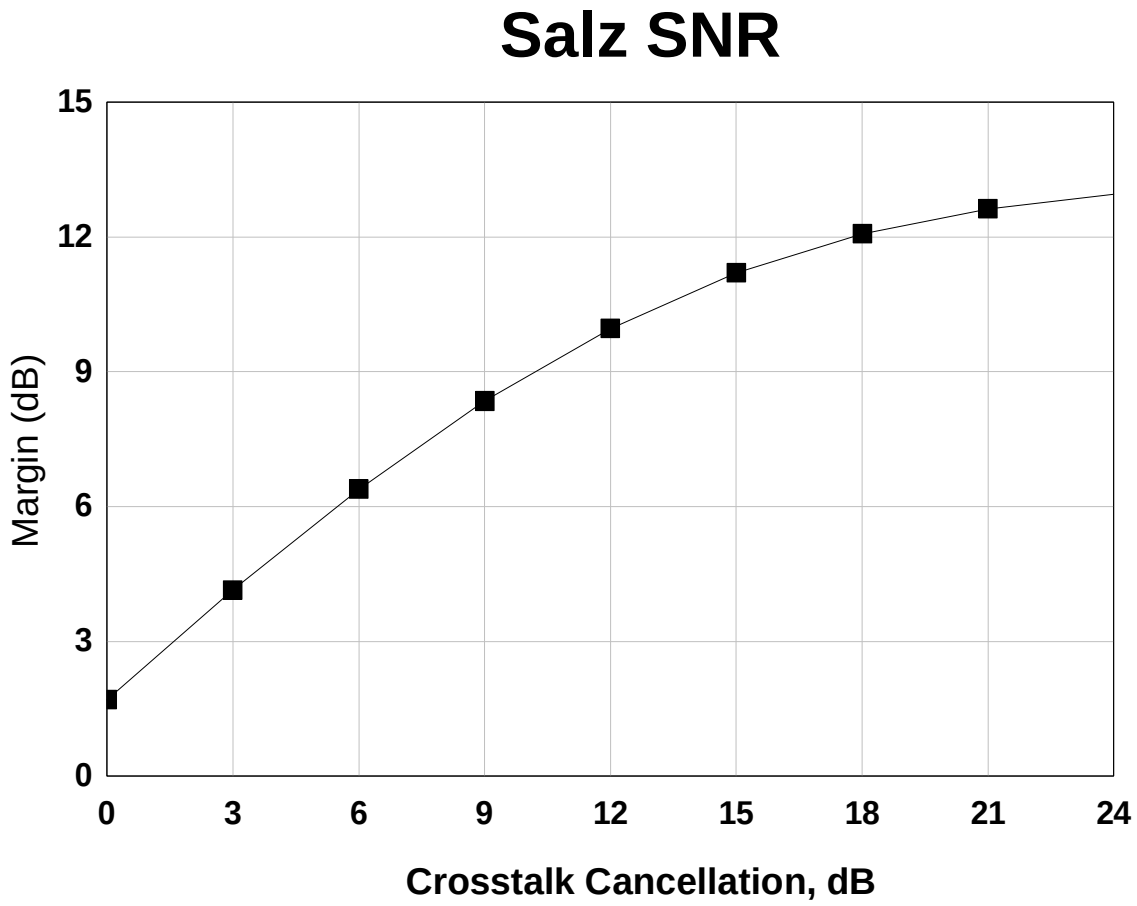
This is due to crosstalk of Package Model(IBM)[4] PCB(5cm) + Module[3] (Both sides)

No coding gain

IC Noise, -140dBm/Hz

TX Power = 5dBm

Improvement by Canceller



Crosstalk canceller improves margin dramatically.

Passive module requires crosstalk canceller and FEC.

No coding gain

IC Noise, -140dBm/Hz

TX Power = 5dBm

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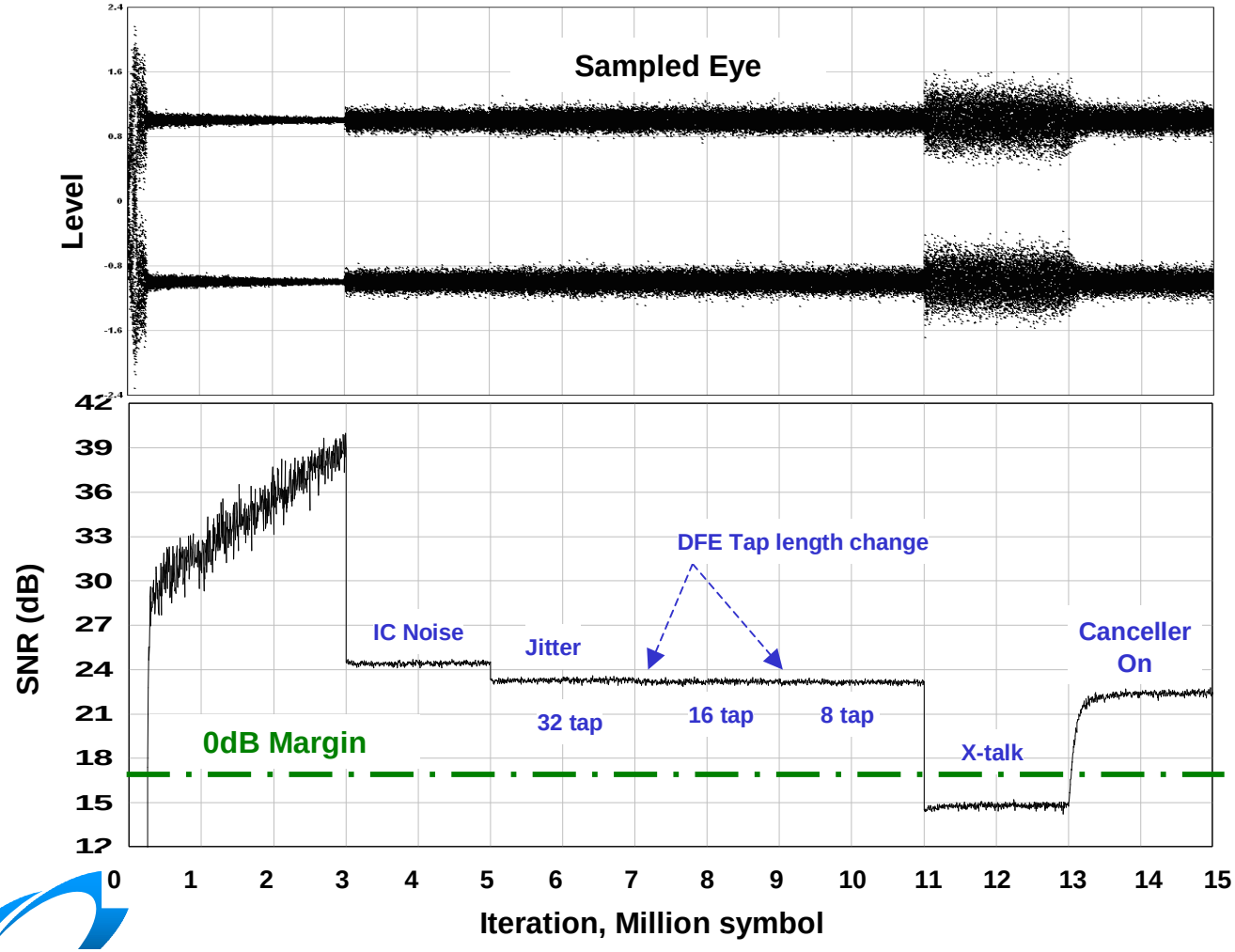
Passive Module 40G, 10G x 4-Lane



Noise Margin:

-2.1dB

(w/o canceller)

5.4dB

(w canceller)

Noise Margin Summary

		Salz Margin	Result of Time Domain Sim.		
			Basic Structure	Crosstalk Canceller	Crosstalk Canceller + FEC
40G	10G x 4 KR-4	12.4dB	6.8dB	8.4dB	12.4dB
		1.7dB	-2.1dB	5.4dB	9.4dB
100G	10G x 10 KR-10	8.2dB	3.7dB	8.1dB	12.1dB
	25G x 4 (4PAM)	3.1dB	-3.3dB	-1.2dB	3.8dB

Cable Only : None shaded rows are cable only.

Passive Module : Shaded is with IC Package, PCB and Module crosstalk

Summary

Performance is estimated for 40/100G copper interconnect based on the measured channel data.

1st Step: Signaling selection is made from the Salz SNR based on measured crosstalk (Cable and Module assembly) and IC electronic noise.

2nd Step: Check Jitter and other IC implementation loss by the time domain simulator

Estimated Noise Margin (10m-24G Twinaxial cable)

1. **6.8dB for 40G 4-Lane system based on KR-4 (NRZ-2PAM),**
2. **3.7dB for 100G 10-Lane system based on KR-10 (NRZ-2PAM) and 8.1dB with crosstalk canceller,**
3. **3.8dB for 100G 4-Lane system based on 25G x 4PAM,13Gbaud with crosstalk canceller and FEC.**
4. **Need crosstalk canceller and/or FEC for passive module even for 40G system.**

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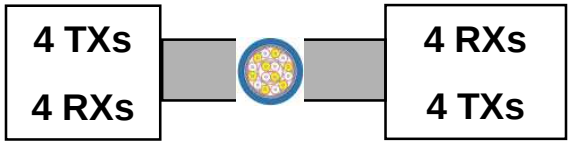
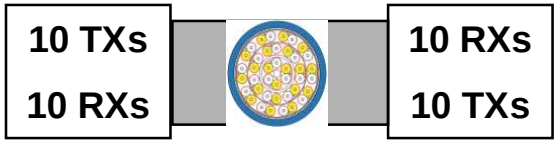
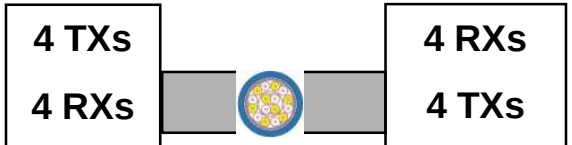
Back Up

Complexity Comparison

	Configuration	TX	RX	Upgrade from 40G
10G x 4 KR-4	 8 pairs	▪10 Gbaud ▪THD: ~23dB ▪Jitter: 0.15UI-pp	▪4~8-tap FFE ▪8-tap DFE	----
10G x 10 KR-10	 20 pairs	▪10 Gbaud ▪THD: ~23dB ▪Jitter: 0.15UI-pp	▪4~8-tap FFE ▪8-tap DFE ▪Crosstalk Canceller	May require major PMD re-architecture New connectors & Modules with reduced crosstalk (No work has been done yet)
25G x 4 (4PAM)	 8 pairs	▪12.5 Gbaud ▪THD: ~28dB ▪Jitter: 0.15UI-pp	▪4~8-tap FFE ▪8-tap DFE ▪Crosstalk Canceller ▪One FEC for 4 lanes	No major re-architect necessary Increase clock frequency by 20~30%

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Passive Module reduces number of PHYs down to half.