OTN mapping of MLD LAN Interfaces and thoughts on MLD stack

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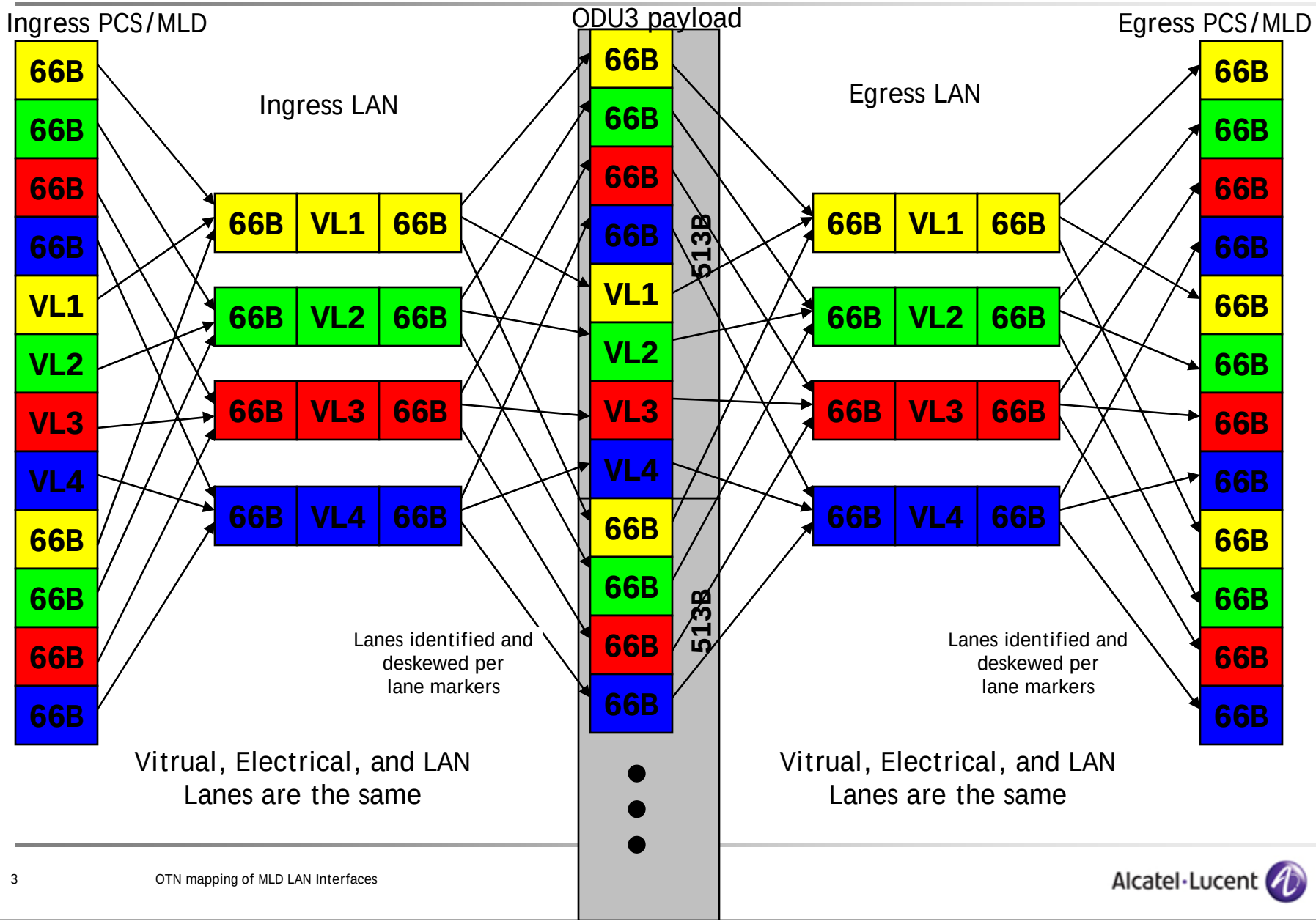
Conclusions from trowbridge_01_0108

- The logical serial LAN format that would follow from the MLD architecture is a bit-mux of virtual lanes rather than a sequence of 66B blocks.
  - For parallel LAN, deskew is likely needed at the OTN ingress which requires recovery of 66B blocks
  - 66B blocks must also be recovered to perform transcoding for 40 GbE into ODU2
  - Option B2 appears to best meet the needs for a common method for OTN transport of parallel or serial 40 GbE and 100 GbE

- Option B2 – Deskew the LAN virtual lanes at the OTN ingress (requires demuxing virtual lanes and recovering 64B/66B on each virtual lane). Remultiplex into a serial stream by assembling the 66B blocks in correct temporal order, resulting in a bitstream that looks like 10G Base-R but faster. At the OTN egress, demux the 66B blocks into 20 virtual lanes, remux bitwise into the required number of LAN lanes.

Four lane 40 GbE interface over OTN



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Transcodable Virtual Lane Markers

Required for 40 GbE

- 512B/513B Transcoding proposal requires 16 or fewer control block types to be used in underlying 64B/66B code
- 10G Base-R 64B/66B coding uses 15 control block types
- 40G/100G may use fewer control block types if packet and ordered set start is restricted to an 8-byte boundary
- A single control block type can be used to encode a lane marker, with 56 bits available for a very sparse coding of the lane number
- Control blocks are restored to their original temporal position in the 64B/66B stream when the 513B blocks are decoded

Changes to 64B/66B for 40 GbE and 100 GbE given 8-byte boundary for packet start and ordered sets

Ordered sets can't start in 5th lane

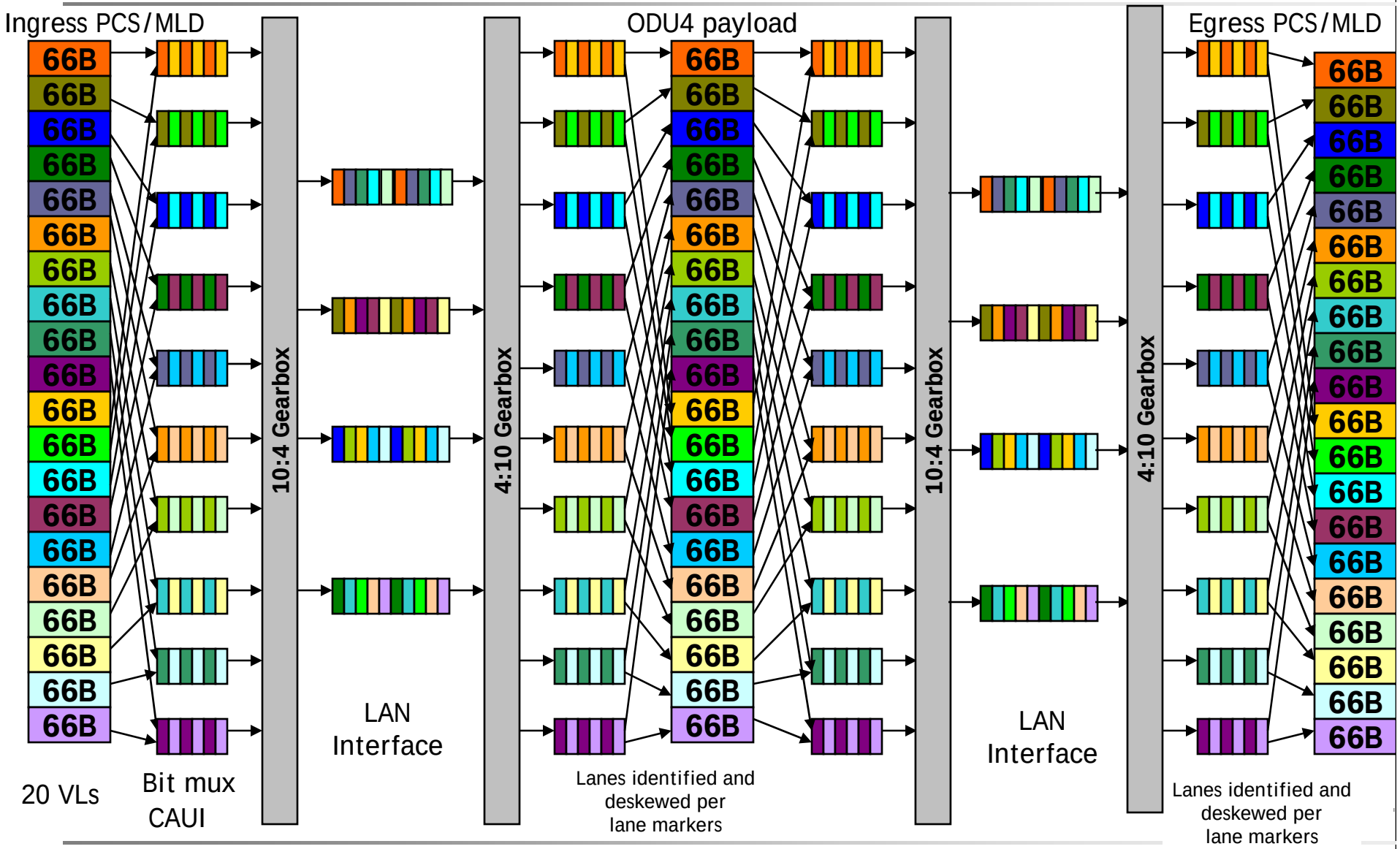
Packets can't start in 5th lane

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 49–7—64B/66B block formats

Four-Lane 100 GbE LAN interface over OTN

Keep lane markers in sequence of 66B blocks



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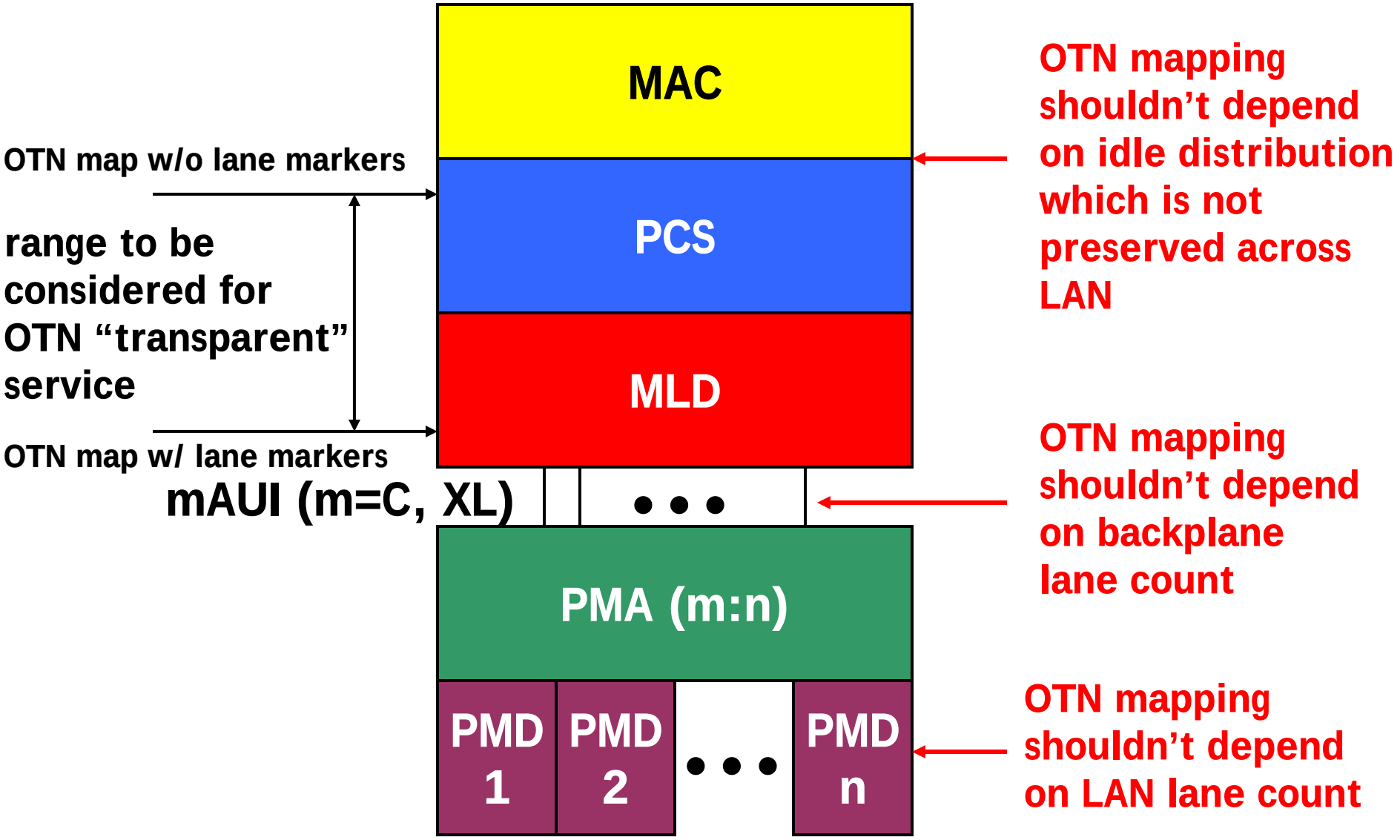
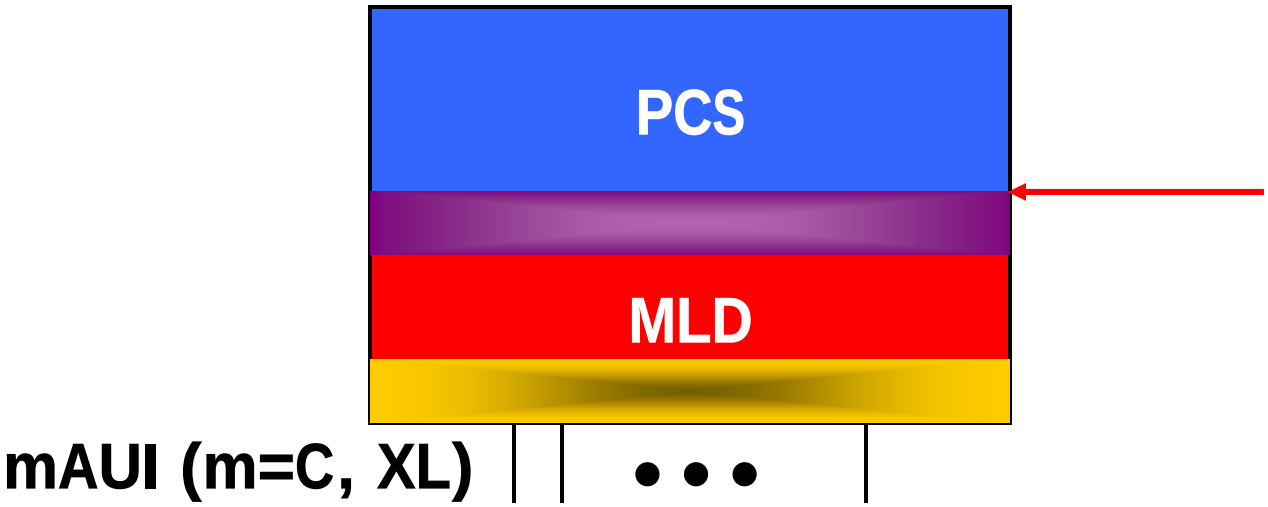
Reference Architecture for assessing OTN "transparency"

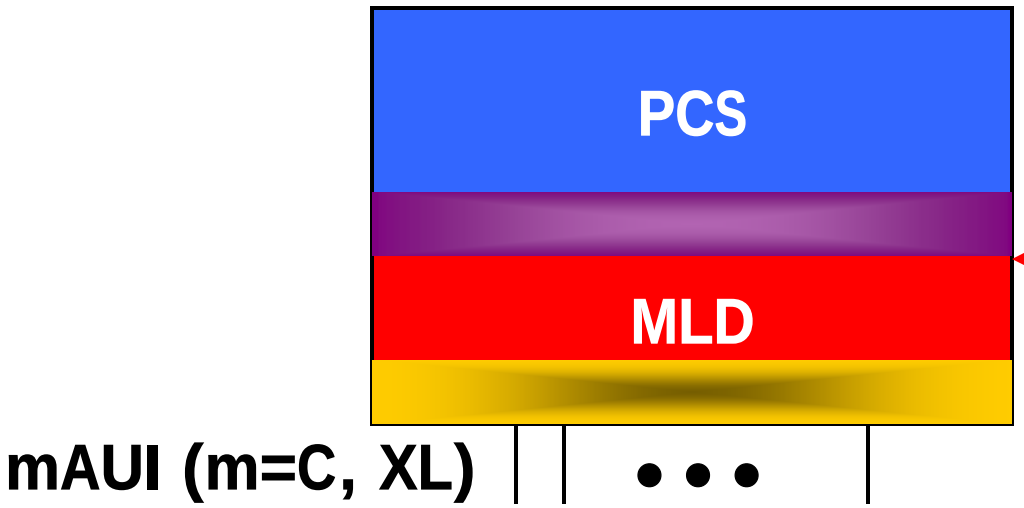


Fuzzy edges between blocks



No “pure” PCS since rate-adapt FIFO used to create space for lane markers (i.e., there is no 103.125Gbit/s or 41.25 Gbit/s stream of 64B/66B encoded MAC data only

Fuzzy edges between blocks



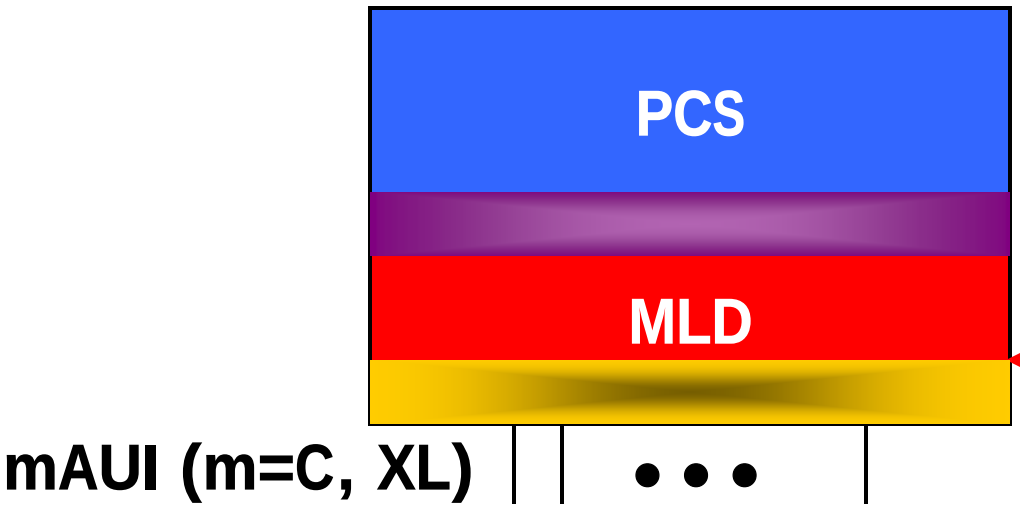
Logical sequence of 66B encoded MAC data can be described, but there may not be a physical realization since the rate adapt FIFO will just be held up for the interval when lane markers are being inserted

41.2474823 Gbit/s of 66B encoded MAC data for 40 GbE

103.1187057 Gbit/s of 66B encoded MAC data for 100 GbE

assuming lane markers every 16K blocks

Fuzzy edges between blocks

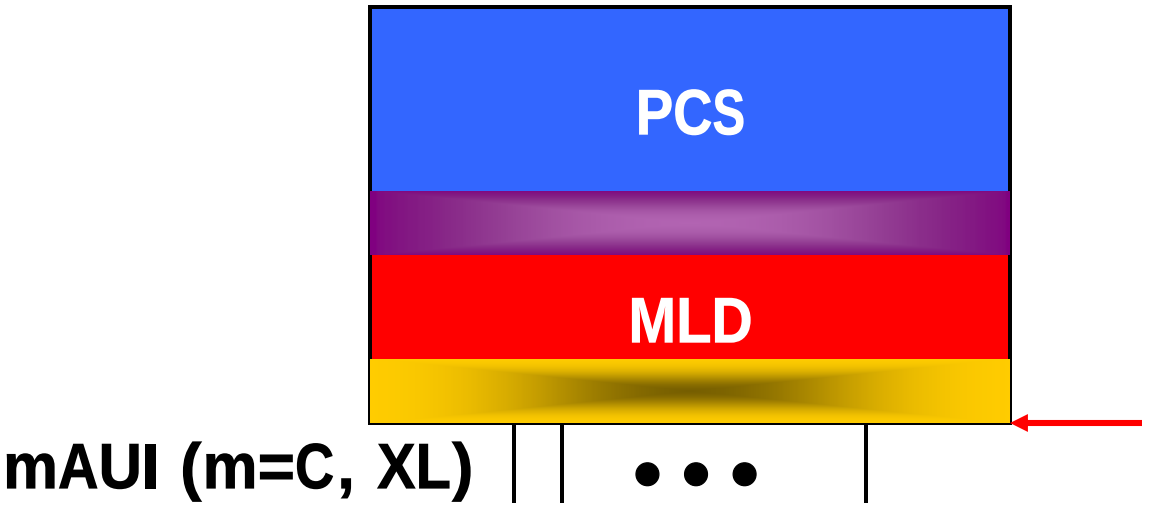


After insertion of lane markers, there exists a set of virtual lanes that sums to the expected PCS encoded bit-rate. But this is a logical sequence that still may not correspond to a physical interface (possible exception for the "degenerate" case of 40 GbE where the number of virtual and physical lanes are the same

41.25 Gbit/s of 66B encoded data with lane markers for 40 GbE

103.125 Gbit/s of 66B encoded data with lane markers for 100 GbE

Fuzzy edges between blocks



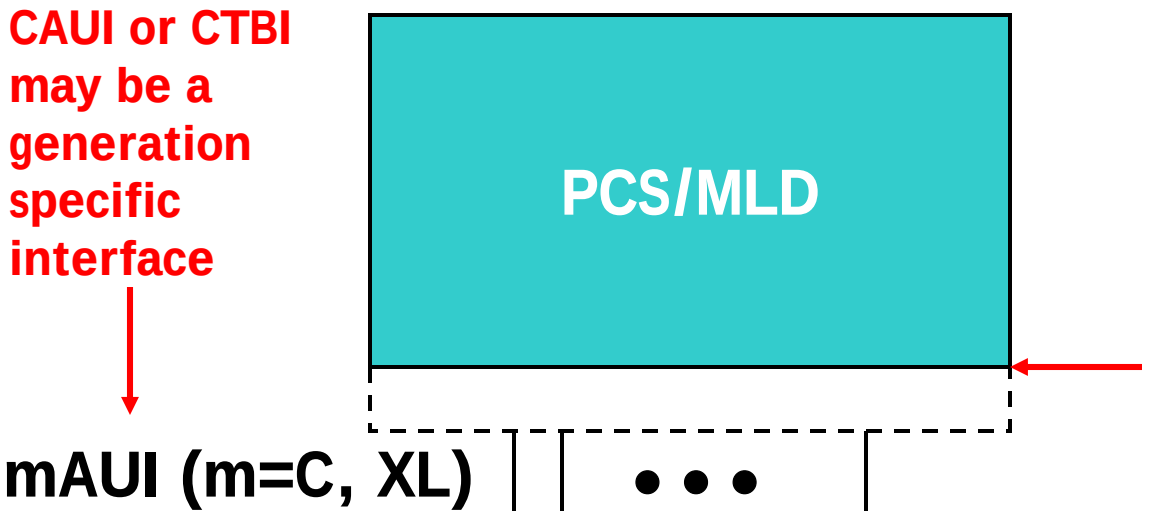
mAUI gets to something that may be physical, but not necessarily the same from 1st to 2nd generation.

LXAUI = 4 lanes of 10.3125 Gbit/s, each carrying one VL of 66B encoded data

1st gen CAUI = 10 lanes of 10.3125 Gbit/s, each carrying two bit-muxed VLs, each VL 66B encoded

2nd gen CAUI (based on OIF CEI25/28G?) could be 4 lanes of 25.78125 Gbit/s, each carrying five bit-muxed VLs, each VL 66B encoded

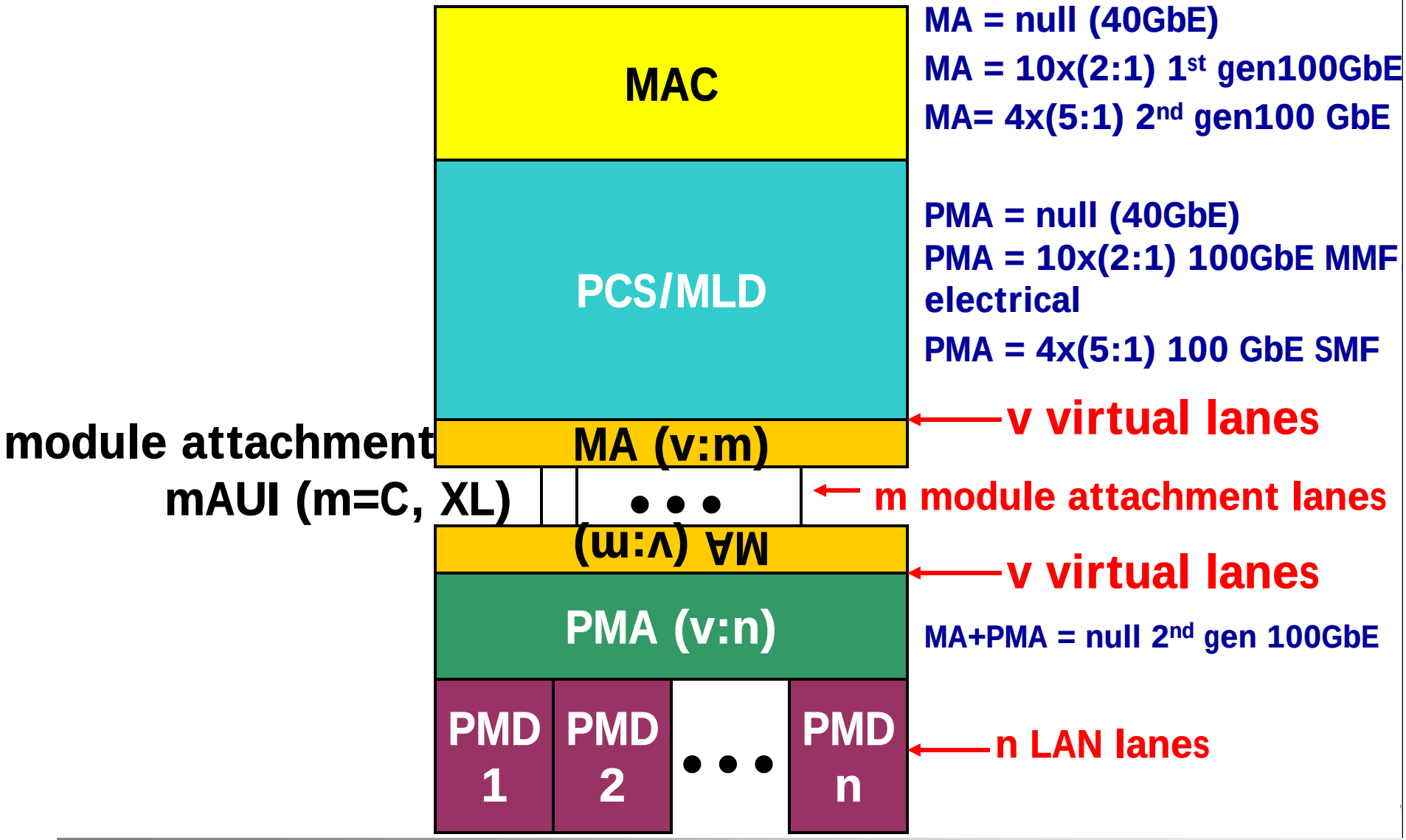
Fuzzy edges between blocks



LXVL = 4 virtual lanes of 10.3125 Gbit/s, 66B encoded

CVL = 20 virtual lanes of 5.1575 Gbit/s, 66B encoded

Possible MLD stack, resilient across technology generations



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Conclusions

- It continues to appear that the most likely OTN mapping involves deskew of virtual lanes at OTN ingress and reconstruction of serialized sequence 66B blocks for OTN transport
- Performing multiple functions with the same FIFO may make it difficult to separate PCS and MLD architecturally
- Specifying logical interface for virtual lanes at an architectural boundary may allow specification in a way that doesn't change across generations of the technology