Table 87–8—40GBASE–LR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	10.3125 ± 100 ppm	GBd
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5	nm
Damage threshold[a] (min)	3.3	dBm
Average receive power, each lane (max)	2.3	dBm
Average receive power, each lane[b] (min)	–13.7	dBm
Receive power, each lane (OMA) (max)	3.5	dBm
Difference in receive power between any two lanes (OMA) (max)	7.5	dB
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA), each lane[c] (max)	–11.5	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	12.3	GHz
Stressed receiver sensitivity (OMA), each lane[d] (max)	–9.6	dBm
Conditions of stressed receiver sensitivity test:		
Vertical eye closure penalty[e], each lane	1.9	dB
Stressed eye J2 Jitter[e], each lane	0.3	UI
Stressed eye J9 Jitter[e], each lane	0.47	UI

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
[b]Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA), each lane (max) is informative.
[d]Measured with conformance test signal at TP3 (see 87.8.11) for BER = 10^{-12}.
[e]Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter, are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

87.8.11 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 87–8 for 40GBASE–LR4 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2. The BER is required to be met for the lane under test on its own.

For each lane, the stressed receiver sensitivity is defined with the transmit section in operation on all four lanes and with the receive lanes not under test also in operation. Pattern 3 or Pattern 5, or a valid 40GBASE–

Table 87–9—40GBASE–LR4 illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDP)	9.3	dB
Operating distance	10	km
Channel insertion loss[a]	6.7	dB
Maximum discrete reflectance	–26	dB
Allocation for penalties[b] (for max TDP)	2.6	dB
Additional insertion loss allowed	0	dB

[a]The channel insertion loss is calculated using the maximum distance specified in Table 87–6 and cabled optical fiber attenuation of 0.47 dB/km at 1264.5 nm plus an allocation for connection and splice loss given in 87.11.2.1.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

R signal is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

87.8.11.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 87–3. The patterns used for testing the receiver are specified in Table 87–11. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 87.8.11.2, and has sinusoidal jitter applied as specified in . A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics.

The low pass filter is used to create ISI-induced vertical eye closure penalty (VECP). The low pass filter, when combined with the E/O converter, should have a frequency response which results in the appropriate level of initial vertical eye closure before the sinusoidal terms are added.

The sinusoidal amplitude interferer 1 causes jitter which is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The ~~sinusoidally~~ sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal ~~jitter~~jitter, the signaling rate and the pattern repetition rate. The Guassian noise generator, the amplitude of the sinusoidal jitter and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J9 Jitter specifications given in Table 87–8 are simultaneously met.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized. ~~Random noise effects, such as RIN and random clock jitter, should also be minimized. Some residual noise and jitter from all sources is unavoidable, but more than 0.25 UI peak-to-peak jitter at the 10^{-12} points is not acceptable. If this is achieved, then pattern dependent effects should be minimal, and short patterns can be used for calibration with the benefit of providing better trace visibility on sampling oscilloscopes.~~

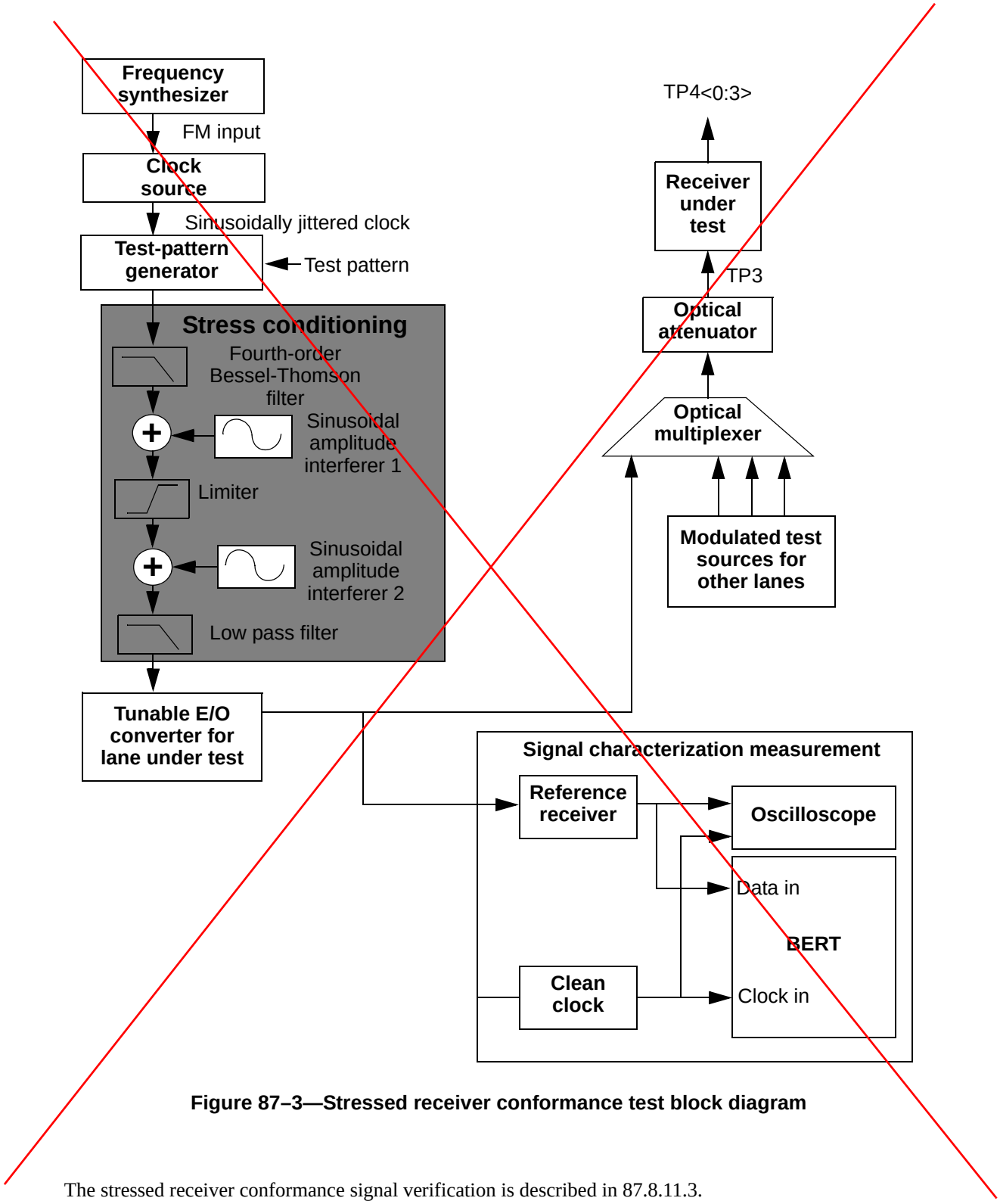

Figure 87–3—Stressed receiver conformance test block diagram

The stressed receiver conformance signal verification is described in 87.8.11.3.

87.8.11.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver of the lane under test meets BER requirements with near worst case waveforms at TP3.

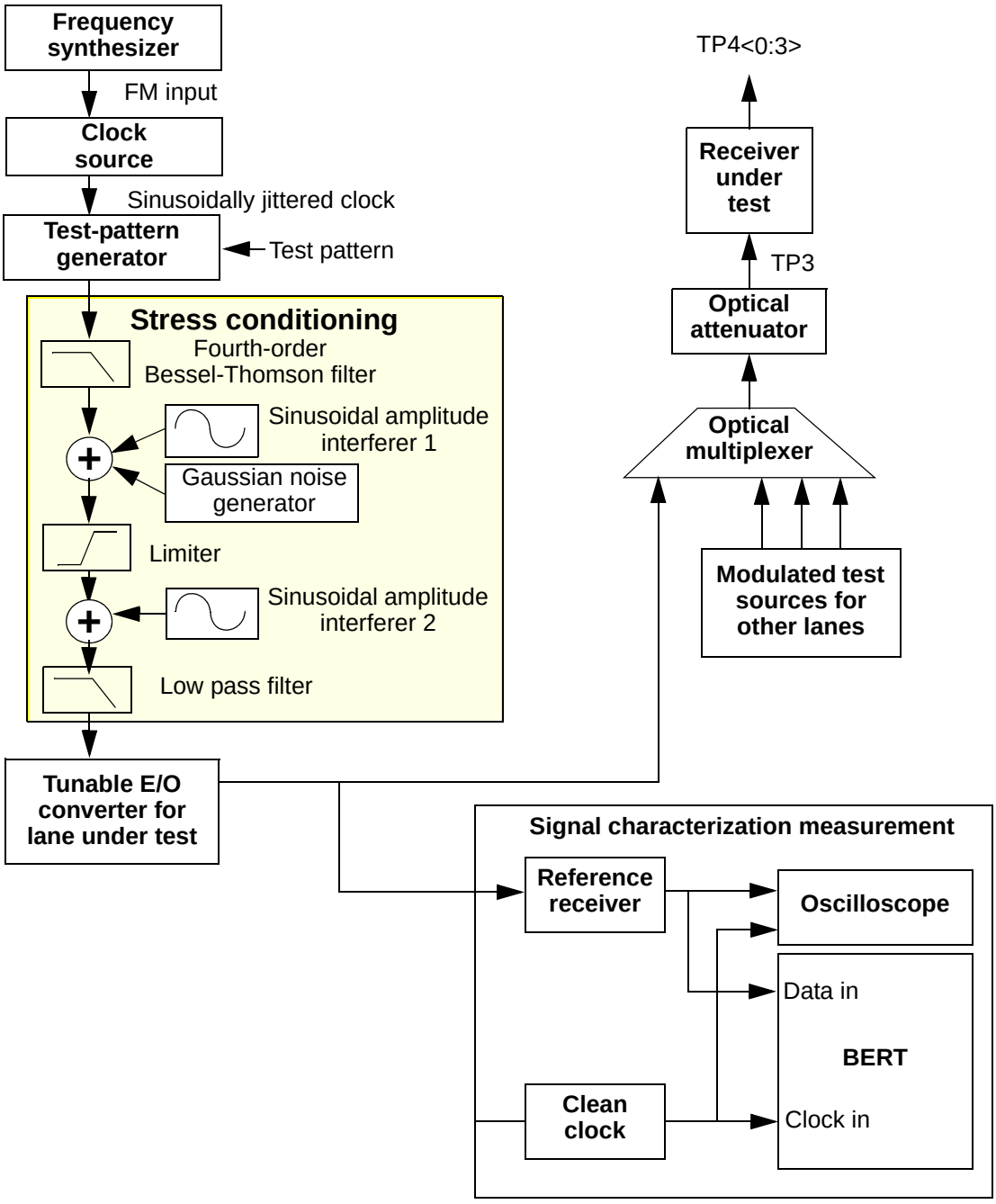

Figure 87–3—Stressed receiver conformance test block diagram

The primary parameters of the conformance test signal are vertical eye closure penalty (VECP) and stressed eye J2 Jitter ~~(SEJ)~~and stressed eye J9 Jitter. VECP is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as defined in 52.9.7). The ~~SEJ~~ stressed eye J2 Jitter is defined as the time interval that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram and is measured at the average optical power, which can be

obtained with AC coupling. J9 Jitter is defined in 86.8.3.3.2. The values of these components are defined by their histogram results.

The vertical eye closure penalty is given by Equation (87–1).

$$\text{Vertical eye closure penalty} = 10\log_{10}\frac{OMA}{A_O} \quad \text{(dB)} \qquad (87\text{–}1)$$

where:

A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram, and

OMA is the optical modulation amplitude as defined in 87.8.5.

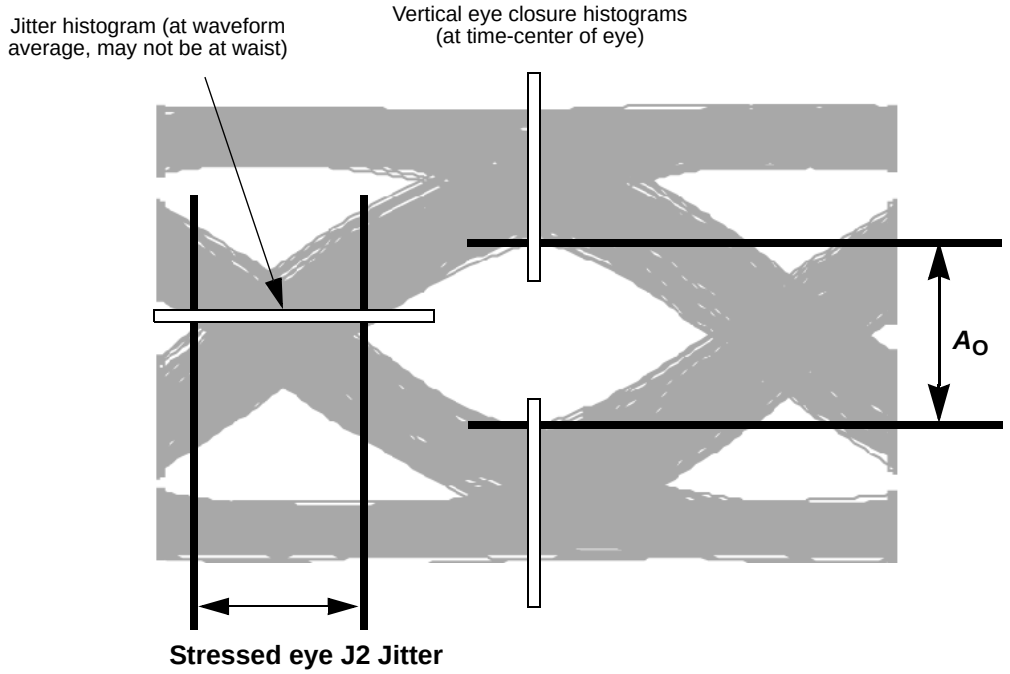

Figure 87–4—Required characteristics of the conformance test signal at TP3

An example stressed receiver conformance test set up is shown in Figure 87–3, however, any approach that modulates or creates the appropriate levels and frequencies of the VECP and jitter components is acceptable.

Residual low-probability noise and jitter should be minimized so that the outer slopes of the final amplitude histograms are as steep as possible.

The following steps describe a possible method for setting up and calibrating a stressed eye conformance signal when using a stressed receiver conformance test set up as shown in Figure 87–3:

1) Set the signaling rate of the test pattern generator to meet the requirements in Table 87-7.
2) With sinusoidal interferers and sinusoidal jitter turned off, set the extinction ratio of the E-O to approximately the minimum specified in Table 87-7.
3) The required values of vertical eye closure ~~penalty~~ penalty, stressed eye J2 Jitter, and stressed eye ~~J2~~ J9 Jitter of the stressed receiver conformance signal are given in Table 87–8.

With the sinusoidal interferers and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the low pass filter. Any remaining VECP must be created with sinusoidal interferer 2 or sinusoidal jitter.

The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate and the pattern repetition rate.

Sinusoidal jitter is added as specified in Table 87–13. When calibrating the conformance signal, the sinusoidal jitter frequency should be well within the 4 MHz to 10 times LB as defined in Table 87–13 and illustrated in Figure 87–5.

Iterate the adjustments of sinusoidal ~~interferers~~ interferers, Gaussian noise generator, and sinusoidal jitter until the values of ~~VECP~~ VECP, stressed eye J2 Jitter, and ~~SEJ~~ stressed eye J9 Jitter, simultaneously meet the requirements in Table 87–8, and sinusoidal jitter above 4 MHz is as specified in Table 87–13. The resulting stressed eye conformance signal is required to have at least 0.05 UI of pulse width shrinkage.

Figure 87–3 shows the stress conditioned signal being applied to a tunable E-O convertor. However, any optical source may be used which can meet the OMA and wavelength requirements for the lane under test as described in 87.8.11.5. Similarly, the other test sources which supply modulated signals to the other lanes may use any tunable or fixed sources which meet the OMA and wavelength requirements described in 87.8.11.5.

Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the stressed receiver sensitivity OMA specified in Table 87–8, and the test sources for the other lanes are set to the required OMA and wavelength as described in 87.8.11.5.

87.8.11.3 Stressed receiver conformance test signal verification

The stressed receiver conformance test signal can be verified using an optical reference receiver with an ideal fourth-order Bessel-Thomson response with a reference frequency f_r of 7.5 GHz. Use of G.691 tolerance filters may significantly degrade this calibration. The clock output from the clock source in Figure 87–3 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye J2 Jitter and stressed eye J9 Jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 87–3) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system will result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O-E, filters and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this document, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 87.8.11.2 and 87.8.11.4.