

100/40Ge PMA Proposal

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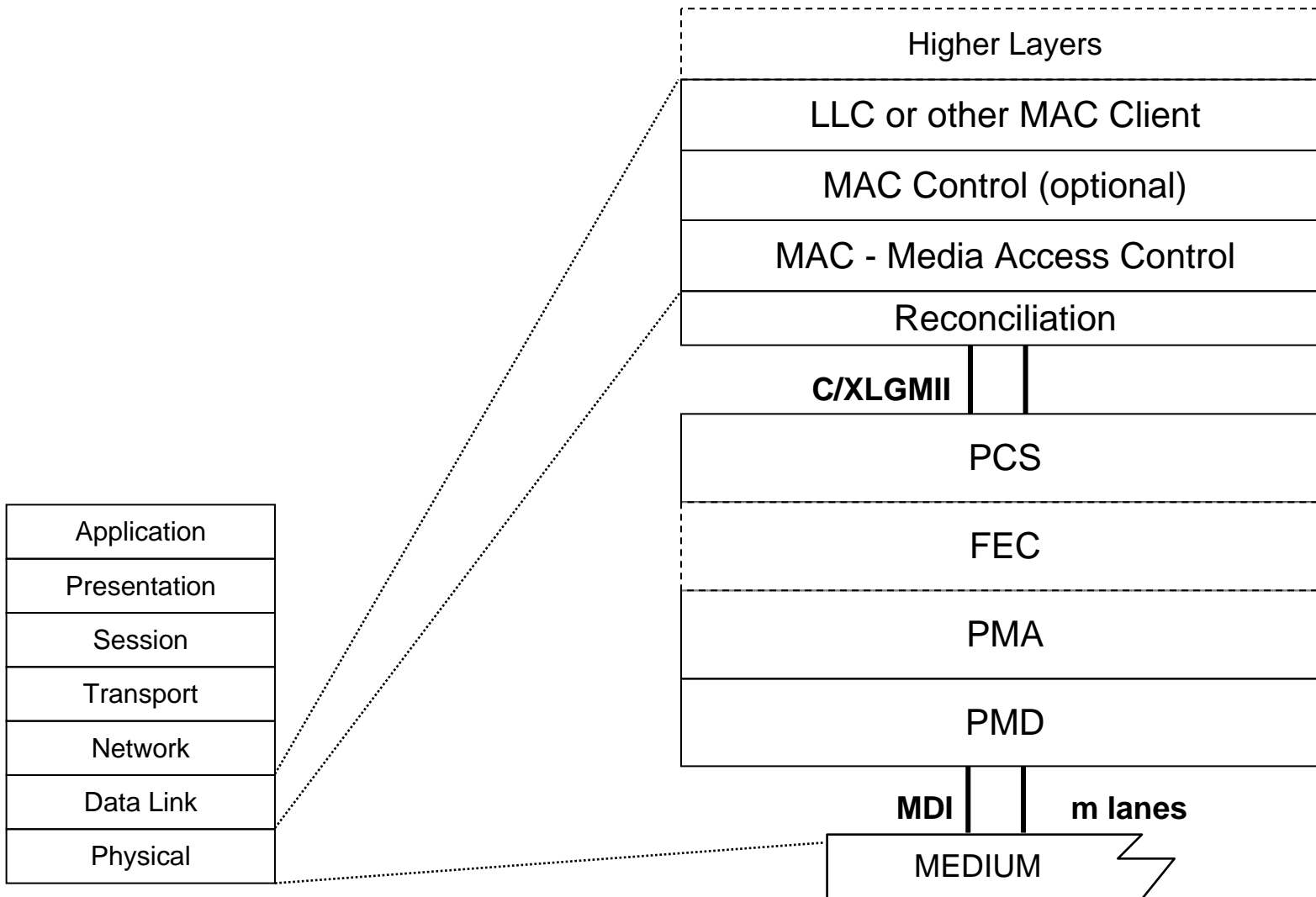
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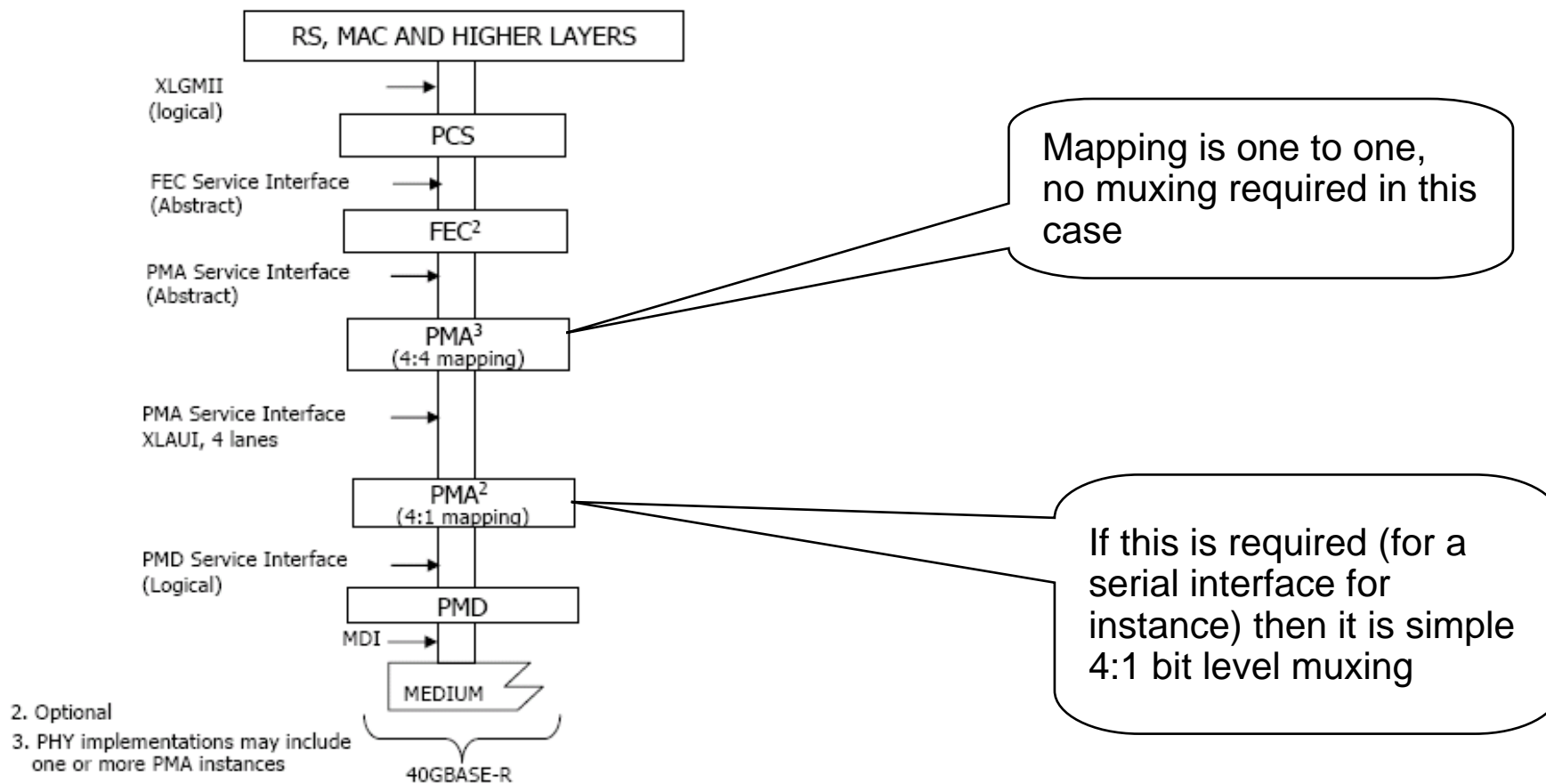
Overview

- This is a proposal for the logical portion on the PMA for 100GE and 40GE
- It does not cover the electrical interfaces (CAUI/XLAUI)

40GE/100GE Generic Architecture

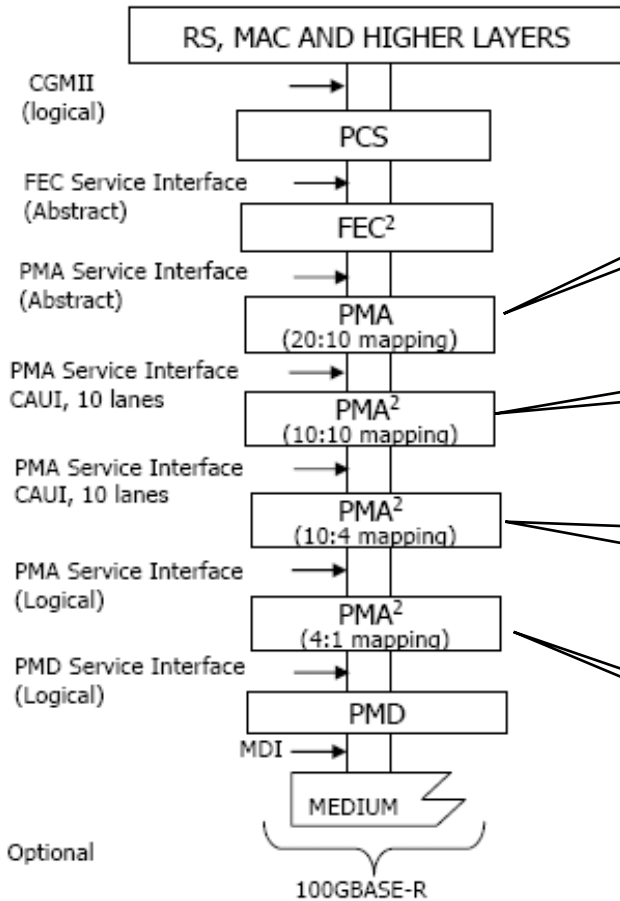


40GE PMA Variants



From ganga_01_0508

100GE PMA Variants



Note: 2. Optional

From ganga_01_0508

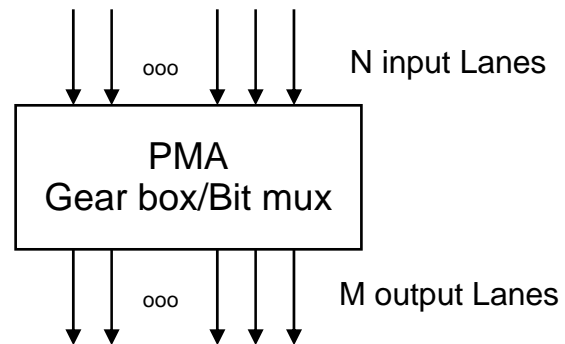
Mapping is two to one, Simply done at the bit level with 2:1 muxes.

Mapping is one to one, no muxing required in this case

If this is required (for the single mode interface for example) then it is 10:4 gearbox. It could also be implemented as 2x 5:2 muxes

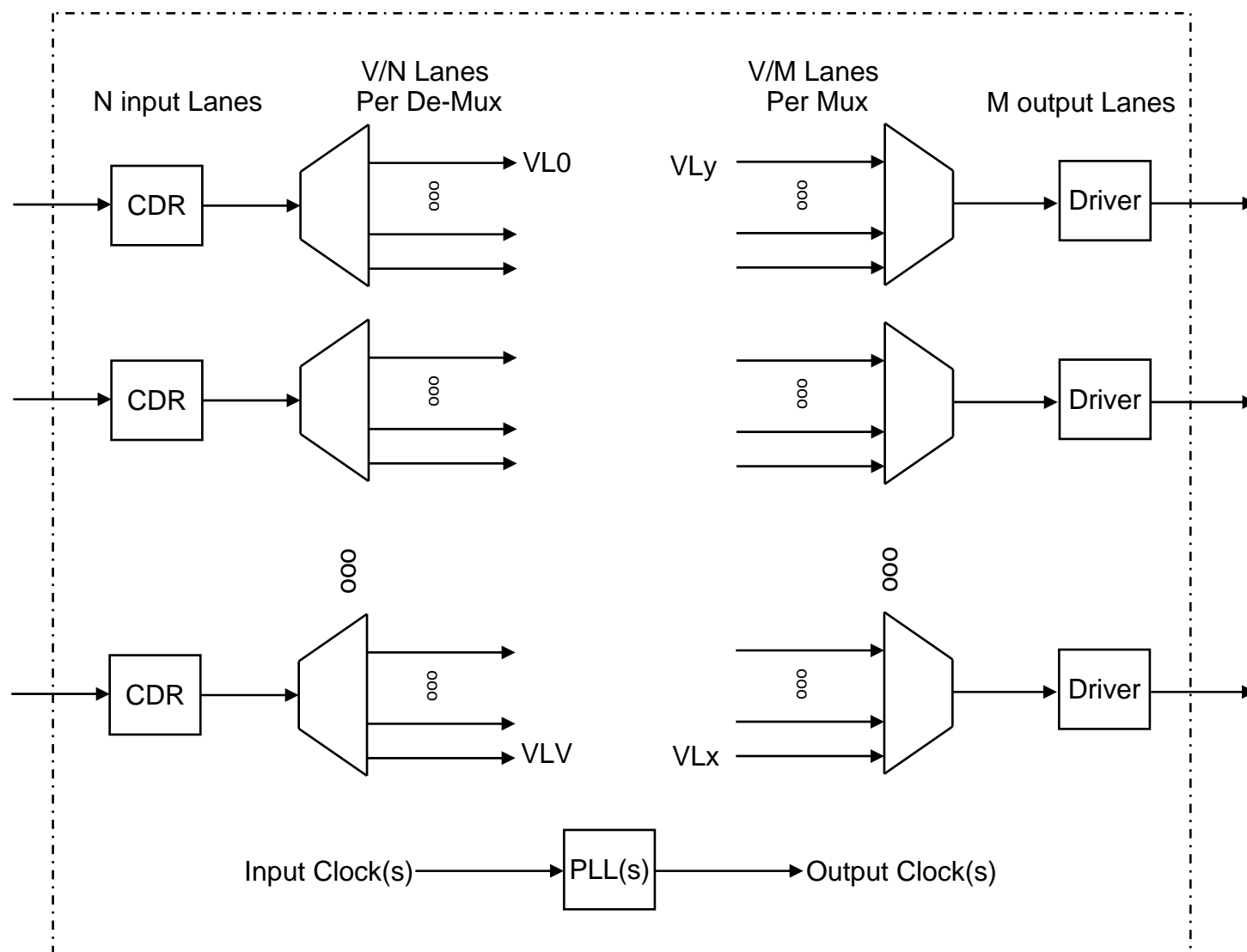
If this is required (for a future serial interface for example) then it is a 4:1 mux.

A Parameterized PMA



- V is the number of Virtual Lanes
- N input lanes, each with V/N virtual lanes
- M output lanes, each with V/M output lanes
- The muxing/gearboxing follows the rules as stated later in this presentation

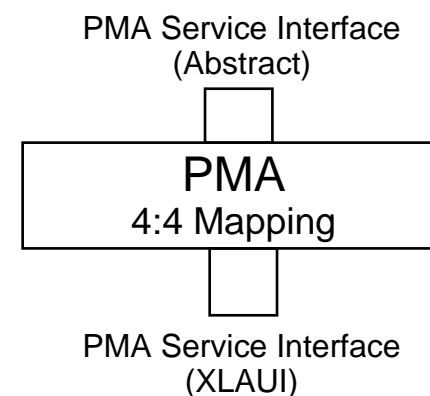
A Parameterized PMA - Details



Note that implementations do not necessarily need to demux the VLs, instead direct gearboxing can be used.

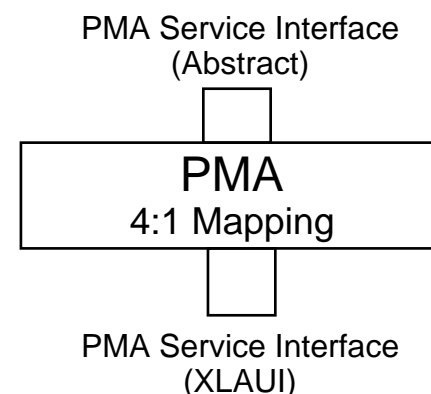
40GE PMA Variant #1

- In the transmit direction the following is provided:
 1. Direct 1:1 mapping of the interface.
 2. Transmission of parallel data to PMD.
- In the receive direction the following is provided:
 1. Direct 1:1 mapping of the interface
 2. Transmission of parallel data to PMA client.
 3. Provide link status information.



40GE PMA Variant #2

- In the transmit direction the following is provided:
 1. Bit level multiplexing of the 4 input lanes into a single output lane
 2. Provide a clock source to the PMA client.
 3. Transmission of serial data to the PMD.
- In the receive direction the following is provided:
 1. Reception of serial data from the PMD
 2. Provides receive clock to PMA client
 3. Bit level de-multiplexing of the serial data into four output lanes
 4. Transmission of parallel data to PMA client.
 5. Provide link status information.



PSI 0	PSI 1	PSI 2	PSI 3
8	9	10	11
4	5	6	7
0	1	2	3

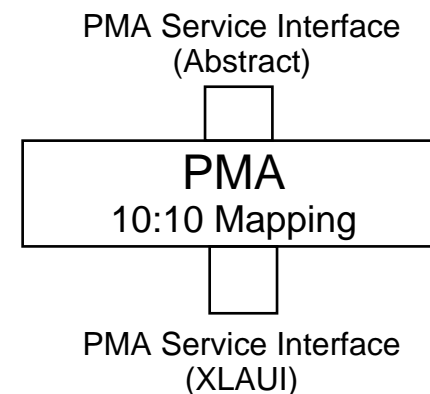
Serial I/F

5
4
3
2
1
0

One possible bit muxing order. PSI = PMA Service Interface

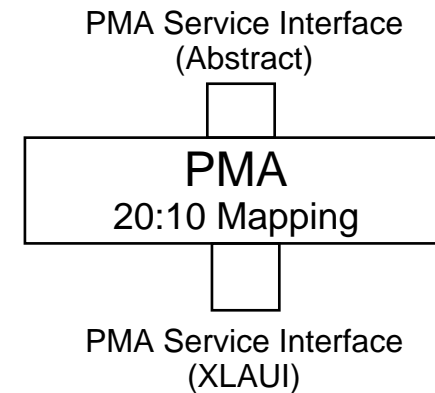
100GE PMA Variant #1

- In the transmit direction the following is provided:
 1. Direct 1:1 mapping of the interface.
 2. Transmission of parallel data to PMD.
- In the receive direction the following is provided:
 1. Direct 1:1 mapping of the interface
 2. Transmission of parallel data to PMA client.
 3. Provide link status information.



100GE PMA Variant #2

- In the transmit direction the following is provided:
 - Bit level multiplexing of the 20 input lanes into a 10 output lanes
 - Provide a clock source to the PMA client.
 - Transmission of parallel data to the PMD.
- In the receive direction the following is provided:
 - Reception of parallel data from the PMD
 - Bit level de-multiplexing of the 10 input lanes into 20 output lanes
 - Provides receive clock to PMA client
 - Transmission of parallel data to PMA client.
 - Provide link status information.



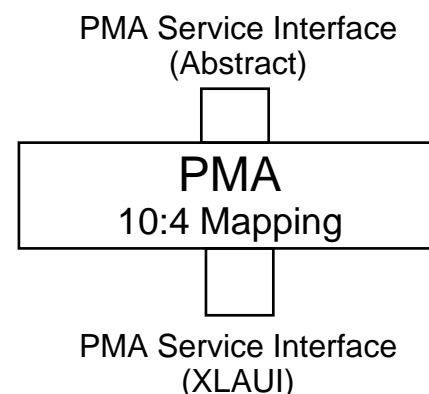
PSI 0	PSI 1	PSI 2	PSI 3	PSI 4	PSI 5	PSI 6	PSI 7	PSI 8	PSI 9	PSI 10	PSI 11	PSI 12	PSI 13	PSI 14	PSI 15	PSI 16	PSI 17	PSI 18	PSI 19
20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

CI 0	CI 1	CI 2	CI 3	CI 4	CI 5	CI 6	CI 7	CI 8	CI 9
30	31	32	33	34	35	36	37	38	39
20	21	22	23	24	25	26	27	28	29
10	11	12	13	14	15	16	17	18	19
0	1	2	3	4	5	6	7	8	9

Here is one bit muxing order. PSI = PMA Service I/F, CI = CAUI I/F. Others are ok also, rx must expect any lane to show up anywhere.

100GE PMA Variant #3

- In the transmit direction the following is provided:
 1. Bit level gearboxing of the 10 input lanes into a 4 output lanes
 2. Provide a clock source to the PMA client.
 3. Transmission of parallel data to the PMD.
- In the receive direction the following is provided:
 1. Reception of parallel data from the PMD
 2. Bit level gearboxing of the 4 input lanes into 10 output lanes
 3. Provides receive clock to PMA client
 4. Transmission of parallel data to PMA client.
 5. Provide link status information.



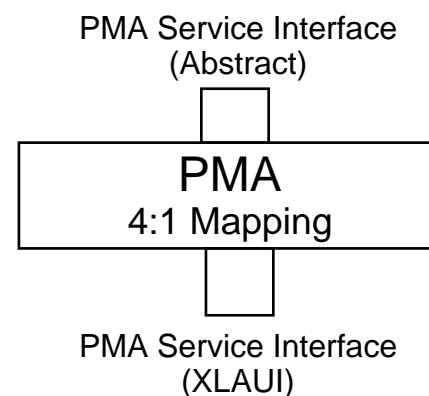
CI 0	CI 1	CI 2	CI 3	CI 4	CI 5	CI 6	CI 7	CI 8	CI 9
30	31	32	33	34	35	36	37	38	39
20	21	22	23	24	25	26	27	28	29
10	11	12	13	14	15	16	17	18	19
0	1	2	3	4	5	6	7	8	9

PI 0	PI 1	PI 2	PI 3
12	13	14	15
8	9	10	11
4	5	6	7
0	1	2	3

Here is one possible bit gearbox order. PI = PMD I/F, CI = CAUI I/F. Others are possible and supportable.

100GE PMA Variant #4

- Same as 40GE PMA variant #2, except for a faster speed
- In the transmit direction the following is provided:
 1. Bit level multiplexing of the 4 input lanes into a single output lane
 2. Provide a clock source to the PMA client.
 3. Transmission of serial data to the PMD.
- In the receive direction the following is provided:
 1. Reception of serial data from the PMD
 2. Bit level de-multiplexing of the serial data into four output lanes
 3. Provides receive clock to PMA client
 4. Transmission of parallel data to PMA client.
 5. Provide link status information.



PSI 0	PSI 1	PSI 2	PSI 3
8	9	10	11
4	5	6	7
0	1	2	3

Serial I/F
5
4
3
2
1
0

One possible bit muxing order. PSI = PMA Service Interface.

A Note on Bit Muxing Requirements

- All PCS receivers must support receiving a virtual lane on any physical lane
 - This allows flexibility now and in the future for how we bit mux and what widths of the interfaces we have today and tomorrow
- This means that there is more than one valid way to multiplex the virtual lanes at all stages
- All are supportable, with the requirement that:
 - When multiplexing from n to m lanes, any given virtual lane is always only sent on one physical lane, which particular lane does not matter
 - On each of M output lanes, every n th bit on a given physical lane must be a given Virtual Lane, where $n = V/M$ (where V = number of total Virtual Lanes)
- With the above multiplexing rules, and with the requirement that the number of virtual lanes is the Least Common Multiple of all the to be supported lane widths, then everything works
 - For 100GE we can support any combination of lane widths of: 20, 10, 5, 4, 2, 1 with 20 VLs
 - For 40GE we can support any combination of lane widths of: 4, 2, 1 with 4 VLs

Summary

- PMA Functions include:
 - Clock and data recovery
 - Bit level multiplexing/gearboxing
 - Clock generation
 - Signal drivers