Proposed Characteristics for 40GBASE-SR4 & 100GBASE-SR10 TP1 & TP4 PMD Service Interfaces

John Petrilla

Avago Technologies

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Supporters

- Ali Ghiasi, Broadcom Corporation
- Petar Pepeljugoski, IBM
- Piers Dawe, Avago Technologies
- Tom Palkert*, Luxtera
- Jonathan King, Finisar

*Contributor and Supporter

Outline

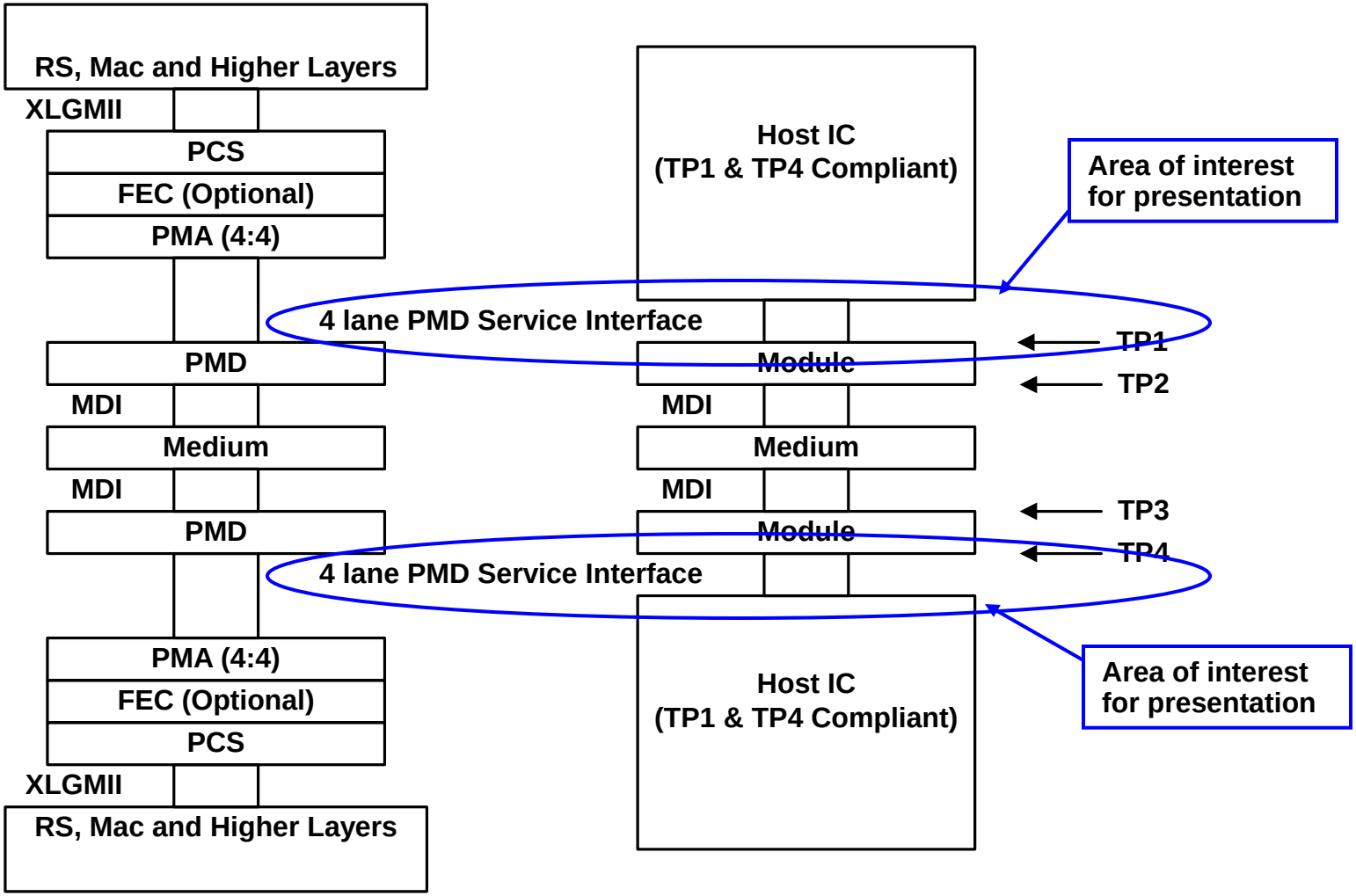
- 802.3ba Alignment
- Elements for success
  - Opportunities for common form factors
- 40GBASE-SR4 & 100GBASE-SR10 Proposal
  - PMD service interface jitter and electrical characteristics
- Conclusions, Recommendations & Next Steps
- References

802.3ba Alignment
802.3ba Objectives Addressed in Presentation

- Support MAC data rates of 40 Gb/s & 100 Gb/s
- Achieve better than or equal to 1E-12 BER at the MAC/PLS Service Interface
- 100 m on OM3 MMF

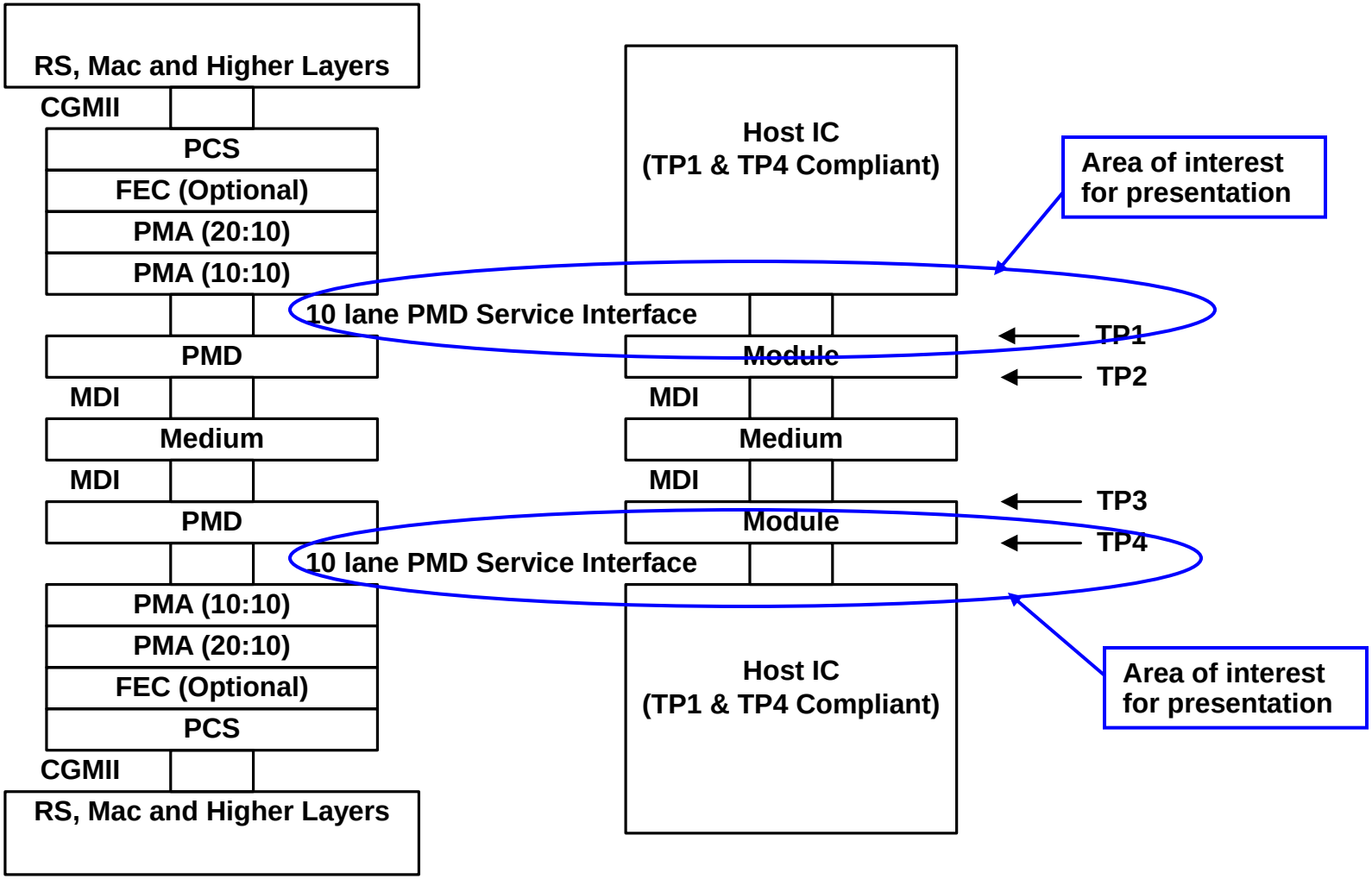
802.3ba Alignment

802.3ba Architectural Layers & Interfaces



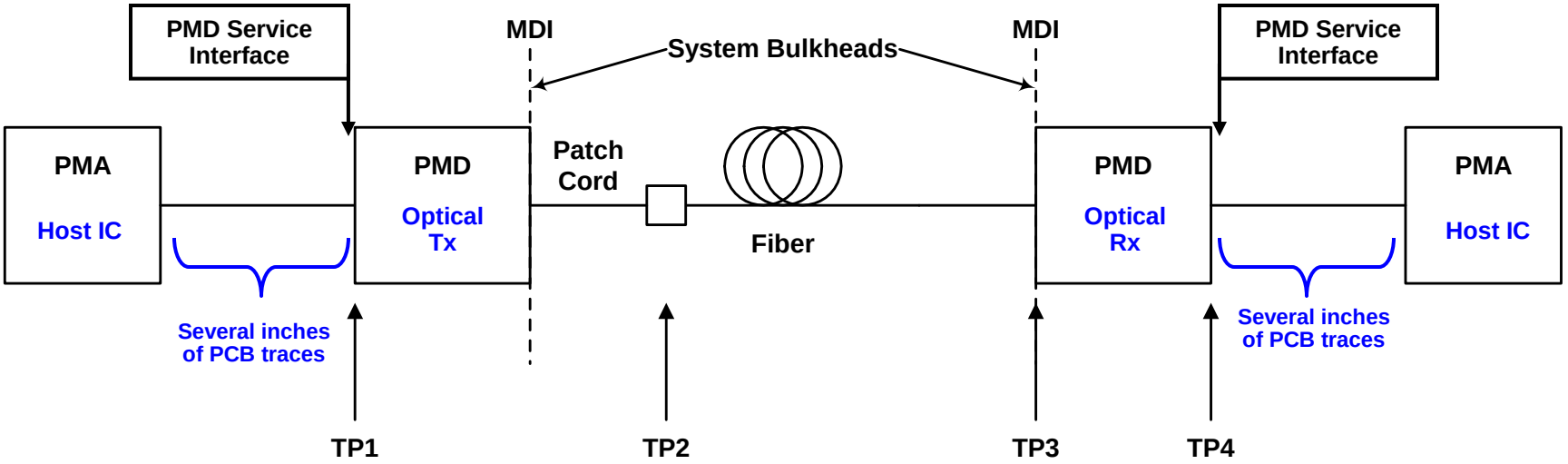
802.3ba Alignment

802.3ba Architectural Layers & Interfaces



802.3ba Alignment

802.3ba PMD Block Diagram

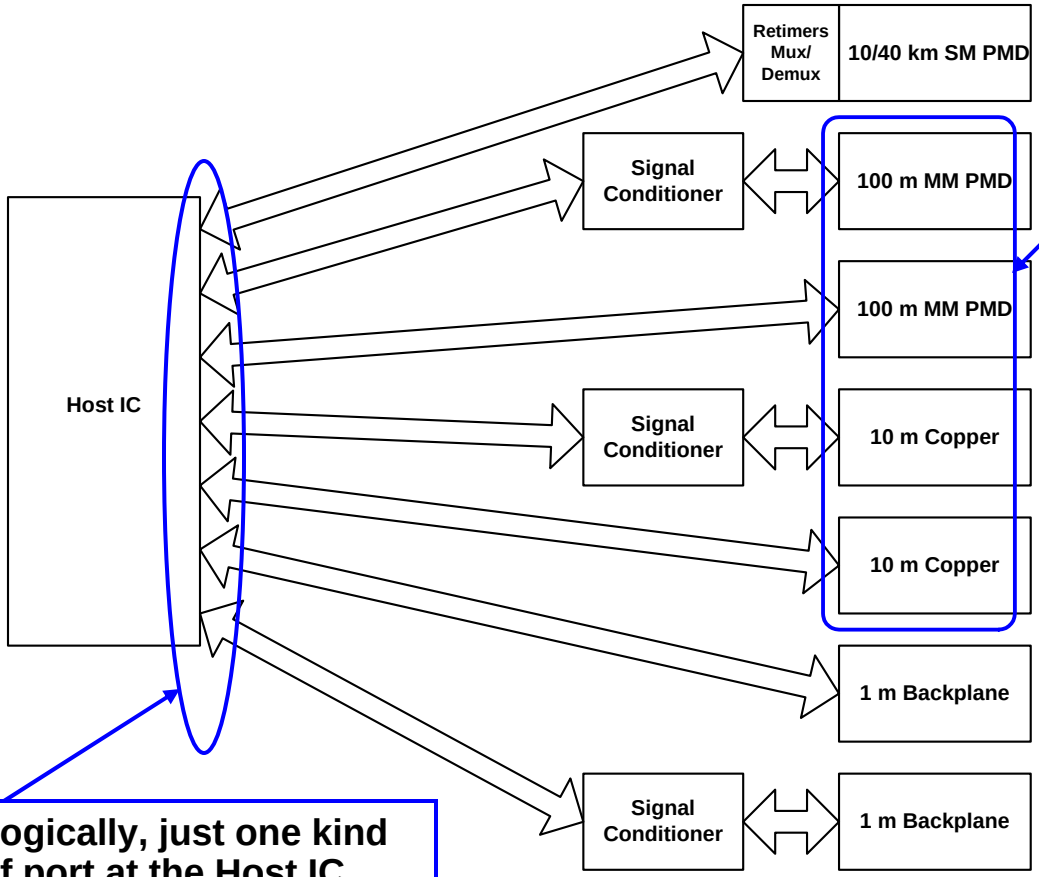


- The above block diagram shows relevant elements and interfaces for an optical link between two PMAs. The patch cord is included for the definition of TP2. Otherwise intermediate fiber connectors are not shown.
- TP1, TP2, TP3 and TP4 are traditional labels for interfaces of a fiber optic link. Here the PMAs may be host ICs and the PMDs, fiber optic modules.
- P802.3ba should fully specify the signals at TP2 and TP3 for optical media and, at least, the jitter allocations at TP1 and TP4 for robust design, as in Gigabit Ethernet. Additional attributes for TP1 and TP4 are herein proposed for consideration, as well as a channel to the host IC. As a set these offer far-end interface targets to host ICs.

Elements for Success
Overview

- Total cost: less than four/ten 10 GbE solutions
  - A pluggable form factor that is common to multiple variants, e.g. copper cable and MM fiber, leads to lower costs by sharing piece parts and footprints and by accelerating market acceptance and increasing volumes. This enables a single build standard for DTE that can be connected by a choice of the two PMD/media types that will dominate the data center. These advantages are compelling and the opportunities should not be overlooked.
- Power consumption: less than four/ten 10 GbE solutions
- High module density: higher than 10 GbE solutions
- Cable plant: 100 m of OM3 & up to 4 intermediate connections
- Reliability: better than ten/four 10 GbE solutions
- Appropriate design points
  - Support ~6 dB channel insertion loss (SDD21 at fundamental frequency) between the host IC and pluggable module without an intermediate connector.
  - Use experience gained in SFP+ (SFF-8431) and 8GFC (FC-PI -4) developments to guide choices for electrical attributes.

Opportunities for a Common Form Factor



Common form factor

- The multilane MM and copper cable variants appear as candidates for a common pluggable form factor due to similarities in size, contact count and power consumption. The SM modules are expected to have ~4x the power consumption of the MM modules.
- Here the term signal conditioner is used to cover all forms of link extenders, CDRs, equalizers, etc.
- It appears reasonable to expect that for some applications the host environment will permit direct connection between a Host IC and the pluggable module or backplane connector. For other environments some form of signal conditioner will be required. Both cases are shown.

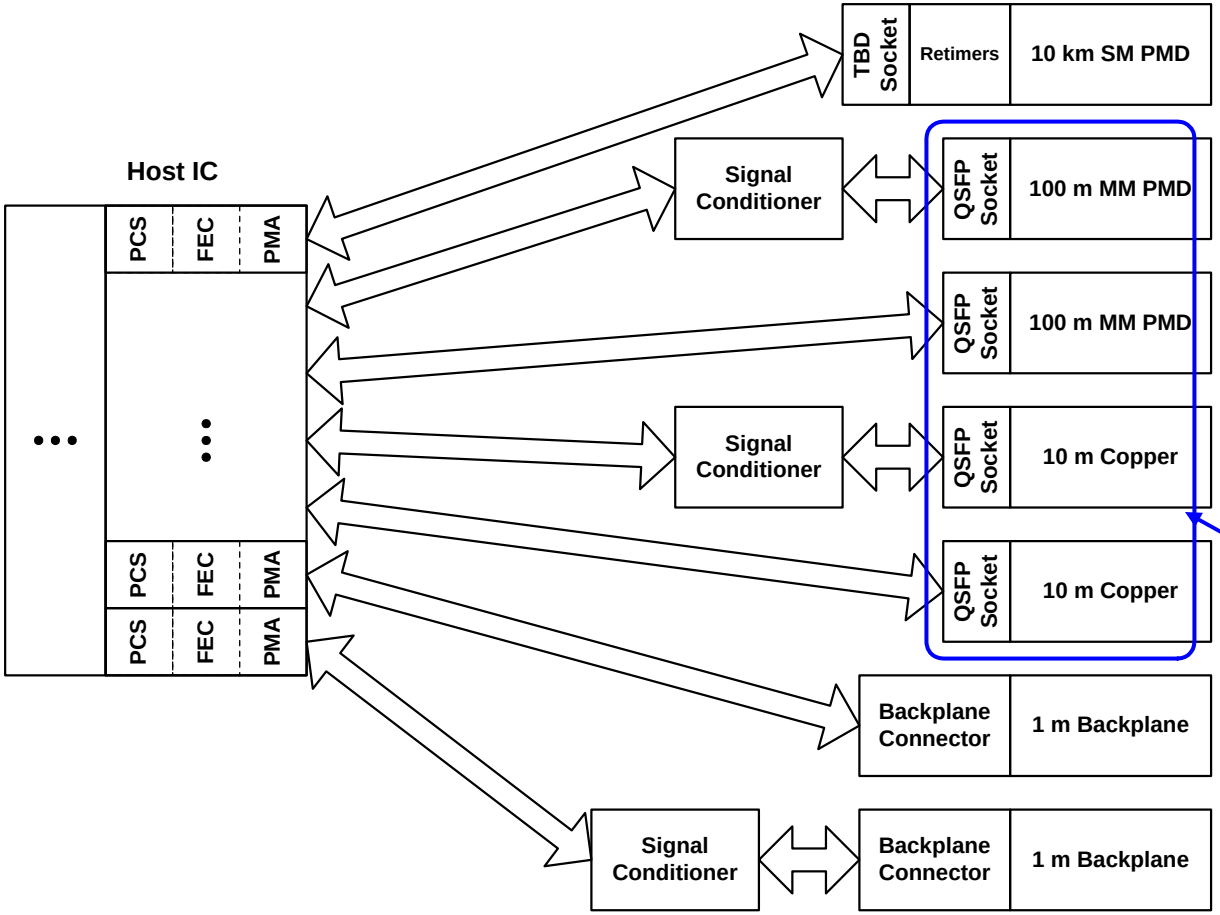
Logically, just one kind of port at the Host IC

Identical functional, logical, digital and management spec

Compatible analog and auto-neg

Opportunities for a Common Form Factor

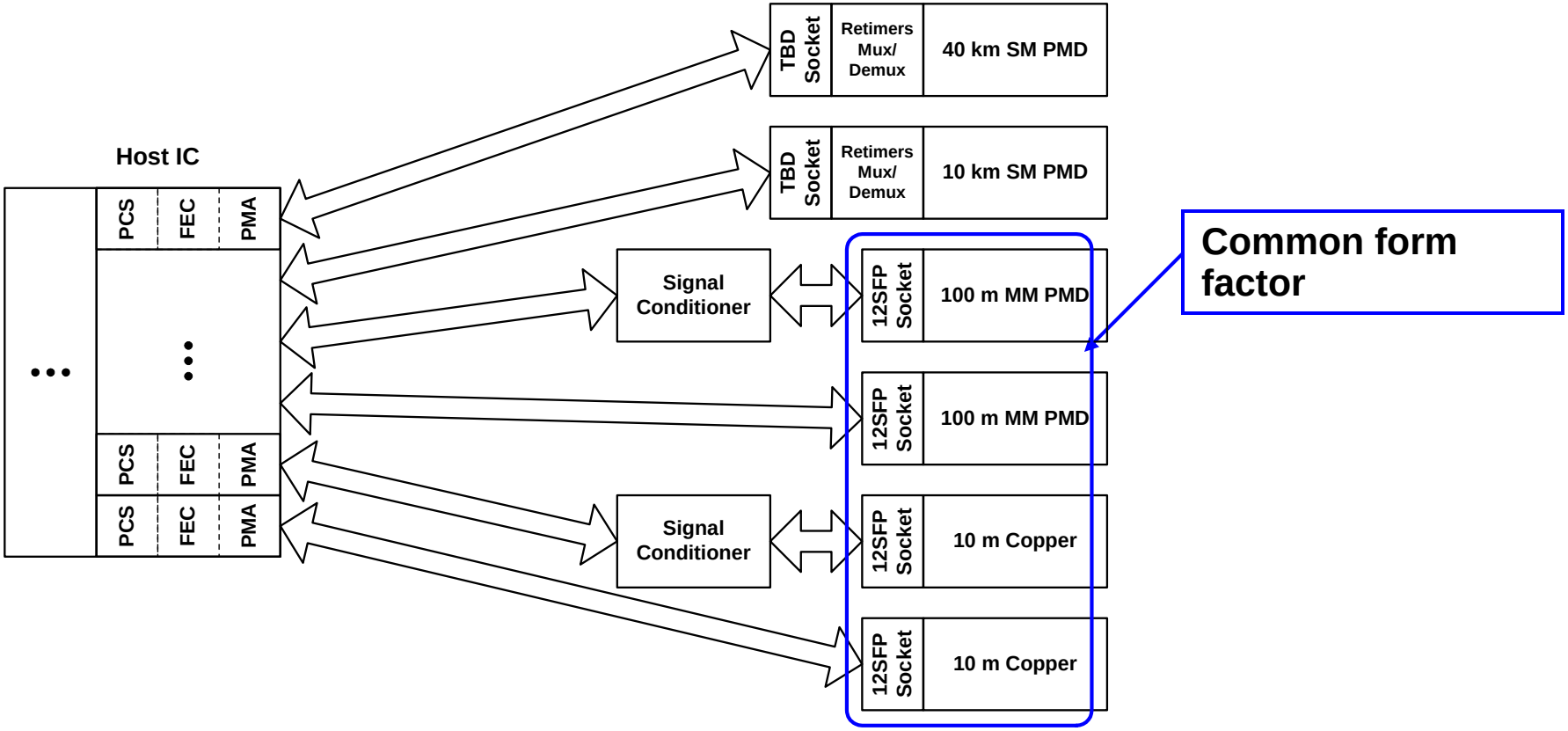
40G Variants & QSFP



- For the 40G variants, the QSFP form factor looks to be a good fit for pluggable 100m MM and 10m Copper variants.

Common form factor

Opportunities for a Common Form Factor
100G Variants & 12SFP



- For the 100m MM PMD and 10m copper variants, a common pluggable form factor seems reasonable. Although there is currently no popular form factor, reasonable 10 lane or 12 lane form factors appear plausible. Here a 12 lane form factor, 12SFP for short, is presumed.

TP1 & TP4 PMD Service Interface
Definition Rationale

- For the 100m OM3 variant, pluggable, multilane, non-retimed, limiting fiber optic modules are expected to provide the lowest power, highest density and lowest cost solution.
  - Direct connection between the module and host IC without intermediate signal conditioners is required to maximize the power, density and cost advantages.
- For the 10m copper cable assembly variant, direct connection between the host IC and cable assembly offers the same cost, density and power savings as with the 100m OM3 variant.
- For the 1m backplane variant, direct connection between the host IC and cable assembly offers the same cost, density and power savings as with the 100m OM3 variant.
- To enable direct connection for the 100m OM3 variant, the approach and characteristics on the following pages are proposed for consideration.
- As more details emerge, requirements for the 10m cable assembly and 1m backplane variants can be included.

TP1 & TP4 PMD Service Interface

Prologue – Jitter Allocation Targets

	GbE	8GFC	10G SFP+ SFF-8431	**40/100G Targets**
TP1 DJ, UI	0.100	0.170	0.100*	**0.150**
TP1 TJ, UI	0.240	0.310	0.280	**0.300**
TP4 DJ, UI	0.462	0.420	0.420	**0.400**
TP4 TJ, UI	0.749	0.710	0.700	**0.700**

* SFF-8431 specifies DDJ instead of DJ.

- Perhaps the most critical attributes of TP1 & TP4 are the jitter allocation. The above table provides information regarding previous choices.
- The targets were chosen to provide a better design point than those from either 8GFC or 10GBASE-SR as implemented in SFF-8431. With respect to 10G SFP+ in SFF-8431, significant relief is expected.

TP1 & TP4 PMD Service Interface
Goal and Approach

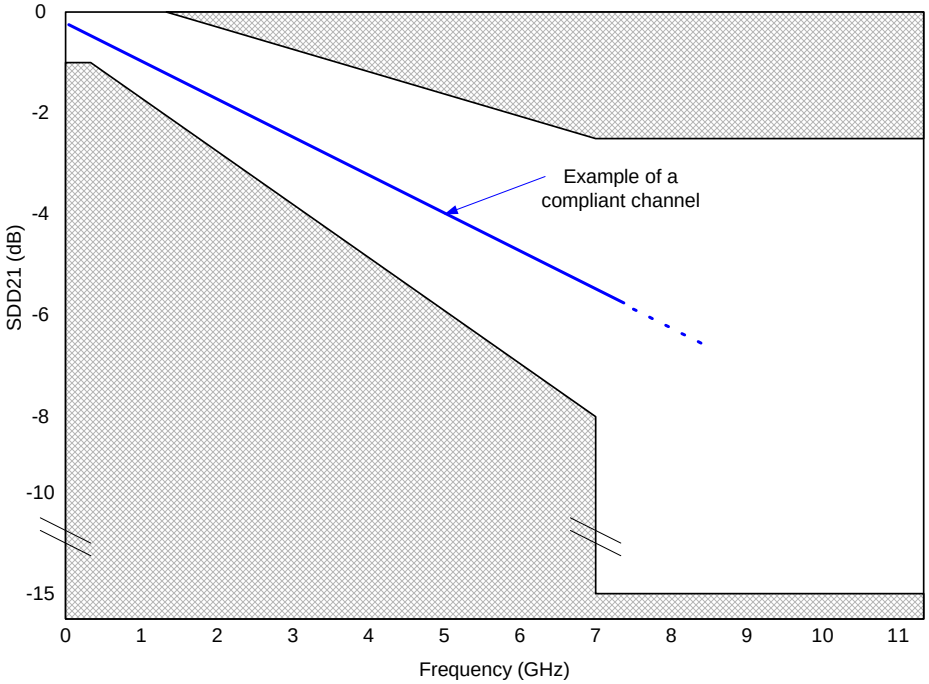
Goal: Establish an approach and specifications that enable direct connection and inter-operability between host ICs and pluggable, multilane, non-retimed, limiting fiber optic modules for a reasonable range of equipment designs

- The proposed approach does not place explicit requirements on the host IC, but, rather, provides far-end characteristics over worst case channels.
- The far-end characteristics for the host IC, TP1 & TP4, are based on experience gained from SFP+ (SFF8431) and 8GFC (FC-PI-4) developments. Included are jitter, signal levels, and reflection coefficients.
- The proposed channel is intended to support 150 mm to 200 mm of PCB traces without an intermediate connector and is defined by an SDD21 template.
- TP1 requirements are defined in an input characteristics table and TP4 requirements are defined in an output characteristics table that follow.
- Compliance, as with SFF-8431, is based on use of compliance test boards to improve measurement accuracy and reproducibility.

The intention is to maintain the same TP1 & TP4 requirements for the 40GBASE-SR4 and 100GBASE-SR10.

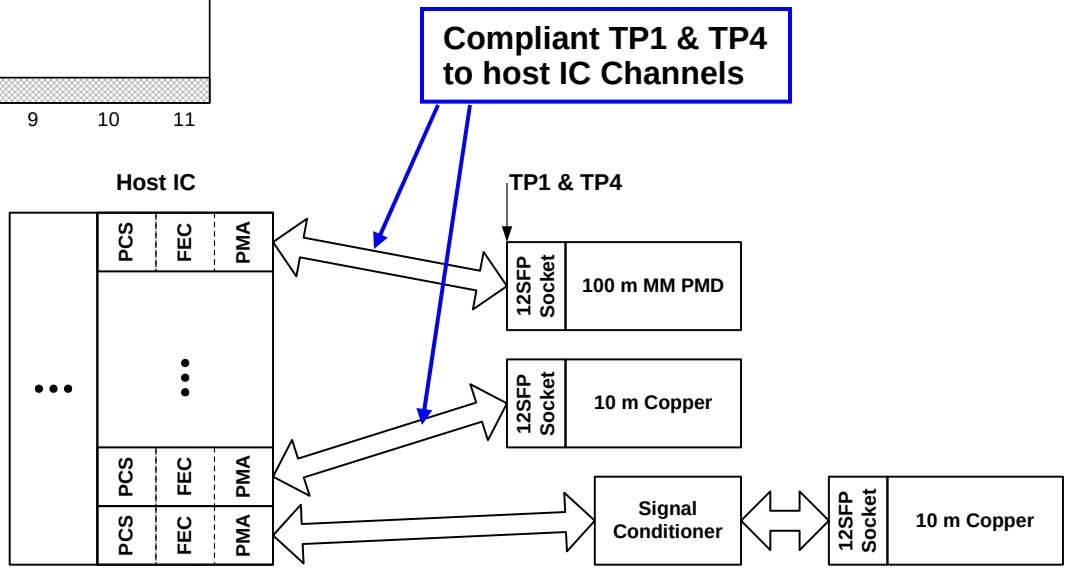
TP1 & TP4 to Host IC Channel

SDD21 Compliance Template



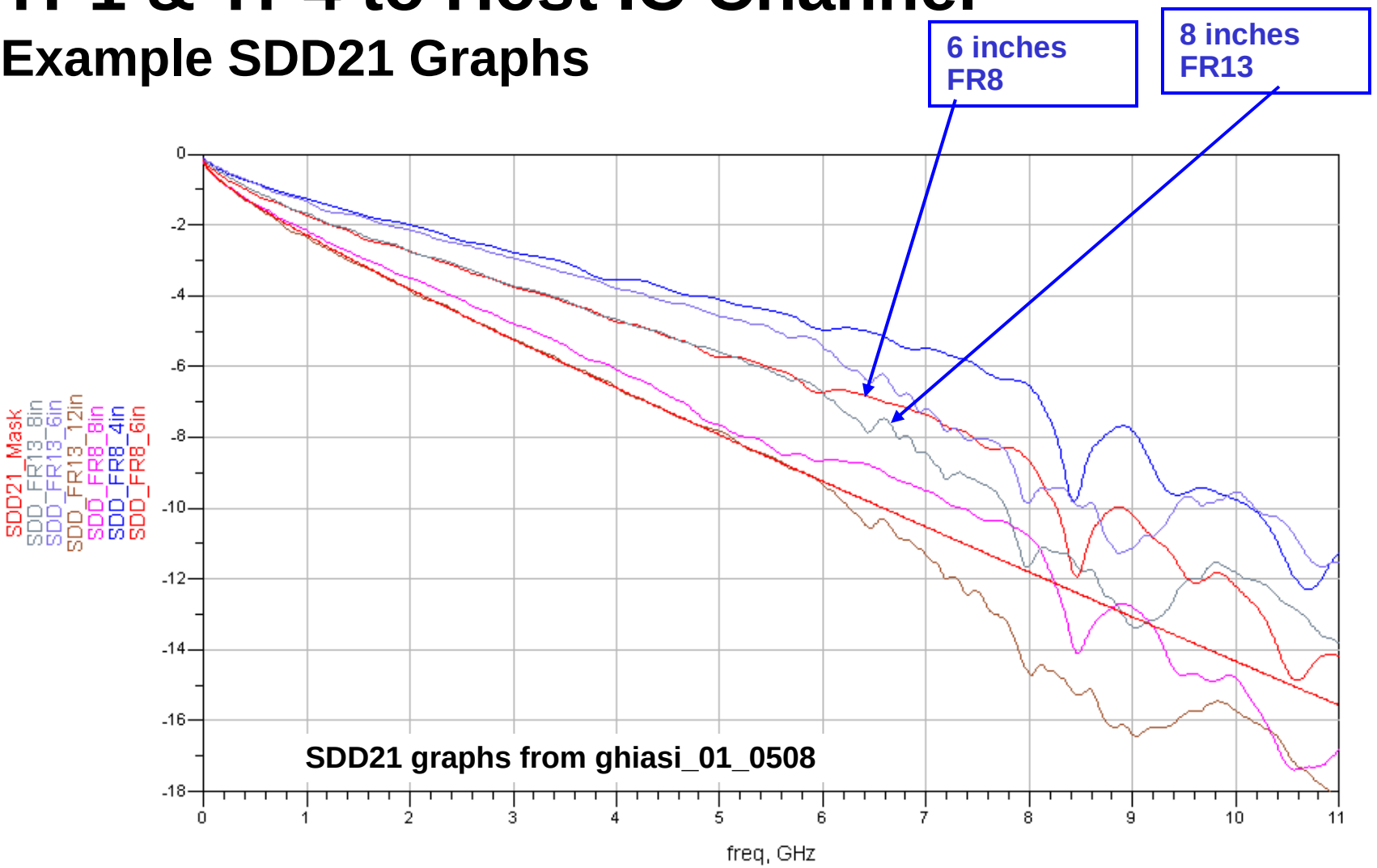
Characteristics are for each lane individually and are normative except where noted.

All items will benefit from additional study.



TP1 & TP4 to Host IC Channel

Example SDD21 Graphs



- The above examples for FR13- 8in, FR13- 6in, FR8-6in and FR8-4in all meet the proposed template.

TP1

40GBASE-SR4 & 100GBASE-SR10 Input Characteristics

Parameter Description	Value	Units	Conditions
Single ended input voltage tolerance range	-0.3 to 4.0	V	Ref'd to module signal common
AC common mode input voltage tolerance (min)	15	mV (RMS)	
Differential input reflection coefficient, SDD11 (max)	See Template A	dB	0.01 to 11.1 GHz
Reflected differential to common mode conversion, SCD11 (max)	-12	dB	0.01 to 11.1 GHz
Total jitter tolerance	0.30	UI	At BER = 1E-12
Deterministic jitter tolerance	0.15	UI(p-p)	
Eye mask coordinates: X1, X2, Y1, Y2	0.15, TBD, 90, 350		TBD

Characteristics are for each lane individually and are normative except where noted.

All items will benefit from additional study.

TP4

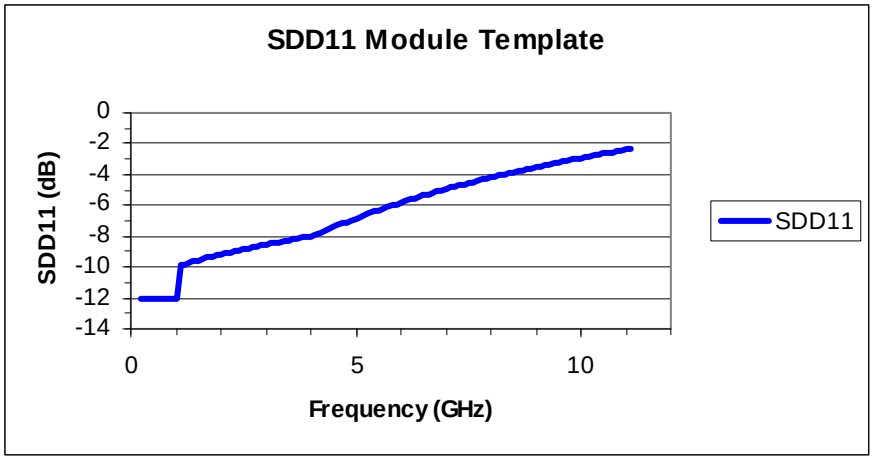
40GBASE-SR4 & 100GBASE-SR10 Output Characteristics

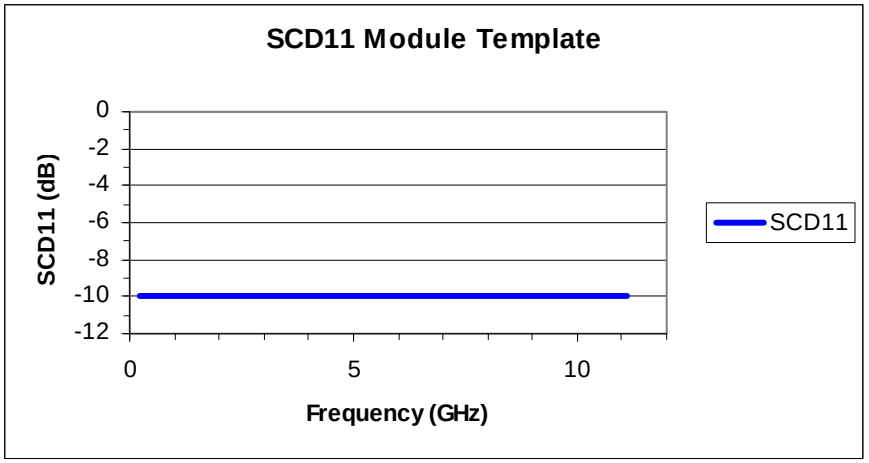
Parameter Description	Value	Units	Conditions
Single ended output voltage tolerance range	-0.3 to 4.0	V	Ref'd to module signal common
AC common mode output voltage (max)	7.5	mV (RMS)	
Termination mismatch at 1 MHz	5	%	
Differential output reflection coefficient, SDD22(max)	See Template B	dB	0.01 to 11.1 GHz
Common mode output reflection coefficient, SCC22 (max)	See Template C	dB	0.01 to 11.1 GHz
Output transition time, 20% to 80%, (min)	28	ps	
Total jitter	0.70	UI	At BER = 1E-12
Deterministic jitter	0.40	UI(p-p)	
Eye mask coordinates: X1, X2, Y1, Y2	0.35, TBD, 150, 425		TBD

Characteristics for are each lane individually and are normative except where noted.

All items will benefit from additional study.

TP1
Reflection Coefficient Characteristics





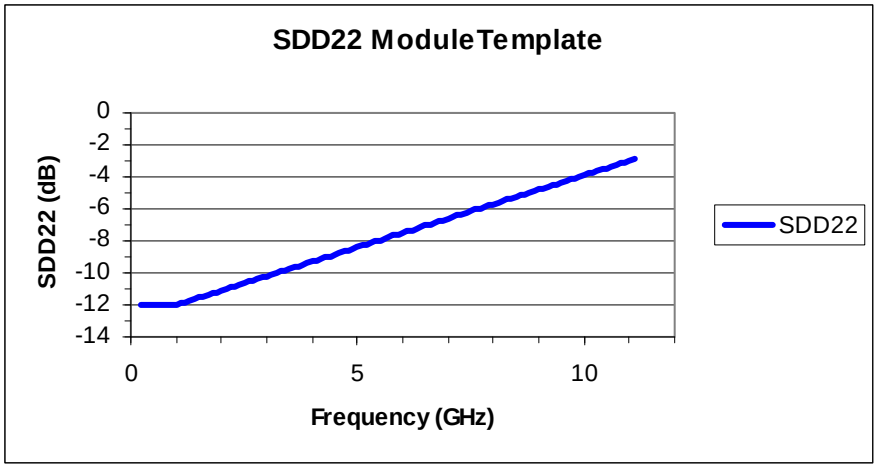
Template A

Characteristics are for each lane individually and are normative except where noted.

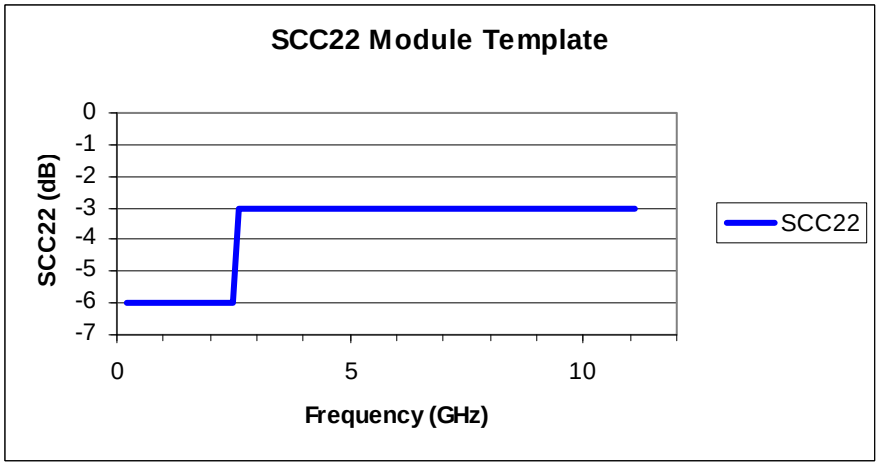
All items will benefit from additional study.

TP4

Reflection Coefficient Characteristics



Template B

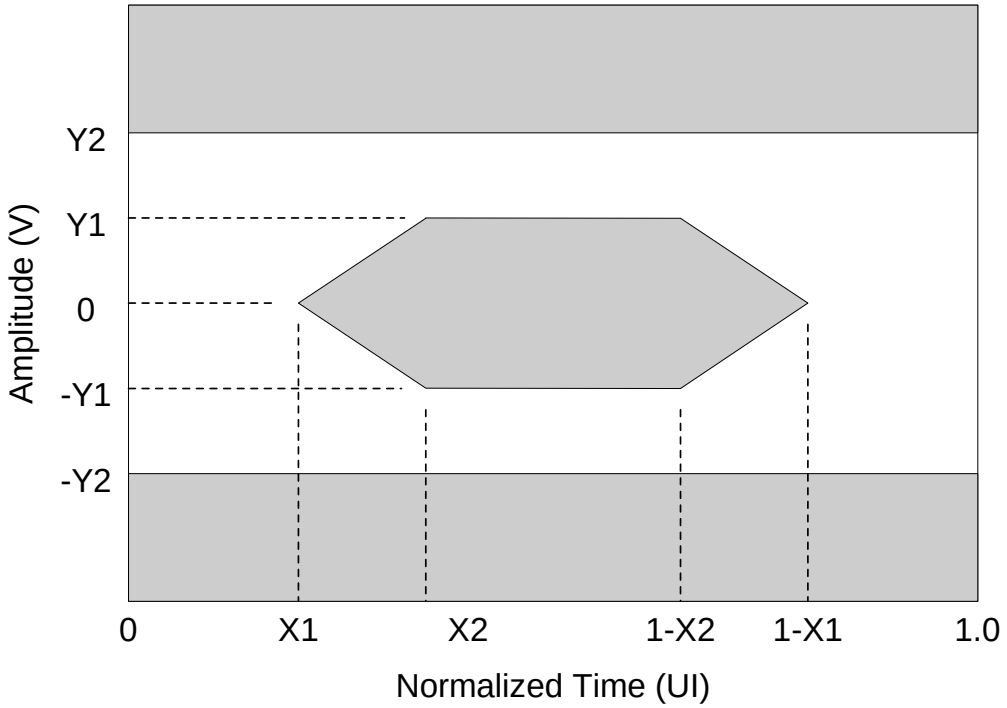


Template C

Characteristics are for each lane individually and are normative except where noted.

All items will benefit from additional study.

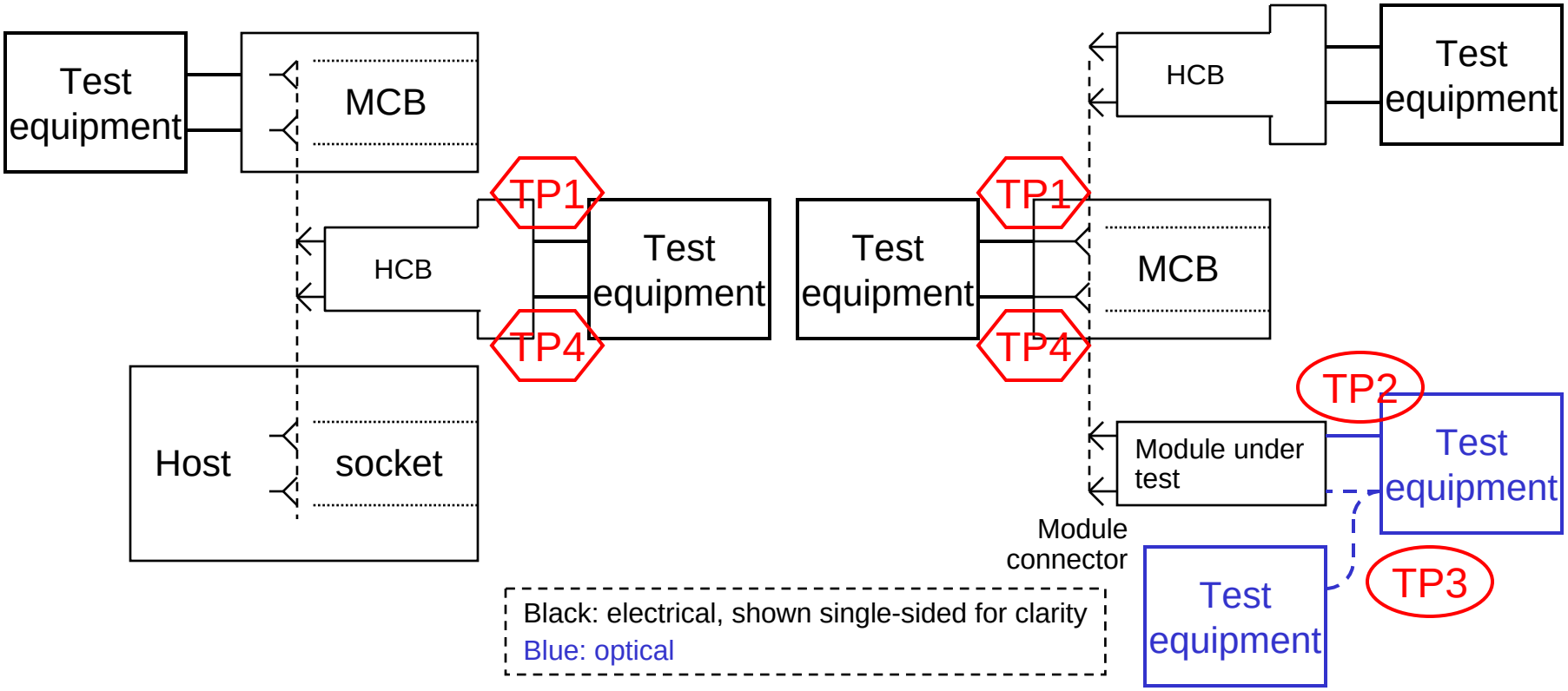
TP1 and TP4
Eye Mask



Characteristics are for each lane individually and are normative except where noted.

All items will benefit from additional study.

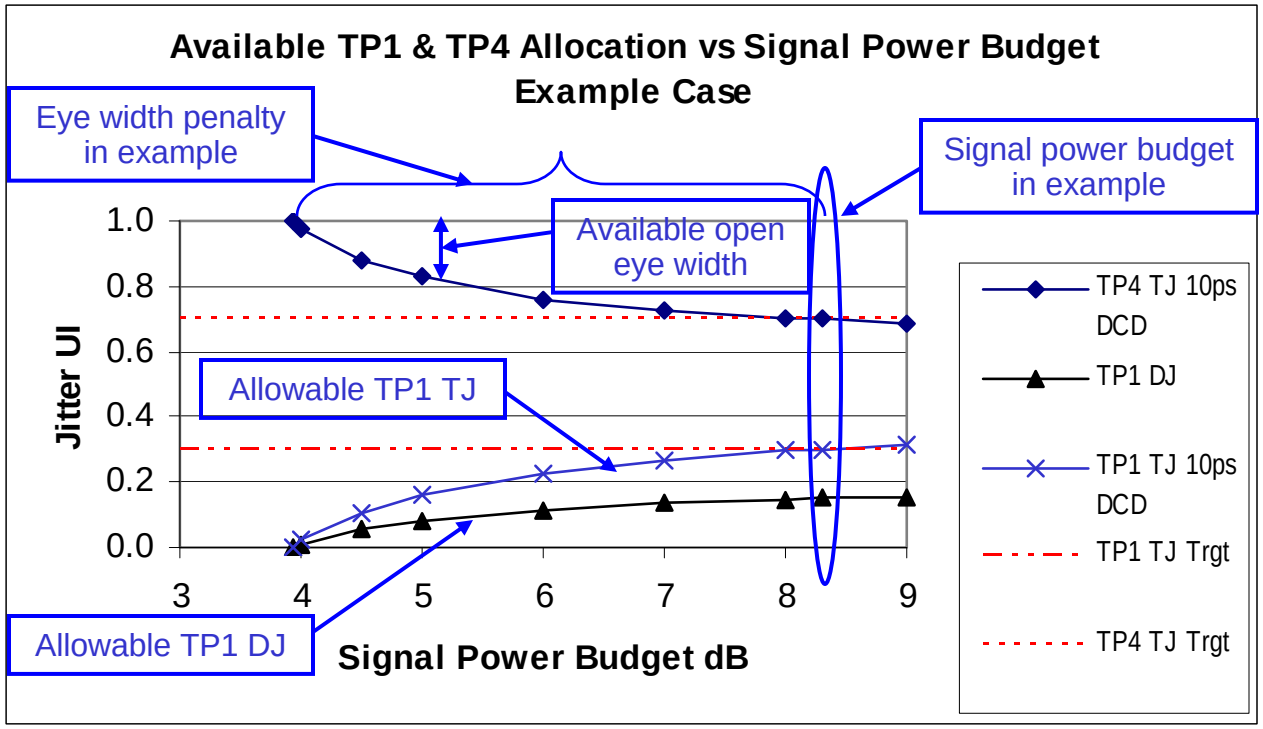
Use of compliance boards



- HCB (Host Compliance Board) Used to provide access at the far-end, TP1 & TP4, to Host IC signals and for calibration of module compliance test signals. Host system transmit and receive signal compliance are defined with the HCB inserted in the pluggable interface of the host.
- MCB: (Module Compliance Board) Used to provide access at TP1 & TP4 to module signals and for calibration of host compliance test signals. Module transmit and receive signal compliance are defined with the module inserted in the pluggable interface provided by the MCB.

Link Model Results

TP1 & TP4 Jitter Allocations Support



The above figure from petrilla_02_0508 is shown as a reminder that the signal budget and characteristics proposed for the 100m OM3 variant support jitter allocations of TP1(DJ) = 0.15 UI, TP1(TJ) = 0.30 UI and TP4(DJ) = 0.40 UI, TP4(TJ) = 0.70 UI. See also pepeljugoski_01_0508.

Conclusions, Recommendations & Next Steps

Conclusions:

- Cost, power and density advantages of 100m OM3, 10m copper cable assembly and 1m backplane variants are maximized by direct connection with the host IC and a single build standard for DTE that can be connected by a choice of the two PMD/media types that will dominate the data center is enabled.
- Robust solutions, inter-operability of pluggable modules and cable assemblies and market acceptance are enabled by well chosen required interface characteristics.
- This presentation provides a set of characteristics sufficient to enable direct connection between the proposed 100m OM3 variant and a host IC.

Recommendations:

- Jitter specifications for TP1 & TP4 should be included in 802.3ba.
- Additional specifications and the specification approach as outlined in the tables and templates in pages 14, 15, 16 through 22 should be considered for inclusion in 802.3ba.

Next Steps:

- Gather and incorporate feedback regarding host IC capabilities
- Coordinate TP1 and TP4 requirements with other PMD variants
- Collect information regarding crosstalk and other impairments related to multilane channels, stacked connectors and modules and incorporate.
- Upgrade proposed specifications.

References

- SFF-8431 Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module ”SFP+”: ftp://ftp.seagate.com/sff/SFF-8431.PDF
- FC-PI-4 Physical Interface-4 (8GFC): http://www.t11.org/index.htm
- ghiasi_01_0508
- pepeljugoski_01_0508
- petrilla_02_0508
- petrilla_01_0308