

Analysis of 40GBASE-SR4 & 100GBASE-SR10 Proposals

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Supporters

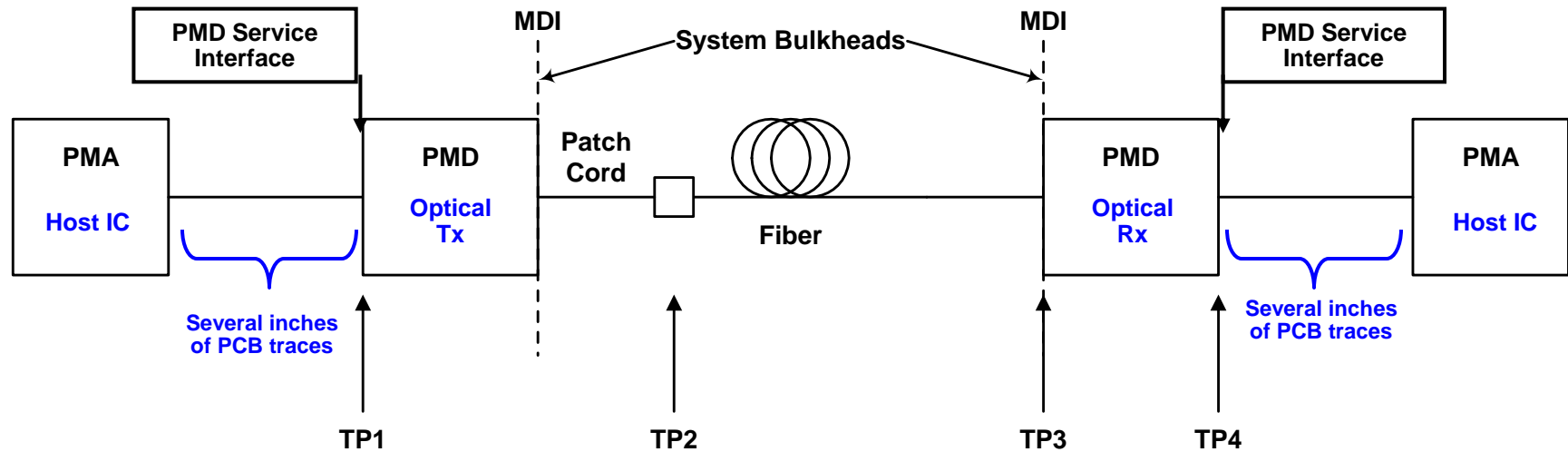
- Jonathan King, Finisar

Outline

- 802.3ba Alignment
- Elements for success - Reminder
- 40GBASE-SR4 & 100GBASE-SR10
Proposal Link Model Analysis
- Conclusion & Recommendation

802.3ba Alignment

802.3ba PMD Block Diagram



- The above block diagram shows relevant elements and interfaces for an optical link between two PMAs. The patch cord is included for the definition of TP2. Otherwise intermediate fiber connectors are not shown.
- TP1, TP2, TP3 and TP4 are traditional labels for interfaces of a fiber optic link. Here the PMAs may be host ICs and the PMDs, fiber optic modules.

Elements for Success

Reminder

- Total cost: less than ten/four 10 GbE solutions
- Power consumption: less than ten/four 10 GbE solutions
- High module density: higher than 10 GbE solutions
- Cable plant: 100 m of OM3 & up to 4 intermediate connections
- Reliability: better than ten/four 10 GbE solutions
- Appropriate design points

This presentation examines the aggregate choices in [pepeljugoski_01_0508](#), Proposal for a PMD for 100GBASE-SR10 and 40GBASE-SR4 and Related Specifications.

Link Model

- The 10GbE link model, 10GEPBud3_1_16a, available at http://www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/ was used for the analysis presented in the following pages.
- Jitter in the following pages follows dual-Dirac methodology and, where used, DJ is intended to be dual-Dirac DJ.
- Since the 10GbE link model is open, available to all and reasonably well-regarded, it is a useful tool for comparing various proposals and tradeoff among attributes.
- The objective is to analyze the aggregate of the choices in pepeljugoski_01_0508, Proposal for a PMD for 100GBASE-SR10 and 40GBASE-SR4 and Related Specifications. Since all attributes required for the 10GbE link model are not yet determined, e.g. a range for RIN12OMA is being explored, a base case is generated from the values found in pepeljugoski_01_0508 and supplemented with presumed values where needed. The choices are found in the following pages.

40GBASE-SR4 & 100GBASE-SR10 Proposal

Link Model Transmitter Attributes (Each Lane) – Base Case

- Min OMA: -3.0 dBm
- Min ER: 3.0 dB
- Min Center Wavelength: 840 nm
- Max RMS Spectral Width: 0.65 nm
- Max Transition Time (20%, 80%): 35 ps (1)
- Max RIN_{OMA}: -130 dB/Hz (2)
- RIN Coefficient: 0.70 (1)
- Mode Partition Noise Coefficient: 0.30 (1)
- Min Optical Reflection Tolerance: -12 dB
- TP1 Jitter Allocation: TJ = 0.300 UI, DJ = 0.150 UI (3)
- TP2 Jitter Allocation: TJ = 0.488 UI, DJ = 0.284 UI (3)

Above attributes are included in the proposal unless otherwise noted.

(1) Attribute is required for link model but is not part of proposal.

(2) Proposal is examining values in the range of -128 dB/Hz to -132 dB/Hz.

(3) TP1 DJ, TP1 TJ & TP2 DJ are informative.

40GBASE-SR4 & 100GBASE-SR10 Proposal

Link Model Receiver Attributes (Each Lane) – Base Case

- Max Sensitivity: -11.3 dBm (1)
- Min Bandwidth: 7500 MHz (1)
- RMS Base Line Wander: 0.025 (1)
- Max Rx Reflection: -12 dB
- TP3 Jitter Allocation: DJ = 0.284 UI, DCD = 0.103 UI (1)
- TP3 Jitter Allocation: TJ = 0.511 UI (2)
- TP4 Jitter Allocation: TJ = 0.700 UI
- TP4 Jitter Allocation: DJ = 0.367 UI (2)

Above attributes are included in the proposal unless otherwise noted.

(1) Attribute is required for link model but is not part of proposal.

(2) TP3 TJ, & TP4 DJ are informative.

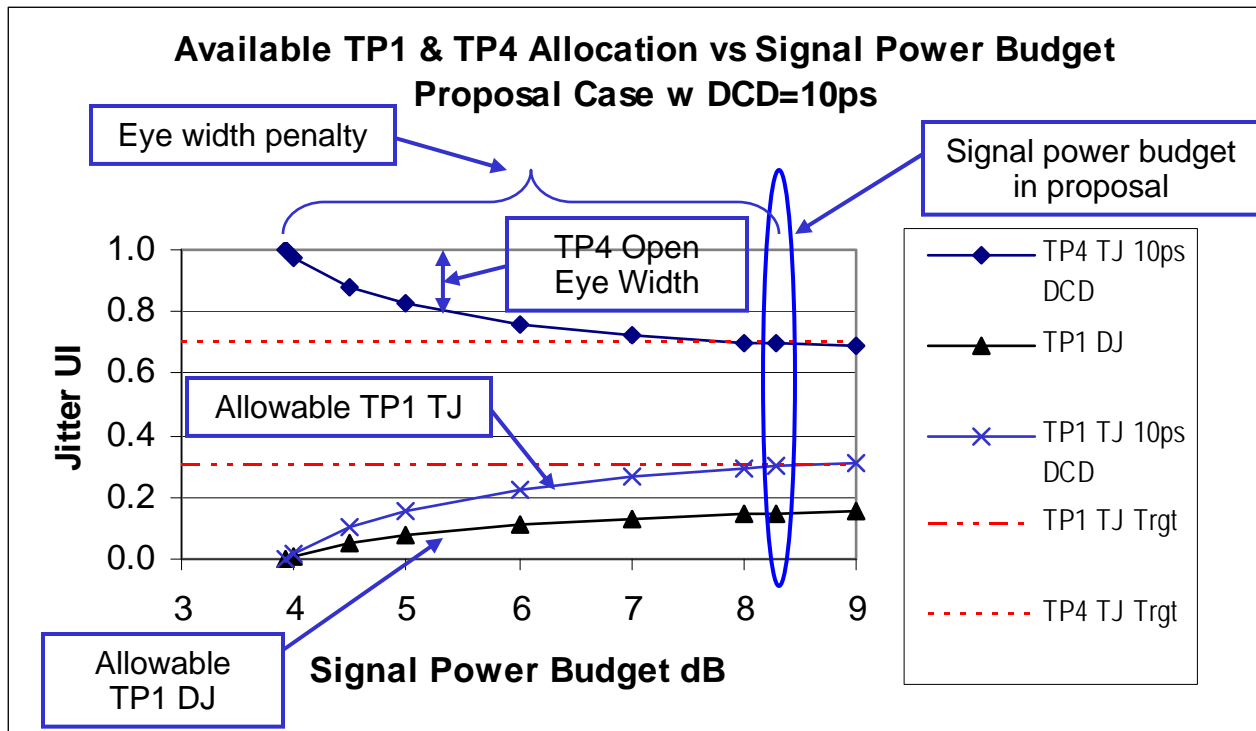
40GBASE-SR4 & 100GBASE-SR10 Proposal

Link Model Receiver Attributes (Each Lane) – Base Case

- Signal Rate: 10.3125 GBd
 - BER: $< 10^{-12}$ (Q = 7.034)
 - 100 m of OM3
 - 1.5 dB connector loss allocation
 - Signal Power Budget: 8.3 dB (1)
 - Attenuation = 0.36 dB (1)
 - Center Eye Penalties (1)
 - Pisi = 1.40 dB
 - Pdj = 0.22 dB
 - Pmn = 0.30 dB
 - Pmpn = 0.02 dB
 - Prin = 0.15 dB
 - Pcross = 0.14 dB
 - 0.30 UI Eye Width Penalty = 4.11 dB (1) (see figure on page 9)
- Above attributes are included in the proposal unless otherwise noted.
- (1) Output of link model.

40GBASE-SR4 & 100GBASE-SR10 Proposal

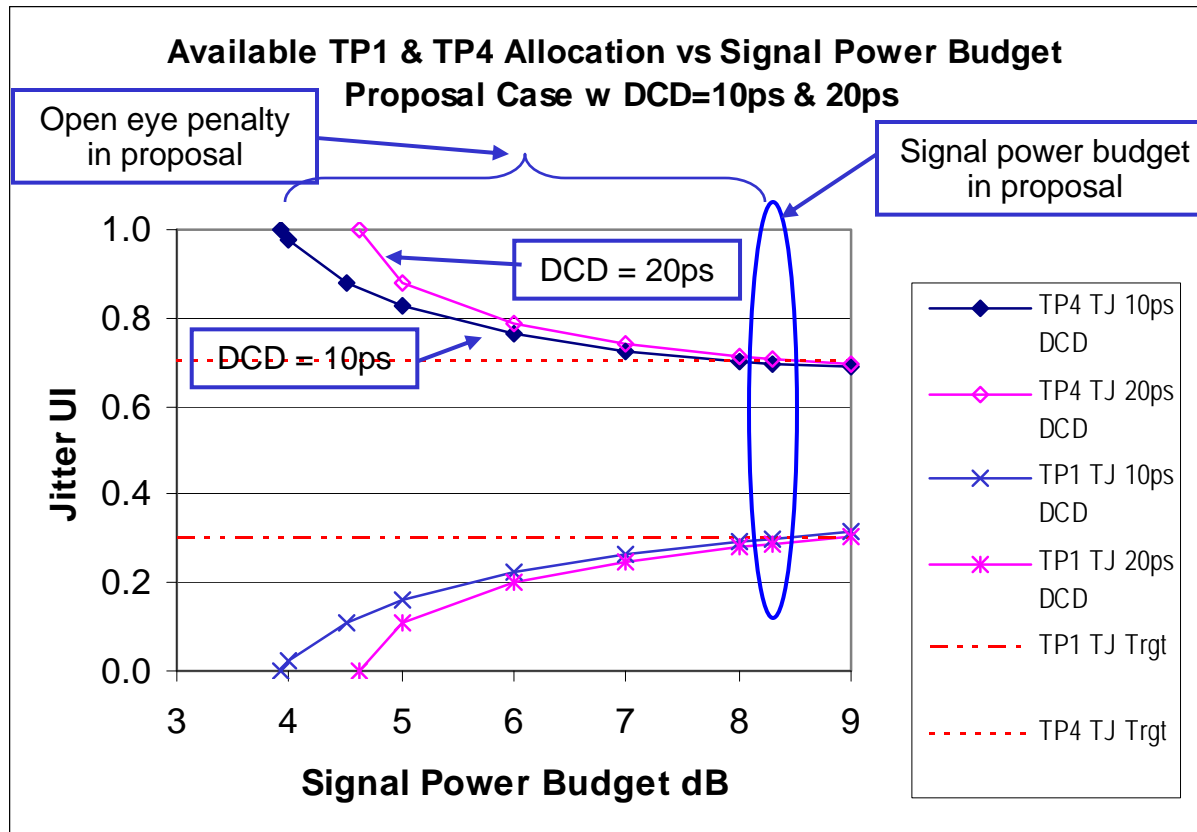
Link Model Results – Base Case TP1 & TP4 TJ Contours



- The figure above shows the relationship between available jitter allocation and signal power budget.
- Targets jitter allocations are shown for TP1 TJ = 0.30 UI & TP4 TJ = 0.70 UI.
- The proposal is based on a 8.3 dB signal power budget and, as shown above, can support jitter allocations of TP1(DJ) = 0.15 UI, TP1(TJ) = 0.30 UI and TP4(TJ) = 0.70 UI.

40GBASE-SR4 & 100GBASE-SR10 Proposal

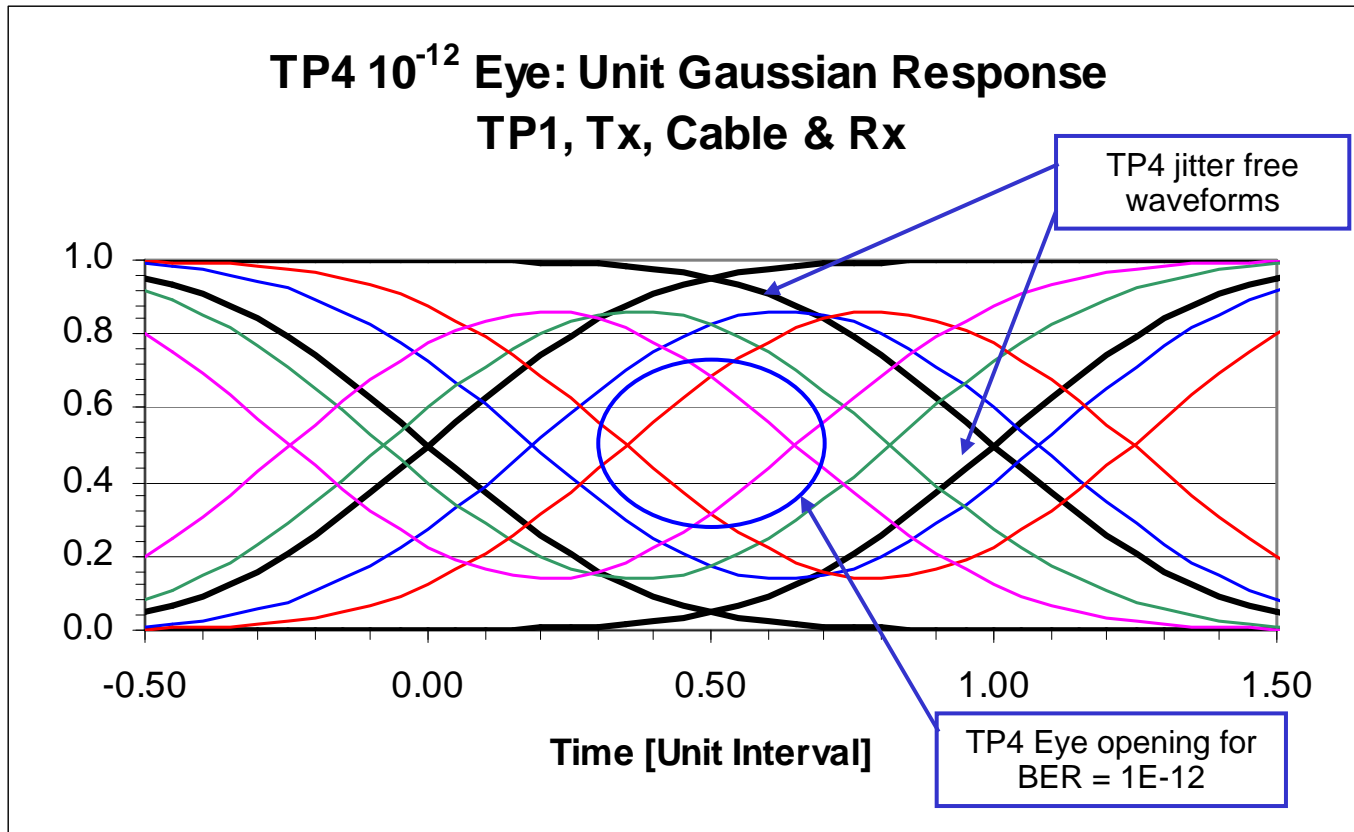
Link Model Results – TP1 & TP4 TJ Contours w DCD = 10ps & 20ps



- The above figure presents contours for TP3 DCD allocations of 10 ps and 20 ps. Referenced to the 10 ps case, DCD of 20 ps generates additional 0.61 dB of power penalties. This translates to an eye width loss of 1.7 ps. For DCD of 27 ps, referred to the 10 ps case, an additional 1.68 dB penalty is generated resulting in an eye width loss of 4.4 ps.

40GBASE-SR4 & 100GBASE-SR10 Proposal

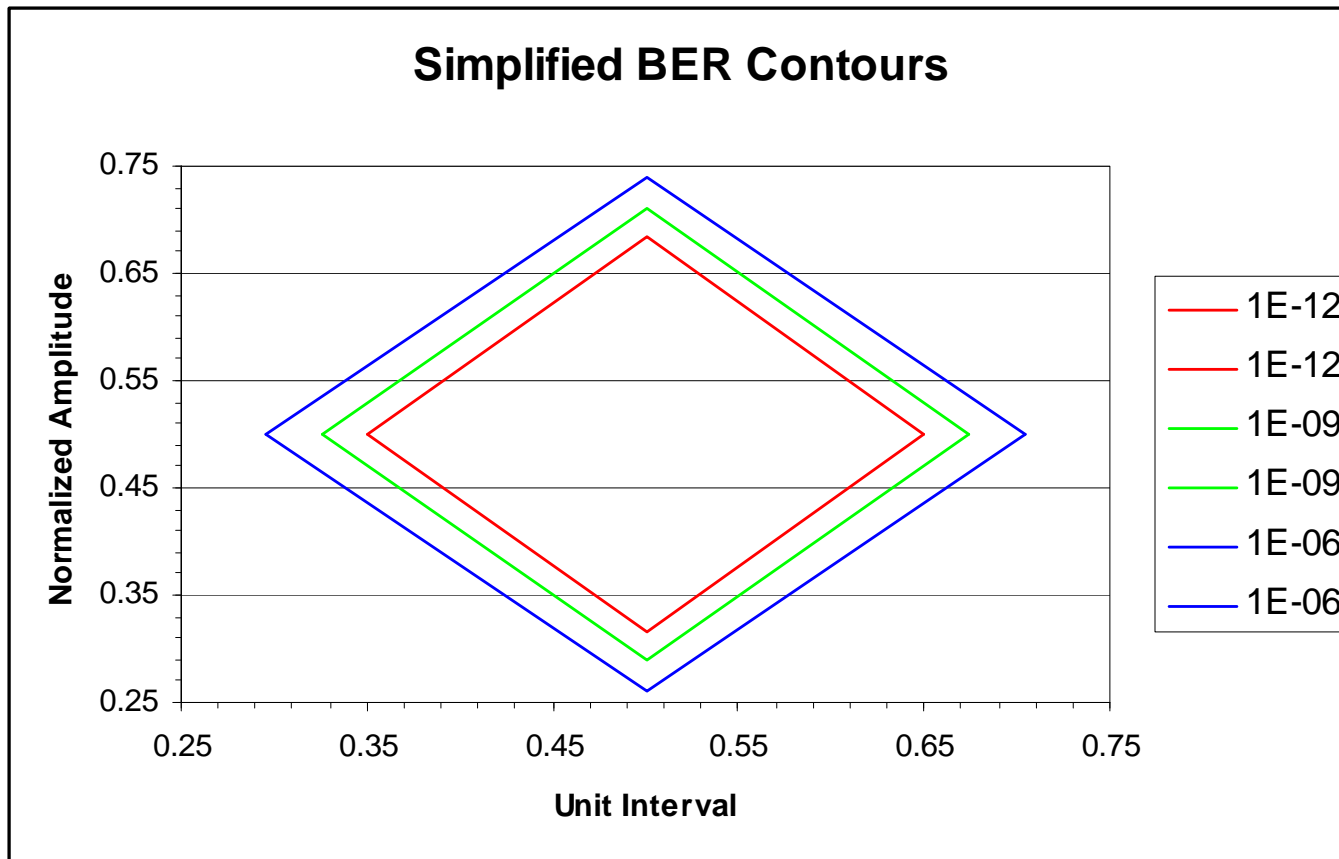
Link Model Results – Base Case TP4 Jitter Contours



- The above figure presents waveforms at TP4 for the proposal and base conditions.
- Note that the TP4 eye opening is approximately diamond shaped.

40GBASE-SR4 & 100GBASE-SR10 Proposal

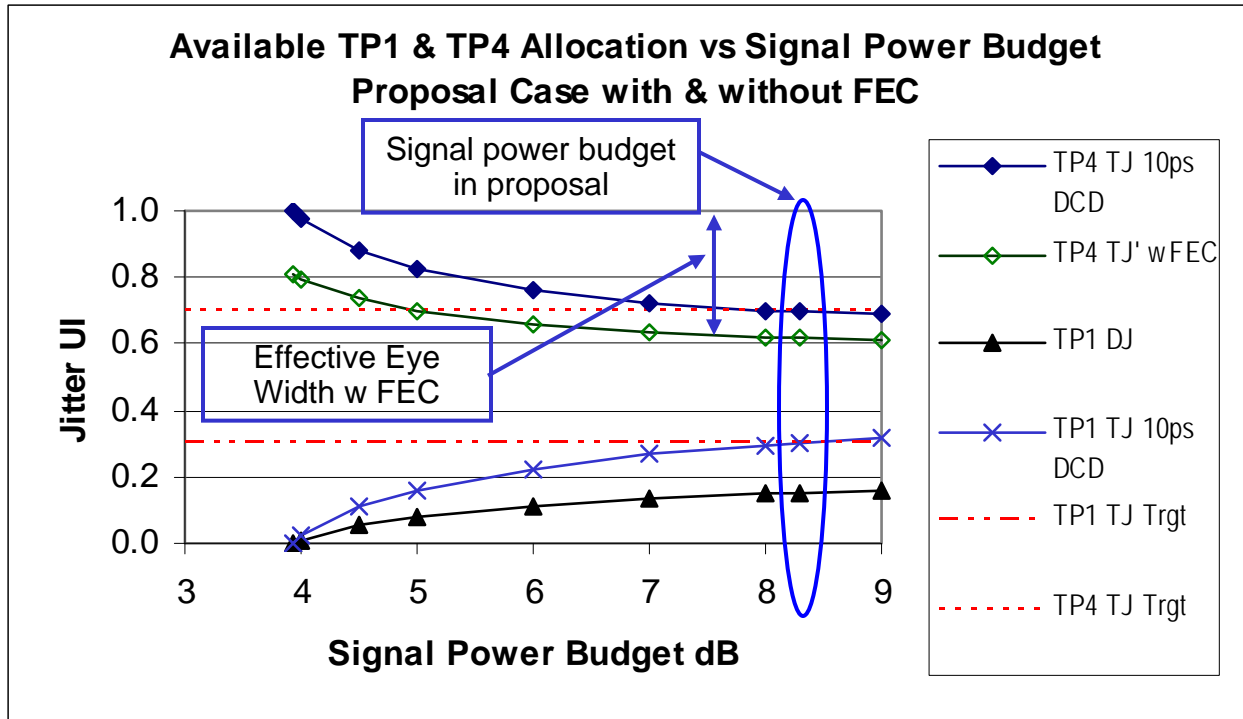
Link Model Results – Base Case TP4 Simplified BER Contours



- The above figure displays simplified BER contours for the proposal and base conditions. These simplified contours are defined by determining the 0.50 amplitude crossing points and the amplitude at 0.50 of the unit interval of the worst case waveforms shown on the preceding page.

40GBASE-SR4 & 100GBASE-SR10 Proposal

Link Model Results – TP4 Contours with & without FEC



- A reminder - Use of FEC may provide some relief in the struggle to allocate jitter properly.

Conclusion & Recommendation

Conclusion:

- The choices and signal power budget in pepeljugoski_01_0508 are sufficient to support target jitter allocations at TP1 and TP4.

Recommendation:

- Accept pepeljugoski_01_0508 as the basis of the work of the task force towards writing the first draft standard for 40GBASE-SR4 and 100GBASE-SR10.

References

- pepeljugoski_01_0508
- petrilla_01_0308
- The 10 GbE link model, 10GEPBud3_1_16a
http://www.ieee802.org/3/ae/public/adhoc/serial_pmd/documents/10GEPBud3_1_16a.xls