# Appropriate Support for OTN Baseline Proposal

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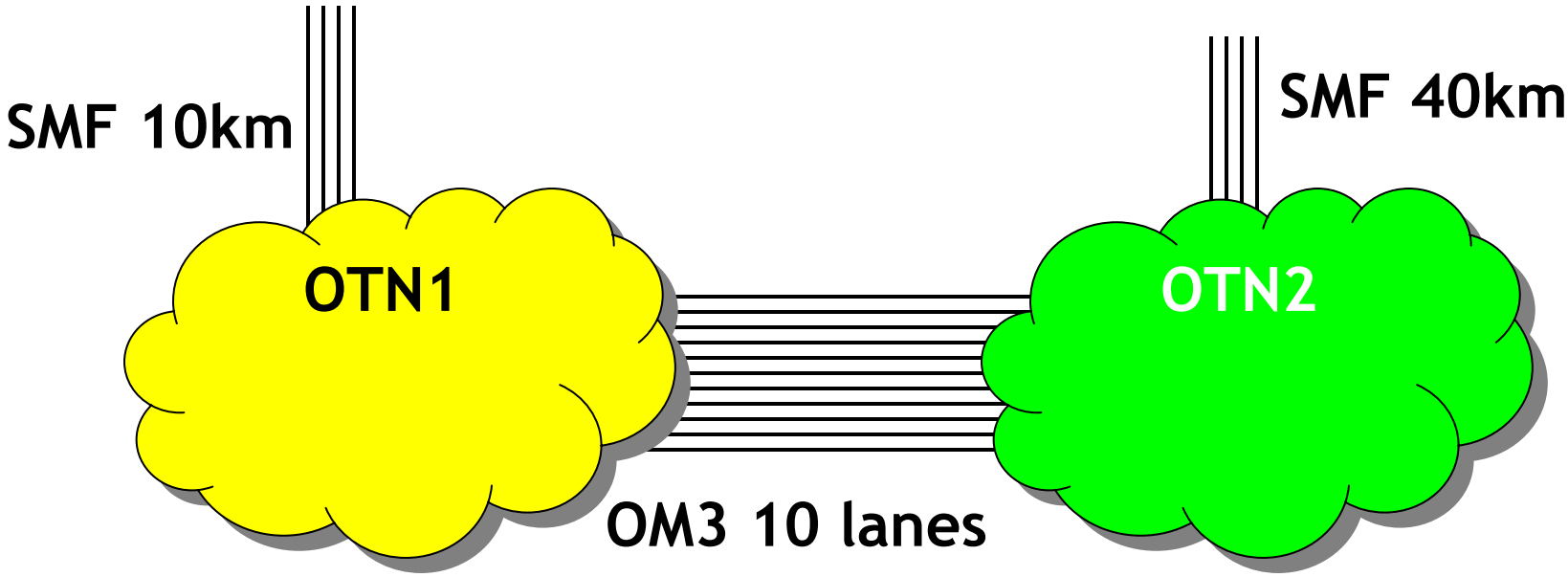
# Supporters

- Thomas Fischer – Nokia-Siemens Networks
- Pete Anslow – Nortel Networks
- Ralf-Peter Braun – Deutsche Telekom
- Martin Carroll – Verizon
- Ghani Abbas – Ericsson
- Arne Alping – Ericsson
- Chris Cole – Finisar
- Mark Gustlin – Cisco
- Osamu Ishida – NTT
- George Young – AT&T
- Gary Nicholl - Cisco

# Key elements of OTN support

- Use a Lane Independent PCS to enable different Ethernet PMDs to be used at the OTN ingress/egress
  - Key feature of MLD
- 40 GbE must fit into the OPU3 payload with a minimum of PCS codeword and timing transparency
  - Limitation on control block types to permit transcoding
- Lane Marker transparency for 40 GbE
  - ITU-T decision, but maintain spare value in 4-bit representation of control block types available for encoding lane markers if necessary
- Link fault signaling for 802.3ba Ethernet over OTN can use existing mechanisms from 802.3ae

# Independence of Ethernet PMDs in OTN mapping

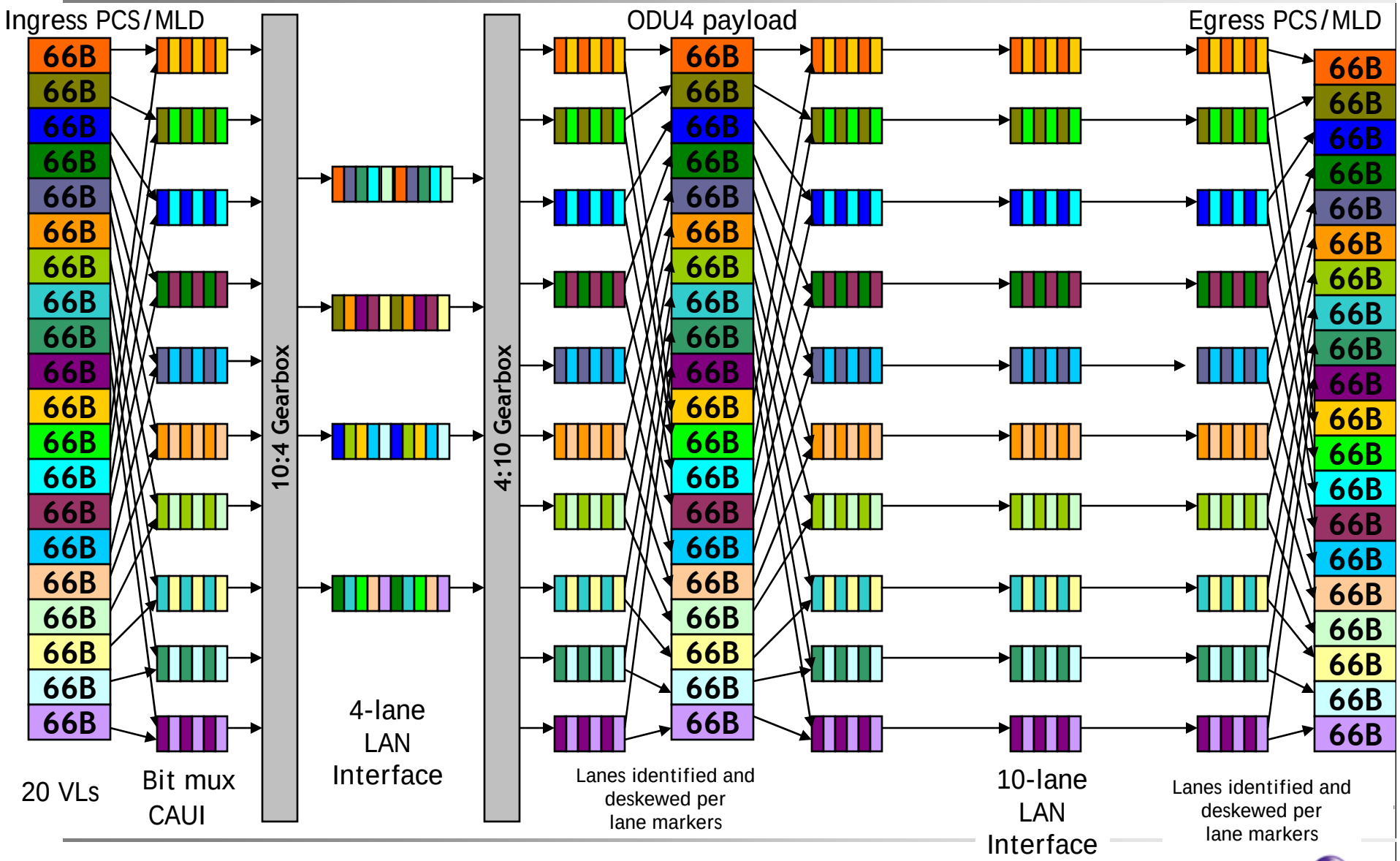



**The sequence of bits transported across OTN should not depend on which physical interface is chosen for Ethernet at the ingress or egress**

# Common PCS – Good news

- The MLD proposal comprises a common PCS that is used across all Ethernet PMDs - see gustlin_01_0308
- As the complexity of using the MLD PCS is no more than that of managing skew to within 32UI (see shafai_01_0308), consensus is moving towards using the MLD PCS for all PHY types including 40 GbE backplane
- Skew in OTN must be managed so that Ethernet over OTN does not exceed LAN deskew budget (OTN must deskew)

# Example: Four-Lane 100 GbE LAN interface at OTN ingress; 10-lane 100 GbE LAN interface at OTN egress.



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# Common PCS Proposal (100 GbE and 40 GbE)

- Adopt MLD with 64B/66B coding as the common PCS for all 802.3ba interfaces. This enables:
  - A single canonical form to be used for mapping of any 802.3ba interface with at least codeword transparency over OTN
  - Selection of different Ethernet PMDs at the OTN ingress and egress

# OTN support for 40 GbE

- **Two ways to provide 40 GbE transparent transport over OTN:**
  - Choose a MAC bit-rate (e.g., 38.9 Gbit/s) such that 64B/66B coding and lane marker insertion results in a bit-stream that fits the payload area of an OPU3 (not preferred)
  - Impose strict requirements on PCS codeword set that permits codeword transparent mapping of 40 GbE into payload of OPU3 (preferred)
- **Feasibility for codeword transparent mapping from 40.0 Gbit/s MAC rate into capacity of OPU3 payload demonstrated in trowbridge_01_0707, with possible improvements shown in trowbridge_01_0308 (actual standard to be specified as mapping of 40 GbE into OTN by ITU-T SG15)**
  - The proposed transcoding method requires 15 or fewer control block types to be used in underlying 64B/66B code
  - A single additional (among the 16 available) control block type can be used to encode a lane marker, with 56 bits available for a very sparse coding of the lane number
- **10G Base-R 64B/66B coding uses 15 control block types. 40GbE/100GbE may use fewer control block types if packet and ordered set start is restricted to an 8-byte boundary**
- **To rely on transcoding, a fixed, limited set of control block types understood by both IEEE and ITU-T is essential to specification of the mapping of 40 GbE into OPU3 and interoperable implementations**

# Possible Changes to 64B/66B for 40 GbE and 100 GbE given 8-byte boundary for packet start and ordered sets

Ordered sets can't start in 5th lane

Packets can't start in 5th lane

| Input Data | Sync | Block Payload | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Bit Position: / Data Block Format: | 0 1 | 2 | | | | | | | 65 |
| $D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$ | 01 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
| Control Block Formats: | | Block Type Field | | | | | | | |
| $C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0x1e | $C_0$ | $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$ | 10 | 0x33 | $O_0$ | $D_1$ | $D_2$ | $D_3$ | | $D_5$ | $D_6$ | $D_7$ |
| $O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$ | 10 | 0x66 | $D_1$ | $D_2$ | $D_3$ | $O_0$ | | $D_5$ | $D_6$ | $D_7$ |
| $S_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$ | 10 | 0x55 | $D_1$ | $D_2$ | $D_3$ | $O_0$ | $O_4$ | $D_5$ | $D_6$ | $D_7$ |
| $S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$ | 10 | 0x78 | $D_1$ | $D_2$ | $D_3$ | $D_4$ | | $D_5$ | $D_6$ | $D_7$ |
| $O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0x4b | $D_1$ | $D_2$ | $D_3$ | $O_0$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0x87 | | $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0x99 | $D_0$ | | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0xaa | $D_0$ | $D_1$ | | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$ | 10 | 0xb4 | $D_0$ | $D_1$ | $D_2$ | | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$ | 10 | 0xcc | $D_0$ | $D_1$ | $D_2$ | $D_3$ | | $C_5$ | $C_6$ | $C_7$ |
| $D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$ | 10 | 0xd2 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | | $C_6$ | $C_7$ |
| $D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$ | 10 | 0xe1 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | | $C_7$ |
| $D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$ | 10 | 0xff | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | |

Figure 49–7—64B/66B block formats

It is expected that the 64B/66B coding for 40GbE and 100 GbE will use between 11 and 15 control block types, leaving one 4-bit code free for encoding of lane markers if necessary

# 40 GbE into OPU3 – what can break the mapping?

- Someone could implement a proprietary extension that used non-standard control block types
  - o Extremely unlikely area for proprietary extension as proper packet delineation depends on control block types and misuse could lose packet framing and impair MTTFPA; however
  - o As a safeguard, the standard should contain extremely strong language to prevent proprietary extensions in this area
- Evolution of the standard could allocate new control block types that are not anticipated by the OTN mapper
  - o As a safeguard, the relationship between IEEE 802.3 and ITU-T Recommendation should be clearly noted in the standards

# OTN support for 40 GbE proposal

- The aggregate PCS encoded bit-rate for 40 GbE including 64B/66B coding with inserted MLD lane markers shall be no more than 41.25 Gbit/s ±100ppm
- Aside from MLD lane markers, PCS codewords are 64B/66B encoded blocks similar to those used in 10G Base-R (IEEE Std 802.3 clause 49)
- The PCS coding for 40 GbE shall use no more than the 15 control block types specified for 10G Base-R (likely fewer, if 8-byte alignment for packet start and/or ordered sets)
- The equivalent of Figure 49-7 for the 40 GbE PCS shall include the following text:
  - **"Control block types not listed in Figure xx-yy shall not be transmitted and shall be considered an error if received"**
  - **"The mapping of 40G Base-?? signals into OPU3 (to be) specified in ITU-T Recommendation G.709 depends on the set of control block types shown in Figure xx-yy. Any change to the coding specified in Figure xx-yy must be coordinated with ITU-T Study Group 15."**

# Link Fault Signaling for Ethernet over OTN

**LF will be transmitted on the Ethernet interface as the forward defect indication when failures are detected within the OTN network (using the same sequence ordered set as in 802.3ae)**

- **Consistent with the definition of link fault signaling (LF/RF) in Clause 46**
- **An OTN failure is treated no differently than any other failure between remote and local RS (Clause 46)**
- **Nothing needs to be added or changed for 802.3ba**
- **The equipment functions specified by ITU-T SG15 supporting the OTN mappings for 40GE and 100GE should clarify that Local Fault (LF) should be inserted on the downstream (egress) ethernet interface in the event of OTN failures**